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The AMANDA-B 1997 Raw Data Format

This is an expanded version of the format description for 1997 AM-B
that was already distributed out by P. Mock.

Some Preliminaries:
        The Am-B DAQ reads in data from CAMAC devices from two separate
CAMAC crates.  The data is stored in separate memory buffers in the
list processors.  Since each memory buffer only reads out data from
devices in a given crate, and since most buffers contain several 10's
of events, the DAQ computer (MAC) combines the buffers to build complete
events from the two buffers which are read out sequentially every ~0.6s.
        The devices in the Am-B DAQ CAMAC crates are:

Slot    Crate1                          Crate2
1       TDC (Lec 3377)                  TDC (Lec 3377)
2       TDC (Lec 3377)                  TDC (Lec 3377)
3       TDC (Lec 3377)                  TDC (Lec 3377)
4       TDC (Lec 3377)                  TDC (Lec 3377)
5       TDC (Lec 3377)                  TDC (Lec 3377)
6       pADC (PS 7164)                  pADC (PS 7164)
7       pADC (PS 7164)                  pADC (PS 7164)
8       pADC (PS 7164)                  pADC (PS 7164)
9       pADC (PS 7164)                  pADC (PS 7164)
10      pADC (PS 7164)                  pADC (PS 7164)
11      pADC (PS 7164)                  pADC (PS 7164)
12      pADC (PS 7164)                  pADC (PS 7164)
13      pADC (PS 7164)                  pADC (PS 7164)
14      pADC (PS 7164)                  pADC (PS 7164)
15                                      pADC (PS 7164)
16      TDC (Lec 3377)
17      TrueTime GPS Int.(UW)
18      Dig OM Input Reg (Jor 60A)      LaPatel Delay
19                                      Output Register (Jor 41)
20      Output Register (Jor 41)        Scaler (Lec 2551)
21      Interrupt Reg (Jor 63  )        TrueTime GPS Interface (UW)
22      Dataway Disp (Jor 203 )         Dataway Display(Jor 203 )
23      List Processor (Hytec 1341)     List Processor (Hytec 1341)
24      SCSI Controller (Jor 73A)       SCSI Controller (Jor 73A)

The readout order is determined by the KMAX Online software, but it
is not important.  If you want to know this detail, then consult with
S. Barwick.

During event building,  ONLINE software repacks the raw data that was
readout from the memories in the List Processors, and deletes zero
bytes that was added during the transfer of data from the CAMAC crates
into the Mac memory.  The packing routine writes the TDC data and ADC
data into more compact structures.  These actions were implemented in
late Feb 97 to reduce the amount of data transferred across the MAP0
network.  During most of 1997, the AMANDA-B DAQ wrote data at ~40kB/s
sustained.  The reduced data traffic permitted  one Dec Alpha in
dome could run the extraction, Gzipping, and tar programs while simultaneously
acquiring data from the Am-A and Am-B DAQs.(see recent memo by G. Hill)
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AMANDA-B 1997 raw data (after late Feb 97)

Note: During the Austral Summer, and prior to late Feb 1997, the data
format was different than described in this section.  However, Pat's reader
subroutine knows the details and translates the data correctly.  Noteably,
the zero suppression was not implemented, the 4 byte format of the the 3377
was used (which is the way the data is read out by the List Processor), and
the pkADC have unique header words, rather than the single header word as
implemented in the more compact format.
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The AMANDA-B 1997 raw data has a hierarchical structure.  The highest
level is the raw data files.  The raw data files contain a variable
length structure called a "record".  There are three types of data
records, which are called the configuration record, event record, and house
keeping record.  Note that the housekeeping record was eliminated in the
1997 data, but was readout in previous years. The record delimiters
(see Table 1) are not unique in the data stream (which means that some
of the CAMAC modules can produce data with the same bytes as the delimiter)
, except for the End_of_Record delimiter which is unique.  Therefore,
a record delimiter can only be recognized at the beginning of a file or after
an End_of_Record delimiter.  Each record has the general form shown in Table 2.


Record Delimiters (Table 1)
---------------------------
Configuration   0x00000101  First record in every file
Event           0x00000001  Contains the event data from both LP buffers
House keeping   0x00000003  Not used in 97, but used in previous years
End_of_Record   0xffffffff  Ends each of the previous records

Record Form (Table 2)
---------------------
Record type delimiter   4-bytes
Record size             4-bytes
...contents...
End_of_Record delimiter 4-bytes


The size of Configuration records are the same for most of summer and
winter 97.  The size of Event records changes from readout to readout
of the LP buffers.  The readout is done every 0.6s, so the data size is
comparable from one to the next, but not exactly the same.  The Record
size is a check of the integrity of the data.
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Description of Each Record Type

1.  Configuration Record
Each data file must start with a configuration record.  The
configuration uses 4-byte data words, and it is a direct write of the
DAQ configuration data structure.  The first word in the contents is the
version number of the DAQ, which is equal to 0x00000001, or it is the
creatation data of the DAQ in decimal form, yyyymmdd.

The structure of the configuration record written to file.  This is the first
record in every file.  Note that it contains the map of OM number
to (string, OM) and TDC channel and ADC channel.  Note that the HV channel
mapping is not implemented, nor is the discriminator information maps.  The
discriminators are not CAMAC controllable in the Am-B 97 DAQ so this
information is not useful.  Finally, Pat reports that a few channels
of mapping data in the configuration record in the data files is not accurate.
The accurate map is maintained by Pat, and I list it below the configuration
structure definition.
-------------------------------------------------
#define MAX_STRING 20
#define MAX_OM 720
#define N_DISC 30
#define CHAN_PER_DISC 16

#define INPUT_MAX (256) /* max line length */

#define LABEL_LEN 16
#define MAX_HITS 8 // max number of tdc edges to decode (of each type)

//#define CONFIG_LEN_WORDS (10*N_OM+N_ADC_CHAN+N_TDC_CHAN+N_HV+
2*N_DISC_CHAN+3*LABEL_LEN+3)
#define CONFIG_VER_NO 1
#define CONFIG_EVENT 257

typedef struct configRec        configRec,*configRecPtr;
struct configRec {
```

```
int     VersionNo;               // Version number of configuration file
int     AdcToOm[MAX_OM];         // OM index for this adc channel
int     TdcToOm[MAX_OM];         // OM index for this tdc channel
int     HvToOm[MAX_OM];          // OM index for this HV channel
int     TrigDiscToOm[MAX_OM];    // OM index for this trigger discriminator channel
int     TdcDiscToOm[MAX_OM];     // OM index for this tdc discriminator channel
int     OmToAdc[MAX_OM];         // adc channel for OM index (index = (string-1)*20+(mod-1)
 )
int     OmToTdc[MAX_OM];         // tdc channel for OM index
int     OmToHv[MAX_OM];          // HV value for OM index
int     OmToTrigDisc[MAX_OM];    // trigger discriminator channel for OM index
int     OmToTdcDisc[MAX_OM];     // tdc discriminator channel for OM index
int     adcPed[MAX_OM];          // adc pedestal to program
int     adcLT[MAX_OM];           // adc low threshold for zero suppression
int     tdcDiscOnOff[MAX_OM];    // tdc discriminator mask for this OM (1 = ON)
int     trigDiscOnOff[MAX_OM];   // trig discriminator mask for this OM (1 = ON)
int     highVolt[MAX_OM];        // HV value for this OM
char    intRegLabel[12][LABEL_LEN];// tags for interrupt register bits
int     tdcDiscLevel;            // tdc discriminator level in mV
int     trigDiscLevel;           // trigger discriminator level in mV
int     OMperString[MAX_STRING];// OMs on each string
int     nStrings;                // total number of strings
int     nOM;                     // computed in XcmdInit from above two.
char    instrumentID[4];         // four byte instrument id passed into XcmdInit
};
```

Note that the configuration record requires about 38k of the file. This size is obviously controlled by the Maximum number of OMs and Strings. For 1997, this is fixed, but different from previous years. Again, Pat's Reader takes this into account.

There is a warning. The Mac DAQ writes this data out as a C-structure which may be compiler dependent. Eric Schnieder checked to make sure that the Dec Alphas read the data as it was written by the Mac, but this may change for different computer systems.

Here is the detailed MAP of OMs.

First, some preliminaries: The string and OM are mapped to particular TDC and ADC channels. The ADC can be programmed to zero suppress unless the peak value exceeds a specified value after subtraction by the pedestal. The pedestal can be changed for each channel. Also, the zero suppression threshold in the ADC can be individually programmed, so we have included the ped and ADC threshold in the file so we know how the hardware was programmed. It was envisioned that the configuration data should include the HV map, and discriminator control map. However, it turned out to be more convenient during the summer to control the HV crate via a standalone Mac, and the HV monitoring by the DAQ was not continued. HV problems could be identified quickly by monitoring OM noise rates reported by SNMP scalers.

Note also that the DAQ had no mechanism to handle more than one TDC and ADC channel for a given OM. Obvious, with the hybrids this was a problem because they produce two different sets of TDCs (no pADC was recorded because there was not enough working hardware at pole). So the kluge solution was to display the LE times for the 10 OMs which produce optical signals on another string (String 11). Then you must map the String 11 OMs to physical OMs. Obviously, this approach should be discontinued with the new DAQ and display. Nevertheless, the new DAQ should be capable of displaying TDCs from the optical side, from the electrical side, or both at the same time. In the future, the number of ADC values per OM per trigger may increase as well.

The order of the ADC and TDC channel are determined by the order of the readout of the specfic CAMAC instruments. This was determined by the Mac DAQ readout. For 1997, here is the order of readout, where the number following the ADC and TDC ID is the CAMAC slot. Next to the ADC and TDCs are the header information required to use Appendix A

```
Main Crate 1:                  Main CAMAC Crate 2:
Interrupt_Register IR_hdr      TDC1    TDC3_hdr
TDC1    TDC0_hdr               TDC2    TDC4_hdr
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TDC2    TDC1_hdr               TDC3    TDC5_hdr
TDC3    TDC2_hdr               TDC4    TDC6_dhr
TDC4    TDC8_hdr               TDC5    TDC7_hdr
TDC5    TDC9_hdr               ADC6    ADC6_hdr
TDC16   TDC10_hdr              ADC7    ADC7_hdr
ADC7    ADC0_hdr               ADC8    ADC8_hdr
ADC8    ADC1_hdr               ADC9    ADC9_hdr
ADC9    ADC2_hdr               ADC10   ADC10_hdr
ADC10   ADC3_hdr               ADC11   ADC11_hdr
ADC6    ADC4_hdr               ADC12   ADC12_hdr
ADC11   ADC15_hdr              ADC13   ADC13_hdr
ADC12   ADC16_hdr              ADC14   ADC14_hdr
ADC13   ADC17_hdr
ADC14   ADC18_hdr              ADC15   ADC19_hdr
TTclock TTGPS0_hdr                     TTclock TTGPS1_hdr
Dig_OM1 Misc0_hdr
Dig_OM2 Misc1_hdr

# Number of modules on each string
20 20 20 31 36 36 36 36 36 36 10
# The remaining lines contain the configuration for each OM. The order is
#unimportant, except that later lines supercede data in earlier lines.
# Channels are numbered starting with 0, strings and tubes numbered starting
# with 1. Tube 1 is at the top of a string.

#str    om   tdc_chan adc_chan  ped     thr
1       1       0       0       26      10
1       2       1       1       26      10
1       3       2       2       26      10
1       4       3       3       26      10
1       5       4       4       26      10
1       6       5       5       26      10
1       7       6       6       26      10
1       8       7       7       26      10
1       9       8       8       26      10
1       10      9       9       26      10
1       11      10      10      26      10
1       12      11      11      26      10
1       13      12      12      26      10
1       14      13      13      26      10
1       15      14      14      26      10
1       16      15      15      26      10
1       17      64      16      26      10
1       18      65      17      26      10
1       19      66      18      26      10
1       20      67      19      26      10
#s      om      tdc     adc     ped     thr
2       1       16      20      26      10
2       2       17      21      26      10
2       3       18      22      26      10
2       4       19      23      26      10
2       5       20      24      26      10
2       6       21      25      26      10
2       7       22      26      26      10
2       8       23      27      26      10
2       9       24      28      26      10
2       10      25      29      26      10
2       11      26      30      26      10
2       12      27      31      26      10
2       13      28      32      26      10
2       14      29      33      26      10
2       15      30      34      26      10
2       16      31      35      26      10
2       17      68      36      26      10
2       18      69      37      26      10
2       19      70      38      26      10
2       20      71      39      26      10
#s      om      tdc     adc     ped     thr
3       1       32      40      26      10
3       2       33      41      26      10
3       3       34      42      26      10
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3       4       35      43      26      10
3       5       36      44      26      10
3       6       37      45      26      10
3       7       38      46      26      10
3       8       39      47      26      10
3       9       40      48      26      10
3       10      41      49      26      10
3       11      42      50      26      10
3       12      43      51      26      10
3       13      44      52      26      10
3       14      45      53      26      10
3       15      46      54      26      10
3       16      47      55      26      10
3       17      72      56      26      10
3       18      73      57      26      10
3       19      74      58      26      10
3       20      75      59      26      10
#s      om      tdc     adc     ped     thr
4       1       48      60      26      10
4       2       49      61      26      10
4       3       50      62      26      10
4       4       51      63      26      10
4       5       52      64      26      10
4       6       53      65      26      10
4       7       54      66      26      10
4       8       55      67      26      10
4       9       56      68      26      10
4       10      57      69      26      10
4       11      58      70      26      10
4       12      59      71      26      10
4       13      60      72      26      10
4       14      61      73      26      10
4       15      62      74      26      10
4       16      63      75      26      10
4       17      76      76      26      10
4       18      77      77      26      10
4       19      78      78      26      10
4       20      79      79      26      10
# Next 6 are twisted pair from 95/96 season, not in trig
4       21      80      312     26      10
4       22      81      313     26      10
# Bad LE disc channels 3-4
4       23      83      314     26      10
4       24      84      315     26      10
4       25      85      316     26      10
4       26      86      317     26      10
# What follows are trigger inputs to the TDCs
#       Amanda-A:
4       27      88      86      26      10
#       Amanda-B:
4       28      89      87      26      10
#       Spase 1:
4       29      90      88      26      10
#       Spase 2:
4       30      91      89      26      10
#       Gasp:
4       31      92      90      26      10
#s      om      tdc     adc     ped     thr
5       1       96      96      26      10
5       2       97      97      26      10
5       3       98      98      26      10
5       4       99      99      26      10
5       5       100     100     26      10
5       6       101     101     26      10
5       7       102     102     26      10
5       8       103     103     26      10
5       9       104     104     26      10
5       10      105     105     26      10
5       11      106     106     26      10
5       12      107     107     26      10
5       13      108     108     26      10
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5       14      109     109     26      10
5       15      110     110     26      10
5       16      111     111     26      10
5       17      112     112     26      10
5       18      113     113     26      10
5       19      114     114     26      10
5       20      115     115     26      10
5       21      116     116     26      10
5       22      117     117     26      10
5       23      118     118     26      10
5       24      119     119     26      10
5       25      120     120     26      10
5       26      121     121     26      10
5       27      122     122     26      10
5       28      123     123     26      10
5       29      124     124     26      10
5       30      125     125     26      10
5       31      126     126     26      10
5       32      127     127     26      10
5       33      128     128     26      10
5       34      129     129     26      10
5       35      130     130     26      10
5       36      131     131     26      10
#s      om      tdc     adc     ped     thr
6       1       132     132     26      10
6       2       133     133     26      10
6       3       134     134     26      10
6       4       135     135     26      10
6       5       136     136     26      10
6       6       137     137     26      10
6       7       138     138     26      10
6       8       139     139     26      10
6       9       140     140     26      10
6       10      141     141     26      10
6       11      142     142     26      10
6       12      143     143     26      10
6       13      144     144     26      10
6       14      145     145     26      10
6       15      146     146     26      10
6       16      147     147     26      10
6       17      148     148     26      10
6       18      149     149     26      10
6       19      150     150     26      10
6       20      151     151     26      10
6       21      152     152     26      10
6       22      153     153     26      10
6       23      154     154     26      10
6       24      155     155     26      10
6       25      156     156     26      10
6       26      157     157     26      10
6       27      158     158     26      10
6       28      159     159     26      10
6       29      160     160     26      10
6       30      161     161     26      10
6       31      162     162     26      10
6       32      163     163     26      10
6       33      164     164     26      10
6       34      165     165     26      10
6       35      166     166     26      10
6       36      167     167     26      10
#s      om      tdc     adc     ped     thr
7       1       168     168     26      10
7       2       169     169     26      10
7       3       170     170     26      10
7       4       171     171     26      10
7       5       172     172     26      10
7       6       173     173     26      10
7       7       174     174     26      10
7       8       175     175     26      10
7       9       176     176     26      10
7       10      177     177     26      10
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7	11	178	178	26	10
7	12	179	179	26	10
7	13	180	180	26	10
7	14	181	181	26	10
7	15	182	182	26	10
7	16	183	183	26	10
7	17	184	184	26	10
7	18	185	185	26	10
7	19	186	186	26	10
7	20	187	187	26	10
7	21	188	188	26	10
7	22	189	189	26	10
7	23	190	190	26	10
7	24	191	191	26	10
7	25	192	192	26	10
7	26	193	193	26	10
7	27	194	194	26	10
7	28	195	195	26	10
7	29	196	196	26	10
7	30	197	197	26	10
7	31	198	198	26	10
7	32	199	199	26	10
7	33	200	200	26	10
7	34	201	201	26	10
7	35	202	202	26	10
7	36	203	203	26	10
#s	om	tdc	adc	ped	thr
8	1	208	204	26	10
8	2	209	205	26	10
8	3	210	206	26	10
8	4	211	207	26	10
8	5	212	208	26	10
8	6	213	209	26	10
8	7	214	210	26	10
8	8	215	211	26	10
8	9	216	212	26	10
8	10	217	213	26	10
8	11	218	214	26	10
8	12	219	215	26	10
8	13	220	216	26	10
8	14	221	217	26	10
8	15	222	218	26	10
8	16	223	219	26	10
8	17	224	220	26	10
8	18	225	221	26	10
8	19	226	222	26	10
8	20	227	223	26	10
8	21	228	224	26	10
8	22	229	225	26	10
8	23	230	226	26	10
8	24	231	227	26	10
8	25	232	228	26	10
8	26	233	229	26	10
8	27	234	230	26	10
8	28	235	231	26	10
8	29	236	232	26	10
8	30	237	233	26	10
8	31	238	234	26	10
8	32	239	235	26	10
8	33	240	236	26	10
8	34	241	237	26	10
8	35	242	238	26	10
8	36	243	239	26	10
#s	om	tdc	adc	ped	thr
9	1	244	240	26	10
9	2	245	241	26	10
9	3	246	242	26	10
9	4	247	243	26	10
9	5	248	244	26	10
9	6	249	245	26	10
9	7	250	246	26	10
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9	8	251	247	26	10
9	9	252	248	26	10
9	10	253	249	26	10
9	11	254	250	26	10
9	12	255	251	26	10
9	13	256	252	26	10
9	14	257	253	26	10
9	15	258	254	26	10
9	16	259	255	26	10
9	17	260	256	26	10
9	18	261	257	26	10
9	19	262	258	26	10
9	20	263	259	26	10
9	21	264	260	26	10
9	22	265	261	26	10
9	23	266	262	26	10
9	24	267	263	26	10
9	25	268	264	26	10
9	26	269	265	26	10
9	27	270	266	26	10
9	28	271	267	26	10
9	29	272	268	26	10
9	30	273	269	26	10
9	31	274	270	26	10
9	32	275	271	26	10
9	33	276	272	26	10
9	34	277	273	26	10
9	35	278	274	26	10
9	36	279	275	26	10
#s	om	tdc	adc	ped	thr
10	1	280	276	26	10
10	2	281	277	26	10
10	3	282	278	26	10
10	4	283	279	26	10
10	5	284	280	26	10
10	6	285	281	26	10
10	7	286	282	26	10
10	8	287	283	26	10
10	9	288	284	26	10
10	10	289	285	26	10
10	11	290	286	26	10
10	12	291	287	26	10
10	13	292	288	26	10
10	14	293	289	26	10
10	15	294	290	26	10
10	16	295	291	26	10
10	17	296	292	26	10
10	18	297	293	26	10
10	19	298	294	26	10
10	20	299	295	26	10
10	21	300	296	26	10
10	22	301	297	26	10
10	23	302	298	26	10
10	24	303	299	26	10
10	25	304	300	26	10
10	26	305	301	26	10
10	27	306	302	26	10
10	28	307	303	26	10
10	29	308	304	26	10
10	30	309	305	26	10
10	31	310	306	26	10
10	32	311	307	26	10
10	33	312	308	26	10
10	34	313	308	26	10
10	35	314	310	26	10
10	36	315	311	26	10
#s	om	tdc	adc	ped	thr
# special channels for AOFM, just LE times, no ADC
# so use bogus ADC channel
11	1	320	90	26	10
11	2	321	90	26	10
```

```
11      3       322     90      26      10
11      4       323     90      26      10
11      5       324     90      26      10
11      6       325     90      26      10
11      7       326     90      26      10
11      8       327     90      26      10
11      9       328     90      26      10
11      10      329     90      26      10
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2. Housekeeping Record
The AMANDA-B 1997 raw data does not contain house keeping records.

In previous years, the Housekeeping kept track of trigger rates from various levels of the hardware trigger. There was a mechanism to readout the HV, but it caused problems with the main DAQ readout once the data transfer rates became significant. The most useful information would be a continuous monitoring of the line voltages to the NIM and CAMAC and VME crates, but no hardware was developed for this task. Scaler rates from all OMs could be another piece of information which goes into the Housekeeping, but no mechanism existed. The new DAQ should implement this, if possible. A variety of the CAMAC hardware can be programmed in different ways. This should be monitored and written into the configuration record, or a onetime housekeeping record.

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3. Event Record

After the data from both list processors are readout, the event building is performed. Each readout of the list processors typically includes data from 50 triggers. The first trigger is displayed graphically. All the data is put into appropriate histograms, and saved to disk. The Event Record contains the data from the readout of both list processors.

As previously discussed, the format of the data being written to disk was reformatted to save space. Also, the KMAX/SCSI interface always transfers 32bit words for every LP memory read, packing extra zero bits. The online Mac DAQ program performed data processing to display information in a useful and meaningful way, and simultaneously performed the reformatting.

The contents of the AMANDA-B 1997 Event record are 3-bytes words, which contain fixed length and variable length components, which are separated by delimiters of the form, 0xffffxx (see Appendix A). These 256 delimiters are unique in the AMANDA-B 1997 event data space (see note1). The data following each delimiter is the raw data from the device indicated by the delimiter, with two exceptions. First, the 3377 data has been converted to the 2277 3-byte format, but the order is still the 3377 order. Second, the 7164 data has been compiled into a single block, indicated by the delimiter, "ADC7164". The lower 12-bits are the original ADC value, and the upper 11-bits contain the complete ADC channel number, which is (device_channel_number + (device_number << 4)).

Note 1: AMANDA-B 1997 does not use the Leeds GPS clock, but it is used in AMANDA-A and AMANDA-B 1996. This clock has valid data in the event delimiter space, but it does not conflict with the END_of_Event delimiter, 0xffffff.

Note 2: The GPS clock is read out in each Crate for every event. The times are nearly the same (but not always due to the timing of the latch pulse) to within several counts (0.1us). The information from both clocks are kept in the data stream, even though it is redundant usually.

A typical Event which is written to DISK is given by the following format , where the headers are found in Appendix A. Note that the "header" structure makes the explicit order of the data in the file irrelevent. Pats reader only checks for the header information, and then processes the data according to the header.


```
----------------------------------------------------
Event Format:

EVENT_Record_Delimiter  (4 bytes) ! Inserted by software
REcord Size             (4 bytes) ! Inserted by software, Addition of both LPs
                                  ! Plus the software added bytes (Typical 30k,
                                  ! max=64k)
EVTNO_hdr               (3 bytes) ! These 3 + next 6 bytes are added by DAQ
        Evnt_number     (6 bytes) ! software.  Increments over run (typ. 24 hr)
                                  !     byte    definition
                                        1       zero
                                        2       zero
                                        3       most significant byte
                                        4       2nd byte
                                        5       3rd byte
                                        6       least significant byte

IR_hdr                  (3 bytes)
        IR_data         (3 bytes) ! Interrupt Register data
TDC0_hdr                (3 bytes)
        TDC_data        (3 bytes)       Bits    Definition
                                        1-16    edge time
                                        17      edge type (LE or TE)
                                        18-22   Channel ID
(Note:  The first word readout from the 3377 TDC by the LP is called the
Header word. It should not be confused with the headers supplied by the
LP hardware.  The header information from the 3377 is not useful, and
deleted from the data stream written to DISK.  Also, the hardware readout
of each edge in a given channel involves 2 separate CAMAC read operations
to achieve maximum dynamic range.  This data is combined in the
MAC DAQ into a single 24 bit word, nearly identical to the 2277 TDC data format.

TDC1_hdr                (3 bytes)

... repeat for all 10 TDCs...
TDC10_hdr               (3 bytes)

ADC7164                 (3 bytes)
...
All ADC channels for a given trigger, but different format from direct
hardware format that was readout by LP.  Hardware readout format is memory
inefficient.  P. Mock has transformation between hardware and software format.
The basic structure of the written format:
                                                Bits    Definition
                                                1-12    ADC peak info
                                                13-23   channel info
...

TTGPS0_hdr              (3 bytes)  ! See Art Webbs write-up on bit definition
        GPS_crate1      (9 bytes)
TTGPS1_hdr              (3 bytes)
        GPS_crate2      (9 bytes)
Misc0_hdr               (3 bytes)
        Dig OM ID       (3 bytes)
Misc1_hdr               (3 bytes)
        Dig OM2 ID      (3 bytes)
END_HDR                 (3 bytes)  !included in the data stream
...
Repeat for all trigger events in combined LP buffer (typically 50 triggers)
...
End_of_Record           (4 bytes)   ! note this is inserted by software
```

```
Appendix A
----------
END_HDR         0x00ffffff      /* End of this event. */
TDC0_HDR        0x00fffffe      /* 3377 TDCs */
TDC1_HDR        0x00fffffd
TDC2_HDR        0x00fffffc
TDC3_HDR        0x00fffffb
```

```
ADC0_HDR        0x00fffffa      /* 7164 ADCs */
ADC1_HDR        0x00fffff9
ADC2_HDR        0x00fffff8
ADC3_HDR        0x00fffff7
ADC4_HDR        0x00fffff6
ADC5_HDR        0x00fffff5
ADC6_HDR        0x00fffff4
ADC7_HDR        0x00fffff3
CLK_HDR         0x00fffff2      /* Real time clock? */
IR_HDR          0x00fffff1      /* Interrupt register */
ATDC0_HDR       0x00fffff0      /* 2277 TDCs (alternate hardware) */
ATDC1_HDR       0x00ffffef      /* 2277 TDCs are oonly used in Am-A*/
ATDC2_HDR       0x00ffffee
ATDC3_HDR       0x00ffffed
EVTNO_HDR       0x00ffffeb      /* software-inserted event number, increments
                                over files within same run */
FADC0_HDR       0X00ffffea      /* 4300B FERA ADC */ used in Am-A only
FADC1_HDR       0X00ffffe9      /* 4300B FERA ADC */ used in Am-A only
FADC2_HDR       0X00ffffe8      /* 4300B FERA ADC */ used in Am-A only
FADC3_HDR       0X00ffffe7      /* 4300B FERA ADC */ used in Am-A only
FADC4_HDR       0X00ffffe6      /* 4300B FERA ADC */ used in Am-A only
```

```
The next 4 headers are not used in 1997.  They were used in previous
years to put prgramming information into the housekeeping records.
The configuration information indicated the specific programmed
operation of the TDC, ADC, FERA and 2277TDC.

TDC_CONFIG_HDR  0X00ffffe5      /* 3377 TDC Configuration */
ATDC_CONFIG_HDR 0X00ffffe4      /* 2277 TDC Configuration */
ADC_CONFIG_HDR  0X00ffffe3      /* Phillips 7164 Peak ADC config */
FERA_CONFIG_HDR 0X00ffffe2      /* 4300B FERA Configuration */
```

```
SC_2551_HDR     0X00ffffe1      /* 2551 Scaler header  */
TDC4_HDR        0x00ffffdf      /* more 3377's */
TDC5_HDR        0x00ffffde
TDC6_HDR        0x00ffffdd
TDC7_HDR        0x00ffffdc
TDC8_HDR        0x00ffffdb
TDC9_HDR        0x00ffffda
TDC10_HDR       0x00ffffd9
TDC11_HDR       0x00ffffd8
TDC12_HDR       0x00ffffd7
TDC13_HDR       0x00ffffd6
TDC14_HDR       0x00ffffd5
TDC15_HDR       0x00ffffd4
TDC16_HDR       0x00ffffd3
TDC17_HDR       0x00ffffd2
TDC18_HDR       0x00ffffd1
TDC19_HDR       0x00ffffd0
ATDC4_HDR       0x00ffffbf      /* more 2277's */
ATDC5_HDR       0x00ffffbe
ATDC6_HDR       0x00ffffbd
ATDC7_HDR       0x00ffffbc
ATDC8_HDR       0x00ffffbb
ATDC9_HDR       0x00ffffba
ATDC10_HDR      0x00ffffb9
ATDC11_HDR      0x00ffffb8
ATDC12_HDR      0x00ffffb7
ATDC13_HDR      0x00ffffb6
ATDC14_HDR      0x00ffffb5
ATDC15_HDR      0x00ffffb4
ATDC16_HDR      0x00ffffb3
ATDC17_HDR      0x00ffffb2
ATDC18_HDR      0x00ffffb1
ATDC19_HDR      0x00ffffb0
ADC8_HDR        0x00ffff9f      /* MORE 7164 ADCs */
ADC9_HDR        0x00ffff9e
ADC10_HDR       0x00ffff9d
ADC11_HDR       0x00ffff9c
ADC12_HDR       0x00ffff9b
ADC13_HDR       0x00ffff9a
```



```
ADC14_HDR       0x00ffff99
ADC15_HDR       0x00ffff98
ADC16_HDR       0x00ffff97
ADC17_HDR       0x00ffff96
ADC18_HDR       0x00ffff95
ADC19_HDR       0x00ffff94
ADC20_HDR       0x00ffff93
ADC21_HDR       0x00ffff92
ADC22_HDR       0x00ffff91
ADC23_HDR       0x00ffff90
TTGPS0_HDR      0x00ffff7f
TTGPS1_HDR      0x00ffff7e
DIGOM_HDR       0x00ffff60      /* Not used in 97 */
MISC0_HDR       0x00ffff40      /* Dig OM 1*/
MISC1_HDR       0x00ffff3f      /* Dig OM 2*/
ADC7164         0x00ffff20      /* header for new ADC7164 format */
SAVEFLAG_HDR    0x00ffff10      /* next word indicates why the event
                                  was extracted. This word is added
                                 by the extraction software.  P. Mock
                                has the definition of this flag */
LO_HDR          0x00ffff00      /* need to put a limit on number of headers. */
```