Technical Information Manual

Revision n. 2

1 June 1999

MOD. V767/V767B

128 CH.
GENERAL PURPOSE
MULTIHIT TDC

NPO:
00001/97:V767x.MUTx/02

2. SPECIFICATIONS

2.1. PACKAGING

1-unit wide VME unit. Height: 6U.

2.2. EXTERNAL COMPONENTS

(refer to fig. 2.1)

CONNECTORS
(refer to fig. 2.2 and fig. 2.3)

- N. 4, "INPUT A, B, C, D", Input connectors, Robinson Nugent P50E-068-P1-SR1-TG type, (34+34) pins; for the 128 single channel inputs.
Connector A refers to Channels 0 to 31.
Connector B refers to Channels 32 to 63.
Connector C refers to Channels 64 to 95.
Connector D refers to Channels 96 to 127.

- N. 1, “CONTROL”, input connector, Header 3M type, 8+8 pins, for the common control signals.

DISPLAYS

- N. 1, "DTACK", green LED, VME Selected. It lights up during a VME access.

- N. 1, "DATA READY", yellow LED. It lights up in occurrence of a Local/Global Data Ready.

- N. 1, "BUSY", red LED. It lights up in occurrence of a Local/Global BUSY.

- N. 1, "TERM ON", red LED. It lights up when the Control BUS has the termination ON.

- N. 1, "TERM OFF", red LED. It lights up when the Control BUS has the termination OFF.

2.3. INTERNAL COMPONENTS

(refer to fig. 2.4)

SWITCHES

- N. 4, rotary switches for the module's VME Base Address selection.

- N. 12, DIP switches for the Control Bus 110 Ohm terminations.

JUMPERS

- N. 1, "SRCCLK" for the External/Internal CLOCK selection.

- N. 5, JP2-JP6, for CAEN Internal Use only.

2.4. CHARACTERISTICS OF THE SIGNALS

- INPUT CHANNELS, START(1): Differential ECL level, 110 Ω impedance; min. width 10 ns.
- CLOCK(1): Differential ECL level, 110 Ω impedance; min. width 25 ns.
- TRIGGER(1): Rising-edge active, differential ECL level, 110 Ω impedance; min. width 25 ns.
- BUSY(1), DRDY(1): Active high, differential ECL level, 110 Ω impedance; min. width 25 ns.
- RESET(1): Active low, differential ECL level, 110 Ω impedance; min. width 25 ns.

(1) These signals are provided with DIP-switch insertable 110 Ω terminations, in order to connect more V767 modules in a daisy chain mode. The 110 Ω terminations must be inserted on the lines of the last module of the chain. All inputs are connected in a way that if the input connector is not inserted they are forced to a 0 logical level.

2.5. GENERAL

TDC CHIP SPECIFICATIONS

PARAMETER	***LO_RES***	***TYP***	**HI_RES**
NUMBER OF CHANNELS	128 + 1		
RESOLUTION (bin size)	1.6 ns	0.8 ns	0.5 ns
DYNAMIC RANGE	20 bit		
	1.6 ms	0.8 ms	0.5 ms
DOUBLE HIT RESOLUTION	10 ns		
MEDIUM RATE (per channel, all channels simultaneous)	approx. 1 MHz		
DIFFERENTIAL NON LINEARITY	absolute timing: < 15 %		
	relative timing: < 1.5 %		
INTEGRAL NON LINERITY	0.3 ns		
STANDARD DEVIATION (estimated)	0.6		

VME BOARD SPECIFICATIONS

LOCAL BUFFER	FIFO 32K (TDC to FIFO tranf. rate = 20 MHz)
TESTABILITY	data path and memory test (from VME)
CONTROL BUS TERMINATION	ON/OFF by dip-switch
CLOCK SOURCE	Internal (40 MHz) / External
TRIGGER WINDOW	software setting (from 1 clock cycle to full dynamic range)
ACQUISITION MODES	start or stop trigger matching, start gating, continuous storage
DATA READOUT	TRG MATCH or START GATING: sequential event RO CONTINOUS STORAGE: sequential data stream RO
VME READ OUT RATE	about 10 MHz
MAXIMUM EVENT SIZE	not defined

2.6. POWER REQUIREMENTS

Mod. V767		**Mod. V767B**	
+ 5 V	2.3 A	+ 5 V	3.5 A
– 5 V	1.5 A	-	-

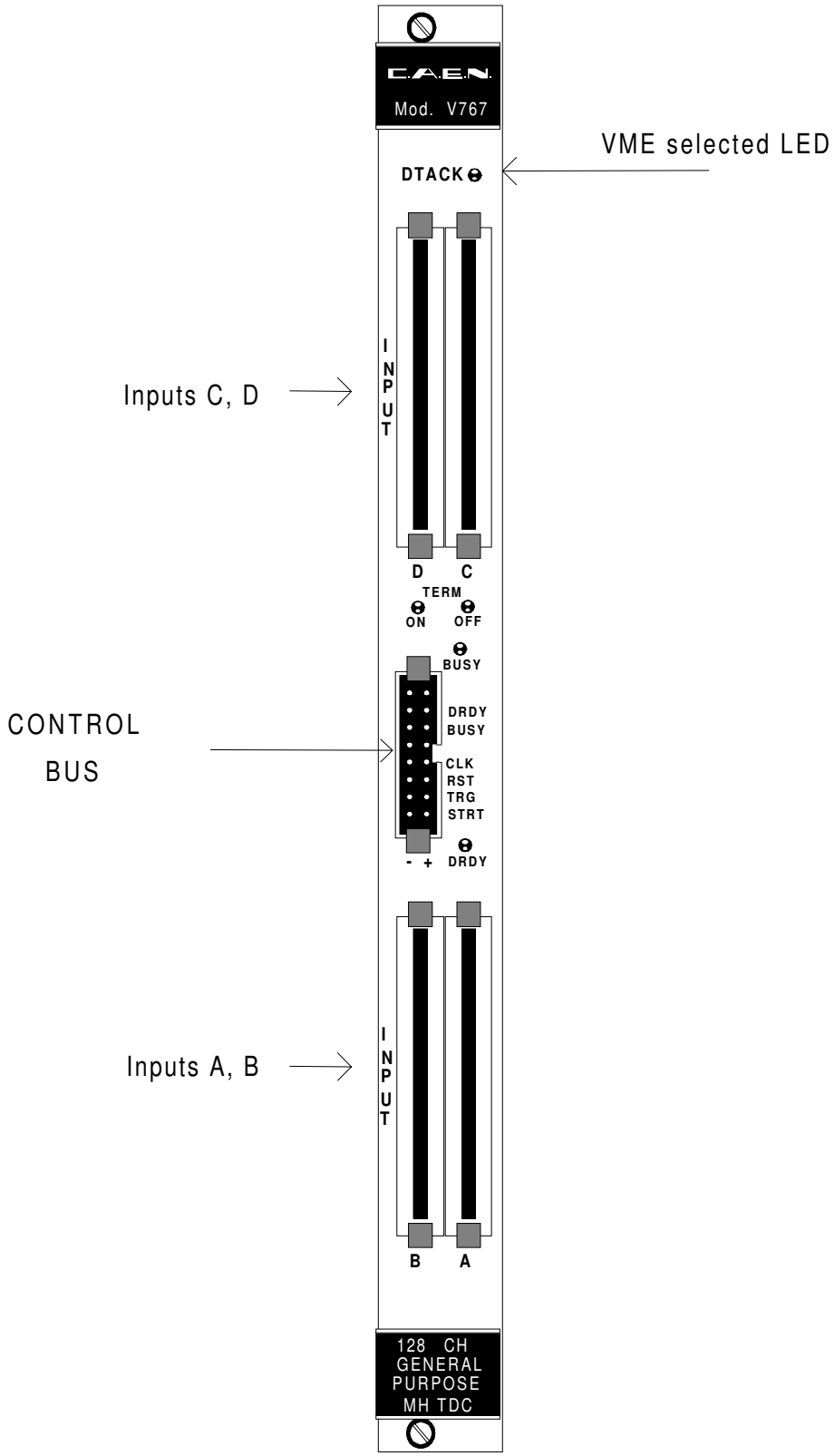


Fig. 2.1: Mod. V767 Front Panel

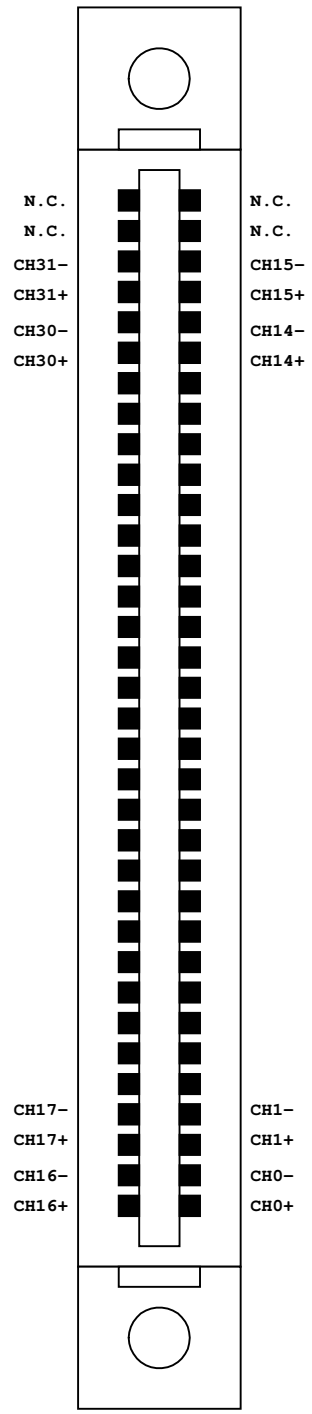


Fig. 2.2: INPUT connector pin assignment

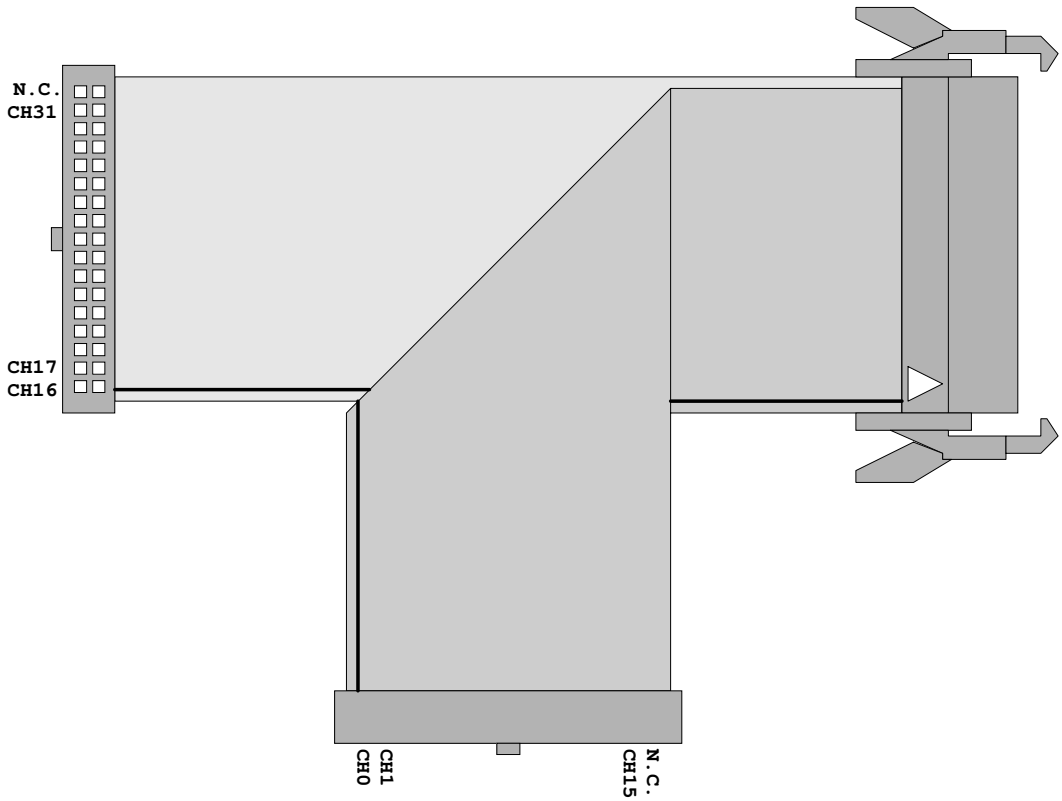
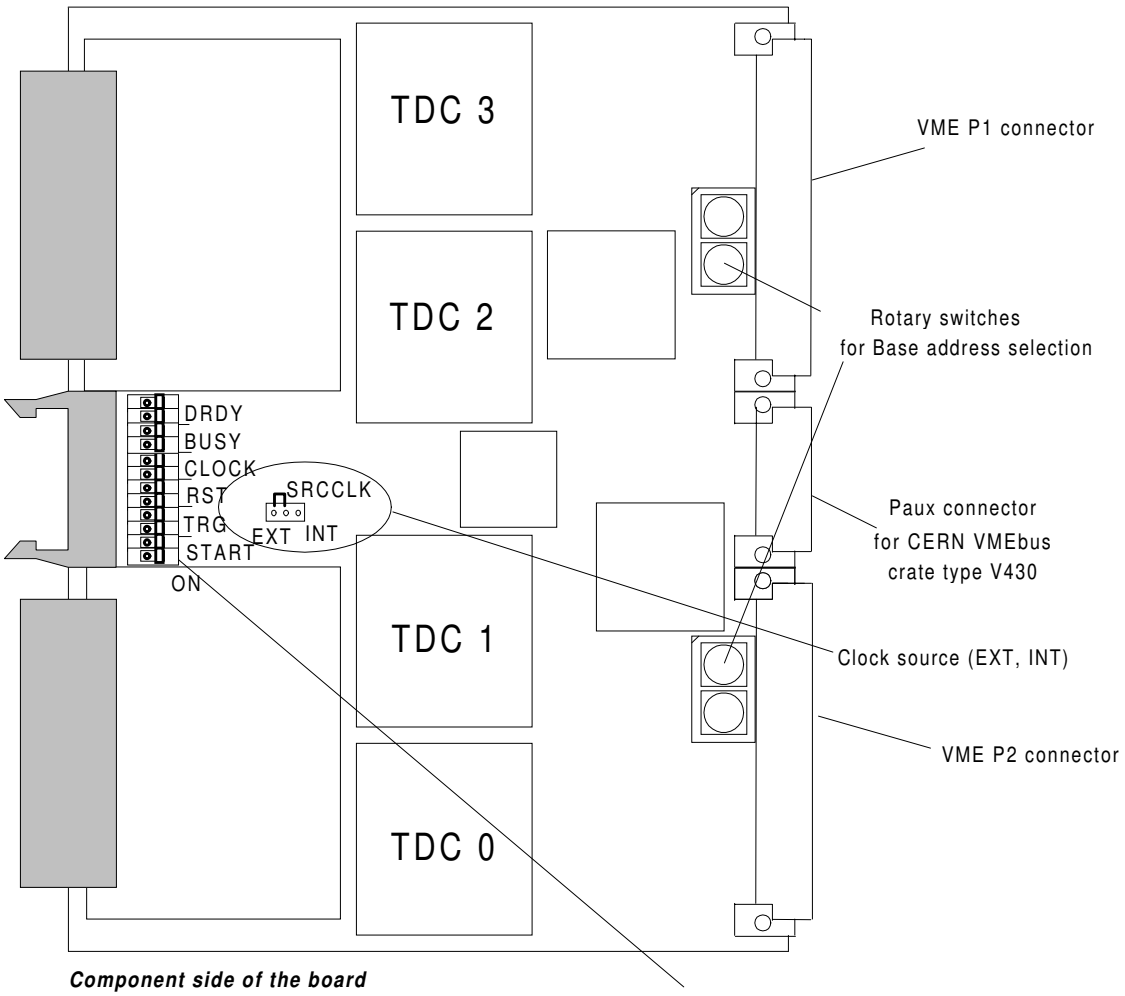


Fig. 2.3: INPUT connector cabling



DIP Switches which allow to insert the 110 Ω terminations: for each signal there are two DIP switches which must be inserted both in oder to insert the 110 Ω termination on the relevant line.

Fig. 2.4: Mod. V767 Components Locations