GRS2   GPS Repeater/Scaler

The GRS2 interface unit is designed to operate in conjunction with the True Time XL-DC GPS receiver, and interface with a CAMAC crate. The unit supplies major time (days:hours:mins:secs) in a BCD form, along with status bits, and a minor time in binary units of 100 nanoseconds.

The major time (day:hrs:min:sec) is set through the RS232 interface with the XL-DC. The minor time is kept by a scaler that is clocked by the 10MHz input signal from the XL-DC, or any timebase generator. This scaler is cleared, and the major time is incremented, by the incoming 1PPS signal also supplied from the XL-DC. The major and minor times are latched by leading edge of the Interrupt Request (IRQ) signal. This time remains latched until the GRS2 A(2) register is read with a F(2) command.

Time Registers

The time registers are arranged in the following manner and can be read by a standard CAMAC F(0) or F(2) read.
Register A(0) - Minor time (Binary)
Register A(1) - Low Major Time word (hours:mins:secs) (BCD)
Register A(2) - High Major Time word (year:days) and status information (BCD)

All registers are fully CAMAC compliant and respond with the standard Q signal. Data in all registers is latched by the leading edge of an IRQ signal and is ready to read within 1 microsecond of that Event signal. The latching is cleared by a read of register A(2), i.e. F(2)A(2), and the unit is ready to accept another Event within 2 microseconds of that clearing action.

**** WARNING ****
THIS UNIT IS DEPENDENT ON SIGNALS RECEIVED FROM THE GPS CLOCK. THEREFORE THE TIME IN ALL THREE REGISTERS SHOULD BE CONSIDERED INVALID IF ANY BIT IN THE STATUS BYTE IS LOW.

Register A(0) Minor Time: The minor time is a binary number that represents the number of clock cycles since the last 1PPS input pulse. For the standard 10MHz. input a clock cycle would be 100 nanoseconds. This number should range from 0 to 10,000,000 base 10, or 000000 to 989680 in base 16 (HEX).

**** NOTICE ****
Any number larger than 8388607 in A(0), or 838,860.7 microseconds, will cause the most significant digit to be set. On some systems this can cause a negative number to be generated.

Register A(1) Low Major Time: The low major time register holds the hours, minutes, and seconds, MSByte to LSByte respectively, for the current time. A sample time output would be as follows

```
MSBit                          LSBit
0010  0011   0100  0111   0101 1001     (234759 Hex)   represents    23 hours  47 minutes  and 59 seconds
  Hours        Minutes        Seconds
```

Register A(2) High Major Time & Status: This word holds the two digit year, the days of the current time, the status of the GPS receiver signals, and the GPS Time Quality Character. A sample output would be as follows

```
MSBit                          LSBit
0000  1111   0000  0010   0110 1000     (0F0268 Hex)   represents    Good Status and  268 days
TQ/S  Y10     Y1   D100   D10   D1    Where;
```

TQ/S is a combination of Time Quality Character and system Status Byte (See Below)
Y10 and Y1 are the Year X10, and Year X1, respectively for the current date.
D100, D10, and D1 are the Days X100, Days X10, and Days X1, respectively for the current time.

**** NOTE ****
For a discussion of Time Quality Characters see page 3-48 of the XL-DC Manual.

Time Quality/Status Byte (TQ/S)

TQ/S is a combination of the Time Quality Character (TQC) as received from the GPS receiver and a status byte showing the status of the GRS2 repeater card. The most significant bit is a general status bit that informs the user as to whether the GRS2 is receiving all the nesessary signals from the GPS receiver, and controls the contents of the 3 lower bits. If the unit is receiving the 1PPS, 10mhz., and RS-232 signals the most significant bit will be high and the lower three bits will correspond to the TQC from the GPS receiver as shown below.

TQ/S when most significant bit is HIGH, status is GOOD:

TQC	MSBit	Bit 3	Bit 2	Bit 1 (LSBit)
1 (best)	1	0	0	1
2	1	0	1	0
3	1	0	1	1
4	1	1	0	0
5(worst)	1	1	0	1

When an input fails the most significant bit will go low informing the user of a problem, and the lower 3 bits will become status bits for the input signals as shown below.

TQ/S when most significant bit is LOW, status is BAD:

Bit 4 (MSBit)	General Status Bit : LOW informing user of a bad input
Bit 3	TIME Bit : is high if RS-232 information received has been valid and incrementing.
Bit 2	10MHz. Bit : is high if 10MHz has been steady.
Bit 1 (LSBit)	1PPS Bit: is high if 1PPS signal has been present.

**** NOTE ****

All status bits require that the monitored input be valid for 3 seconds in a row before the status bit is set to a high state.

Internal Time Register: The GPS Repeater unit has an internal time register (ITR) which keeps the time that is presented to the CAMAC bus. The ITR is incremented by the controller at the detection of the 1PPS signal. When the incoming RS-232 time information arrives two comparisons are made. First the current time signal is compared to the last time received to see that it has incremented by one second. If the comparison is good a counter is incremented, if not it is cleared. When this counter reaches 3, meaning that the incoming RS-232 time has been incrementing correctly for 3 seconds, the GPS Status Bit is set. Anytime this counter is less then 3 the GPS Status Bit is cleared. Next the current time signal is checked with the ITR to see if they match. Again, if the comparison is good a counter is incremented and the same process takes place with the TIME Status Bit. If the comparison is bad the unit transfers the current RS-232 time into the ITR if the GPS Status Bit is high.

This means that if the time signal changes the GPS Repeater will not show the new time for at least 3 seconds. This occurs most often when setting up the TrueTime GPS Clock. When first powered up the XL-DC will transmit 000:00:00:01 and increment that time until it acquires the actual time, which can take several minutes. During this time the Repeater will accept the time as the true time and load it into the ITR. At some point the XL-DC will acquire the correct time and start transmitting it. The Repeater will Not Trust the new time until it has been stable for 3 seconds, at which time it will load the new time and present it to CAMAC.

Although this procedure allows the Repeater to receive bogus signals that occasionally happen due to a noisy environment, loose or frayed cables, or any other problems in the line**, the time CAN NOT be guaranteed ANYTIME Status Byte 1 has any low bits**. In practice the RS-232 cable can be disconnected and the unit should continue to keep the correct time once it has been properly set, and as long as the 1PPS signal is present. However, because the internal timebase cannot determine exact times this practice is not recommended as any disruption of the 1PPS will cause the ITR to become completely unreliable.

**** WARNING ****

THIS UNIT IS DEPENDENT ON RS-232 SIGNALS RECEIVED FROM THE XL-DC GPS CLOCK. THIS REQUIRES THAT THE XL-DC BE SET-UP FOR THE PROPER

COMMUNICATION PROTOCOLS. PLEASE SEE THE FOLLOWING PAGE FOR INSTRUCTIONS.

Unit Timing Precautions

The GRS2 has 2 microsecond set-up times and a throughput of over 100KHz. While this speed allows the user flexibility in operation it can also cause erroneous errors in system timing. For example the time required from an F(2)*A(2), which clears the IRQ line, until the next IRQ is allowed to latch the unit is less than 2 microseconds. When another IRQ pulse appears after this set-up time the GRS2 will latch that time until the next F(2)*A(2) from CAMAC. If this new IRQ arrives before the system is ready to accept it the time in the GRS2 registers will contain that IRQ time when next read. For this reason the GRS2 should not be read until the system is ready to accept another IRQ, or a system IRQ holdoff should be employed to assure that no further IRQ pulses are applied to the GRS2 until the system is ready.

GRS2 Specifications

INPUTS

Power : **+6 Volts @ 200mA** (from CAMAC crate)
-6 Volts @ 50mA (from CAMAC crate)

1 PPS : **TTL -** Vmin = 2.5v Width = 1 uS. Impedance = 1K ohms Edge = Rising

10 MHz. : **TTL -** Vmin = 2.5v Duty Cycle = 40 - 60 % Impedance = 1K ohms
SineWave - Vmin = .75vRMS Impedance = 1K ohms

IRQ : **TTL -** Vmin = 2.5v Width = 1 uS. Impedance = 1K ohms Edge = Rising
NIM - Vmin = -.3v Width = 10 nS. Impedance = 50 ohms Edge = Falling

RS-232 : **9600 baud, 8 data bits, no parity, and 1 stop bit**
Receiver Input Low Threshold 0.8v min. 1.2v typ.
Receiver Input High Threshold 1.7v typ. 2.4v max.
Transmitter Output (3K load) +/- 5v min. +/- 9v typ.
Transmitter Short Circuit Output +/- 10 mA. typ.
DCE Standard DB9 pinout

GRS2 (DCE) DB9 - Pin	RS232 Signal	XL-DC (DTE) DB9 - Pin
5 (GND)	GROUND	5 (GND)
3 (Rx)	TRANSMIT	3 (Tx)
2 (Tx)	RECEIVE	2 (Rx)

Set Up Times

IRQ to F(0,2) : 1 microsecond

F(2)A(2) to IRQ : 2 microsecond

CAMAC Interface

X : **Follows N**

Q : **Asserts on F(0)A(0,1,2) or F(2)A(0,1,2)**

LAM : **Currently no conditions cause the LAM to assert**

TrueTime XL-DC Set-Up

The XL-DC GPS Clock must be set to the proper RS-232 mode in order for the Repeater/Scaler unit to accept the time inputs. The GRS2 requires setting of **9600 baud, 8 data bits, no parity, and 1 stop bit**. These settings are **NOT** the default setting for the XL-DC and must be made at the front panel keypad. The instructions for these setting appear on page 3-13 of the XL-DC manual, and a summary follows.

1) Press FUNC/ENTR then 0 4 The display should read
Ser port Setup
Baud rate 9600

IF NOT 9600 Press the up or down arrows to select 9600 baud.

2) Press FUNC/ENTR The display should read
Ser port Setup
Data Bits 8

IF NOT 8 Press the up or down arrows to select 8 data bits.

3) Press FUNC/ENTR The display should read
Ser port Setup
Parity none

IF NOT none Press the up or down arrows to select none for parity.

4) Press FUNC/ENTR The display should read
Ser port Setup
Stop bits 1

IF NOT 1 Press the up or down arrows to select 1 stop bit.

4) Press FUNC/ENTR
The XL-DC should now be properly set-up for **9600 Baud, 8 data bits, no parity, and 1 stop bit**.

GRS2 Frequently Asked Questions

Q. Im strobing the GRS2 IRQ line more times then I read it but the clock times are unreliable, whats wrong?

A. When you pulse the IRQ line of the GRS2 it freezes the current clock time into the output registers. The output registers are not released until a F(2)A(2) read of the GRS2. Therefore the time you are reading is the time of the first strobe after a read, not the lastest strobe time.

Q. Why do I get negative numbers in the minor time on some reads and not others when I read the clock?

A. The minor time output register (A0) is a binary number between 0 and 10,000,000 base ten, or 0 and 989680 base sixteen (HEX). Any number larger than 8388607 in A(0), or 838,860.7 microseconds, will cause the most significant digit to be set. On some systems this can cause a negative number to be generated.

Q. Why do I get a negative number in the A2 register on some reads and not others when I read the clock?

A. The most significant digit of the A2 register is a staus bit which will normally be high informing the user that all inputs are good. On some systems this can cause a negative number to be generated, however if an error occurs this most significant bit will go low and the binary number will be positive on those systems.