mini_Fieldhub – Communication Modules Register Map

Rev. 0.2

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Firmware Rev. xxx or later

Change History

Revision	changed
0.2	several typos fixed, TERM_ENA introduced -> see ICM_CTRL1 and ICM_STAT reg.,

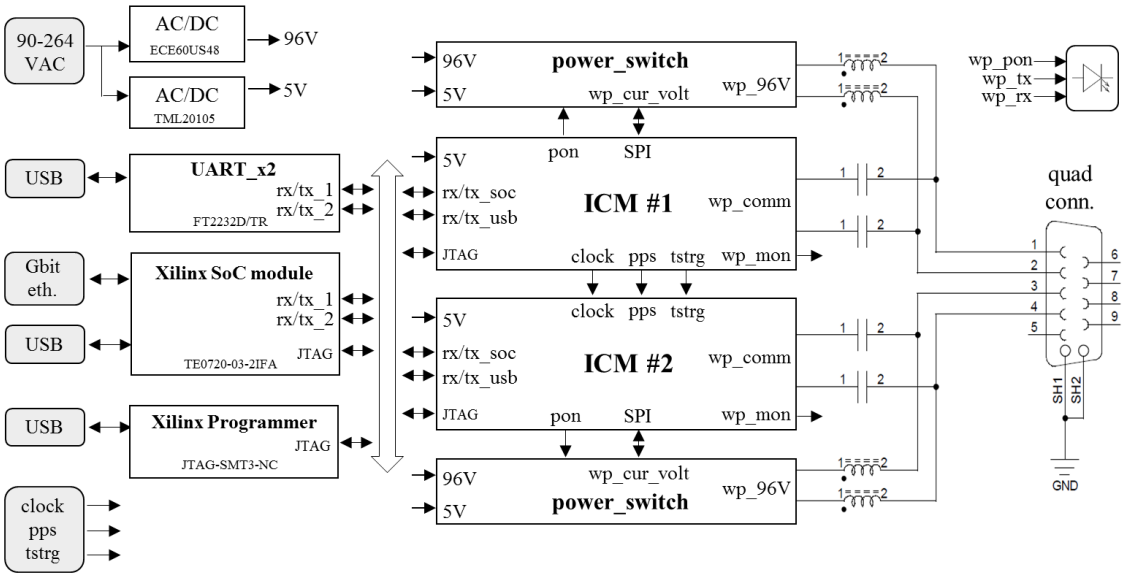
Used Abbreviations

abbreviation	meaning
API	Application Program Interface
FH	Field Hub
ICM	IceCube Communication Module
IRIGB	Inter-Range Instrumentation Group time code format B (typically provided by GPS systems)
JTAG	Joint Test Action Group
PCA	Printed Circuit Assembly
SoC	System on Chip (e.g. ARM core within the FPGA)
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver Transmitter

Introduction

This document is a first trial to describe the mini_Fieldhub - API. It should be seen as a basis of discussion. Comments and proposals are welcome.
There are two basic ways to communicate with inice modules through the mini_Fieldhub. Firstly using the SoC module, its ethernet or USB connection and some Linux based software, talking via UART channels to the two ICMs.
Secondly, providing two serial terminal channels to the user, to talk directly to the ICMs via a dedicated USB port.
Presently, the description is focussing on the second method. A Communications Modules (ICM for the mini_Fieldhub) register map will be described here.
To avoid confusion, the ICMs being plugged to the mini_Fieldhub are referred to as “communication modules” within this document.
The real fieldhub will be equipped with one communication module per wire pair. From the hardware point of view, these modules are very similar to the ICM. The main differences is the absence of the DC/DC converter, the local oscillator and the USB to UART interface.

mini_Fieldhub, Block Diagram



UART

The UART channels run at 3Mbd, with 1 start, 8 data, 1 stop bit, LSB first.
The UART protocol follows the definition by Tyler Anderson, see below.

Notes: CRC16 has checksum 0x8005, polynomial = x^16 + x^15 + x^2 + 1

Single Write

TX/RX	TX									
Subpacket Component	Header Word (0x8fc7)		Single Write (0x0001)		Address		DATA		CRC16 (Bytes 4-9)	
Byte in Packet	0	1	2	3	4	5	6	7	8	9
Bits in Subpacket	[31:24]	[23:16]	[15:8]	[7:0]	[11:8]	[7:0]	[15:8]	[7:0]	[15:8]	[7:0]
Hex Value	8f	c7	00	01	0x	xx	xx	xx	xx	xx

Single Read

TX/RX	TX						RX			
Subpacket Component	Header Word (0x8fc7)		Single Read (0x0002)		Address		DATA		CRC16 (Bytes 4-9)	
Byte in Packet	0	1	2	3	4	5	6	7	8	9
Bits in Subpacket	[31:24]	[23:16]	[15:8]	[7:0]	[11:8]	[7:0]	[15:8]	[7:0]	[15:8]	[7:0]
Hex Value	8f	c7	0	2	0x	xx	xx	xx	xx	xx

Burst Write

TX/RX	TX															
Subpacket Component	Header Word (0x8fc7)		Burst Write (0x8001)		Length (max N=2048)		Address		DATA[0]		...	DATA[N-1]		CRC16 (Bytes 6-2N+13)	
Byte in Packet	0	1	2	3	4	5	6	7	8	9	...	2N+8	2N+9	2N+10	2N+11
Bits in Subpacket	[31:24]	[23:16]	[15:8]	[7:0]	[11:8]	[7:0]	[15:8]	[7:0]	[15:8]	[7:0]	...	[15:8]	[7:0]	[15:8]	[7:0]
Hex Value	8f	c7	80	01	0x	xx	xx	xx	xx	xx	..	xx	xx	xx	xx

Burst Read

TX/RX	TX								RX							
Subpacket Component	Header Word (0x8fc7)		Burst Write (0x8002)		Length (max N=2048)		Address		DATA[0]		...	DATA[N-1]		CRC16 (Bytes 6-2N+13)	
Byte in Packet	0	1	2	3	4	5	6	7	8	9	...	2N+8	2N+9	2N+10	2N+11
Bits in Subpacket	[31:24]	[23:16]	[15:8]	[7:0]	[11:8]	[7:0]	[15:8]	[7:0]	[15:8]	[7:0]	...	[15:8]	[7:0]	[15:8]	[7:0]
Hex Value	8f	c7	80	02	0x	xx	xx	xx	xx	xx	..	xx	xx	xx	xx

Address Schema

The register and buffer ports are 16 bit wide. There are two types of register maps. One is dedicated to the Fieldhub control and monitoring, the other belongs to the communication with the ICMs, plugged to the inice modules.

Offset range (hex)	Name
00..FF	**Field Hub Control**
100..1FF	**ICM_0**
200..2FF	**ICM_1**
300..3FF	**ICM_2**
400..4FF	**ICM_3**

Data Transfer between the Communication Modules and the SoC or USB Ports

As a first approach, the data transfer could be initiated by the SoC or via the USB-connected device. The software has to poll an buffer status flags before initiating a data transfer. This model is based an a master / slave relationship, with the communication modules being the slaves.
Other, more efficient schemas can be implemented, with data transfers initiated by the communication modules, possibly also, using interrupts.

Fieldhub Control & Status Register, Address Map

Access: 16bit

Offset (hex)	Name	Description
00	**FH_CTRL**	Communication Module Control Reg.
01	**FH_GSTAT**	Communication Module Global Status Reg.
02	**FH_PSTAT**	Communication Module Power Status Reg.
03	**FH_CUR**	Communication Module Wire Pair Current
04	**FH_VOLT**	Communication Module Wire Pair Voltage
05	**FH_CURL**	Communication Module Wire Pair Current Limits
06	**FH_VOLTL**	Communication Module Wire Pair Voltage Limits
07	**FH_TIME**	Timer bit_47..0, system clock ticks (25ns)
08	**FH_TSTRG**	Time String buffer, e.g. IRIGB format
09	**FH_FLADR**	FPGA Flash, Start Address bits 31..0
0A	**FH_FLBUF**	FPGA Flash Data Buffer
...		
FE	**FH_ID**	Communication Module, 64 bit ID
FF	**FH_FREV**	Firmware Revision

xDOM access, ICM Control & Status Registers, Address Map

Access: 16 bit

Offset (hex)	Name	Description
x00	**ICM_CTRL1**	ICM Control Reg. #1
x01	**ICM_CTRL2**	ICM Control Reg. #2
x02	**ICM_STAT**	ICM Status Reg.
x03	**ICM_CERR**	Communication error counter, 16bit
x04	**ICM_TXBUF**	Tx data buffer
x05	**ICM_WRCVD**	ICM_RXBUF, amount of words
x06	**ICM_RXBUF**	Rx data buffer
x07	**ICM_TCBUF**	TCAL data buffer
x08	**ICM_TRBUF**	Trigger time stamp buffer
x09	**ICM_FLADR**	FPGA Flash, Start Address bits 31..0
x0A	**ICM_FLBUF**	FPGA Flash Data Buffer
...		
xFD	**ICM_ID**	ICM ID buffer
xFE	**ICM_PCA_ID**	PCA (main board) ID buffer
xFF	**ICM_FREV**	ICM Firmware Revision

x= 1..4, corresponds to xDOM_0..3 (A..D)

Fieldhub Control & Status Register – Detailed Description

RW Read / Write
RWC Read / Write-Clear, writing a 1 clears the status bit
RO Read Only
WO Write Only
RWSC Read / Write / Self Clear, gets 0 when ready (poll function)

FH_CTRL @ 00h Communication Module Control register power on state: **0000h**

Bit	Signal	Attribute	Description
0	WP_PON	RW	Wire pair power on/off bit, poll on WP_PON_RDY (DSTAT) to get the status,
1	x	RW	Unused
2	x	RW	Unused
3	x	RW	Unused
4	x	RW	Unused
5	x	RW	Unused
6	x	RW	Unused
7	x	RW	Unused
8	TIMER_CLEAR	RWSC	The 0-1 transition clears the 48 bit timer
9	TIMER_SNAP	RWSC	The 0-1 transition cause a snapshot of the 48 bit ICM timer, The value can be read from TIME buffer.
10	x	RW	Unused
11	x	RW	Unused
12	x	RW	Unused
13	FPGA_IMAGE_0	RW	FPGA firmware version (FLASH page) select bits
14	FPGA_IMAGE_1	RW	
15	FPGA_RELOAD	WO	Initiates the fieldhub communication modules FPGA reload. Check the new firmware revision. All registers are set to default values now !

FH_GSTAT @ 01h Communication Module Global Status Register power on state: **0000h**

Bit	Signal	Attribute	Description
0	'0'	RO	not used
1	'0'	RO	not used
2	'0'	RO	not used
3	'0'	RO	not used
4	TSTRG_10x	RO	Ten time strings (10x18x9bit) are available for readout.
5	TSTRG_1x	RO	One (at least) time string (18x9bit) is available for readout.
6	TSTRG_F_FF	RO	Time String Fifo Full Flag. Eleven time strings are available for readout.
7	'0'	RO	not used
8	IRIGB_DET	RWC	IRIG-B signal detected, for test purposes. Writing a "1" clears the bit temporarily, must be "1" again after <10ms
9	IRIGB_MISSED	RWC	IRIG-B data stream interrupted for >18 ms. Writing a "1" clears the bit.
10	IRIGB_PAR_ERR	RWC	Parity error detected while recording the IRIG-B data stream. Writing a "1" clears the bit.
11	'0'	RO	not used
12	FL_PROG_DONE	RO	'0' after writing to the FL_BUF register, '1' when the latest programming cycle is done
13	'0'	RO	not used
14	'0'	RO	not used
15	COM_ID_VALID	RO	the communications modules-ID is valid (after power on / FPGA reload)

FH_PSTAT @ 02h Communication Module Power Status Register power on state: **0000h**

Bit	Signal	Attribute	Description
0	CBL_PLGD	RO	the quad cable has been plugged
1	CBL_STAT_CHGD	RWC	the quad cable has been plugged / unplugged
2	WP_PON_RDY	RWC	the wire pair has been powered on, current and voltage values are within the limits
3	WP_PON_FAILED	RWC	the wire pair has been powered on, current and / or voltage is beyond the limits (see FH_CURL, FH_VOLTL reg.) or a cable has been unplugged while under power. Check the FH_PSTAT reg. for details.
4	WP_CUR_BL	RWC	wire pair current is BELOW the limits, the current was smaller than the programmed value, see FH_CURL reg.
5	WP_CUR_AL	RWC	wire pair current is ABOVE the limits, the current was bigger than the programmed value, see FH_CURL reg.
6	WP_VOLT_BL	RWC	wire pair voltage is BELOW the limits, the voltage was smaller than the programmed value, see FH_VOLTL reg.
7	WP_VOLT_AL	RWC	wire pair voltage is ABOVE the limits, the voltage was bigger than the programmed value, see FH_VOLTL reg.
8..15	‘0’	RO	not used

FH_CUR @ 03h Communication Module Current Register power on state: **0000h**

Bit	Signal	Attribute	Description
0..11	WP_CUR_11..0	RO	wire pair current, 4.2 mA / bit
13..15	0	RO	not used

FH_VOLT @ 04h Communication Module Voltage Register power on state: **0000h**

Bit	Signal	Attribute	Description
0..11	WP_VOLT_11..0	RO	wire pair voltage, 0.34426 V / bit
13..15	0	RO	not used

FH_CURL @ 05h Communication Module Current Limit Register power on state: **8E05h**

Bit	Signal	Attribute	Description
0..7	CUR_MIN_0..7	RW	4.2 mA / bit, default = 21mA
8..15	CUR_MAX_0..7	RW	4.2 mA / bit, default = 600 mA

FH_VOLTL @ 06h Communication Module Voltage Limit Register power on state: **9165h**

Bit	Signal	Attribute	Description
0..7	VOLT_MIN_0..7	RW	0,68852 V / bit, default = 70 V
8..15	VOLT_MAX_0..7	RW	0,68852 V / bit, default = 100 V

FH_TIME @ 07h Communication Module Time Stamp Register power on state: **0000h**

Bit	Signal	Attribute	Description
0..15	TIME_STAMP_0..47	RO	25ns resolution, burst read of 3 words, bits 15..0 first

FH_TSTRG @ 08h Communication Module Time String Register power on state: **0000h**

Bit	Signal	Attribute	Description
0..15	TSTRG_BYTES_0..19	RO	burst read of 11 words, bits 15..0 first

The 20 bytes are defined as followed:

byte	meaning	comment
0	(SOH)	Start Of Header (ASCII control character)
1..3	DDD	Julian day
4	":"	delimiter
5..6	HH	hour
7	":"	delimiter
8..9	MM	minute
10	":"	delimiter
11..12	SS	second
13	Q	Quality indicator of the 1PPS accuracy, see table below
14..19	CCCCCCCC	Binary (!!!) timer[47..0] snapshot, multiples of 25ns (40MHz), byte14 is the most -, byte 21 the least significant byte

The 1PPS quality indicator Q according to the GPS systems (ET6010 ExacTime GPS TC & FG) manual:

ASCII Character	HEX Equivalent	Definition
(space)	20	< 1 microsecond
.	2E	< 10 microsecond
*	2A	< 100 microsecond
#	23	< 1 millisecond
?	3F	> 1 millisecond

FH_FLADR @ 09h Communication Module Flash Address Register power on state: **0000h**

Bit	Signal	Attribute	Description
0..15	FL_ADR_0..31	RW	FPGA configurations flash, start address, burst read / write of 2 words, bits 15..0 first

FH_FLBUF @ 0Ah Communication Module Flash Data Buffer power on state: **0000h**

Bit	Signal	Attribute	Description
0..15	FL_DATA_0..15	RW	FPGA configuration flash, data buffer burst read / write of 2 ..1024 words

FH_ID @ FEh Communication Module ID power on state: **xxxxh**

Bit	Signal	Attribute	Description
0..15	FH_ID_0..15	RO	communication modules 64bit unique ID, burst read of 4 words, bits 15..0 first

FH_FREV @ FFh Communication Module Firmware revision power on state: **xxxxh**

Bit	Signal	Attribute	Description
0..15	FH_FREV_0..15	RO	communication modules firmware revision

xDOM access, ICM Control & Status Registers - Detailed Description

ICM_CTRL1@ 00h ICM Control register #1 power on state: **0000h**

Bit	Signal	Attribute	Description
0	xDOM_PON	RW	xDOM secondary psupply on/off
1	COM_RES	RWSC	writing a '1' resets the comm. state machines and clears all comm. buffers
2	MCU_RES	RWSC	writing a'1' generates a xDOM-MCU reset pulse
3	x	RW	Unused
4	x	RW	Unused
5	x	RW	Unused
6	x	RW	Unused
7	TERM_ENA	RW	enables the ICMs cable termination
8	ICM_ID_UPDATE	RWSC	writing a'1' updates the ICM_ID register
9	PCA_ID_UPDATE	RWSC	writing a'1' updates the xDOM_ID register
10	ICM_FREV_UPDATE	RWSC	writing a'1' updates the ICM FREV register
11	x	RW	Unused
12	TCAL_REQ	RWSC	writing a'1' initiates a time calibration cycle
13	TRIG_REQ	RWSC	writing a'1' generates a time stamped trigger signal
14	x	RW	Unused
15	x	RW	Unused

ICM_CTRL2@ 01h ICM Control register #2 power on state: **0000h**

Bit	Signal	Attribute	Description
0	INTLK_0	RW	'1' actvates interlock #0
1	INTLK_1	RW	'1' actvates interlock #1
2	INTLK_2	RW	'1' actvates interlock #2
3	INTLK_3	RW	'1' actvates interlock #3
4	INTLK_ENA	RW	'1' enables the interlocks
5	x	RW	Unused
6	x	RW	Unused
7	x	RW	Unused
8	x	RW	Unused
9	x	RW	Unused
10	x	RW	Unused
11	x	RW	Unused
12	x	RW	Unused
13	FPGA_IMAGE_0	RW	ICM FPGA firmware (FLASH page) select
14	FPGA_IMAGE_1	RW	ICM FPGA firmware (FLASH page) select
15	FPGA_RELOAD	WO	Initiates the ICMs FPGA reload. Check the new firmware revision afterwards. All registers are set to default values then !

ICM_STAT@ 02h ICM Status Register power on state: **0017h**

Bit	Signal	Attribute	Description
0	ICM_TXBUF_EF	RO	Tx buffer is empty
1	ICM_TXBUF_AEF	RO	Tx buffer is almost empty, a word string of max. packet length (e.g. 1024) can be written to the Tx buffer
2	ICM_RXBUF_EF	RO	Rx buffer is empty
3	ICM_RXBUF_AFF	RO	Rx buffer is almost full, xDOM data read request is stopped
4	ICM_FLBUF_EF	RO	all ICM flash data have been transmitted
5	'0'	RO	not used
6	'0'	RO	not used
7	TERM_ENABLED	RO	ICMs cable termination is active
8	ICM_ID_AVAIL	RO	ICM_ID register contents is valid
9	PCA_ID_AVAIL	RO	PCA_ID register contents is valid
10	ICM_FREV_AVAIL	RO	ICM_FREV register contents is valid
11	TCAL_RDY	RO	TCAL buffer contains a valid data set
12	ICM_TRIG_DONE	RO	TRIG_BUF contains valid time stamps
13	COMM_ERR_DET	RWC	CERR reg. not equal to zero
14	ICM_TIME_OUT	RO	lost communication with ICM
15	ICM_DETECTED	RO	to be checked after power on

ICM_CERR @ 03h Communication Error Counter power on state: **0000h**

Bit	Signal	Attribute	Description
0..15	CERR_CT_0..15	RO	communication error counter

ICM_TXBUF @ 04h Tx Data Buffer power on state: **0000h**

Bit	Signal	Attribute	Description
0..15	ICM_TX_DATA_0..15	RO	Tx data buffer port

ICM_WRCVD @ 05h Amount of Words Received from the ICM power on state: **0000h**

Bit	Signal	Attribute	Description
0..15	ICM_WRCVD_0..15	RO	amount of words in the RX_BUF

ICM_RXBUF @ 06h Rx Data Buffer power on state: **0000h**

Bit	Signal	Attribute	Description
0..15	ICM_RX_DATA_0..15	RO	Rx data buffer port

ICM_TCBUF @ 07h TCAL Data Buffer power on state: **0000h**

Bit	Signal	Attribute	Description
0..15	ICM_TCAL_DATA_0..15	RO	TCAL data buffer port

ICM_TRBUF @ 08h Trigger Data Buffer power on state: **0000h**

Bit	Signal	Attribute	Description
0..15	ICM_RX_DATA_0..15	RO	trigger time stamps buffer port

ICM_FLADR @ 09h Comm. Module Flash Address Register power on state: **0000h**

Bit	Signal	Attribute	Description
0..15	ICM_FL_ADR_0..31	RW	ICM FPGA configurations flash, start address, burst read / write of 2 words, bits 15..0 first

ICM_FLBUF @ 0Ah Communication Module Flash Data Buffer power on state: **0000h**

Bit	Signal	Attribute	Description
0..15	ICM_FL_DATA_0..15	RW	ICM FPGA configuration flash, data buffer burst read / write of 2 ..1024 words

ICM_ID @ FDh ICM ID power on state: **0000h**

Bit	Signal	Attribute	Description
0..15	ICM_ID_0..15	RO	ICMs 64bit unique ID, burst read of 4 words, bits 15..0 first

ICM_PCA_ID @ FEh ICM-PCA ID power on state: **0000h**

Bit	Signal	Attribute	Description
0..15	ICM_PCA_ID_0..15	RO	xDOM main board 64bit unique ID, burst read of 4 words, bits 15..0 first

ICM_FREV @ FFh ICM Firmware revision power on state: **0000h**

Bit	Signal	Attribute	Description
0..15	ICM_FREV_0..15	RO	ICMs firmware revision