

# 4 x 5 SoM Integration Guide

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## Power and Signal Pin Assignment

### How to Use This Guide

- This guide is split into two tables:
    - Module Power Connection Table** section shows the power source of the different FPGA banks and components of the different module boards as well as the power and group location on the B2B connectors of the module site.
    - Carrier Board Power Connection Table** section shows the power source of the B2B connectors with pins, schematic names and available options of the different carrier boards as well as the power location on the B2B connectors of the carrier site.
  - The PCBs have fixed and variable user supplied I/O voltage pins. Variable power supply pins are colored in four groups (VCCIOA, VCCIOB, VCCIOC and VCCIOD).
- Find your module model on the **Module Power Connection Table** and check the power supply of the different FPGA banks.
  - If the power supply is variable(colored), go to the **Carrier Board Power Connection Table** and see how it's connected on your carrier board. Often the power source can be selected by jumper, resistor or variable used from other connector pin of the carrier board. So use the schematic name or the component designator from the table to search for the available options in the PCB schematics or TRM.
  - Additional Master Pinout Viewer/XDC-Generator is available on [Trenz Electronic Download - Pinout](#)

### Module Power Connection Table

Group	1				2				3				4				5					
Module Model	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs
TE0710	B15	48	HR	VCCIOA	-	-	-	-	-	-	-	-	B34	50	HR	VCCIOD	B16	6	HR	3.3V	B14	8
TE0711	B15	48	HR	VCCIOA	B34	36	HR	VCCIOB	B14	18	HR	3.3V	B35	50	HR	VCCIOD	B16	6	HR	1.8V	B14	8
TE0712	B16	48	HR	VCCIOA	B13	20	HR	VCCIOB	B14	18	HR	3.3V	B15	50	HR	VCCIOD	B13	6	HR	VCCIOB	B14	8
TE0713																						
TE0715-xx-15	B13	48	HR	VCCIOA	B34	16	HR	VCCIOC	B34	18	HR	VCCIOC	B35	50	HR	VCCIOD	B501	6	MIO	1.8V	B500	8
TE0715-xx-30	B13	48	HR	VCCIOA	B34	16	HP	VCCIOC	B34	18	HP	VCCIOC	B35	50	HP	VCCIOD	B501	6	MIO	1.8V	B500	8
TE0720	B35	48	HR	VCCIOA	B34	36	HR	VCCIOB	B33	18	HR	VCCIOC	B13	50	HR	VCCIOD	B501	6	MIO	1.8V	B500	8
TE0820*	B66	48	HP	VCCIOA	B65	16	HP	VCCIOC	B65	18	HP	VCCIOC	B64	50	HP	VCCIOD	B501	6	MIO	3.3V	B501	8
TE0741	B13	48	HR	VCCIOA	B16	16	HR	VCCIOB	B15	18	HR	VCCIOC	B12	50	HR	VCCIOD	GTX	1 Lane			B14	8
TE0742*																						
TE0841	B64	48	HR	VCCIOA	B66	16	HP	VCCIOB	B68	18	HP	VCCIOC	B67	50	HP	VCCIOD	GTH	1 Lane			B65	8
TE0842*																						

I/O resource comparison for all 4x5 modules. There are maximum 4 user supplied I/O voltages (VCCIOA, VCCIOB, VCCIOC and VCCIOD).

Attention: Maximum supply voltage for HP banks is 1.8V.

#### Module B2B FPGA-Banks and Voltages

JMI						
Direction	Name	Pin	Pin	Name	Direction	
in	PWR_1	1	2	GND		
in	PWR_1	3	4	GROUP7 ETH MDIO0	MGT TX io/ta/out	
in	PWR_1	5	6	GROUP7 ETH MDIO0	MGT TX io/ta/out	
io	NOSQ	7	8	GND		
in	VCCIOA	9	10	GROUP7 ETH MDIO1	MGT RX io/ta/in	
in	PWR_2	11	12	GROUP7 ETH MDIO1	MGT RX io/ta/in	
in	PWR_2	13	14	ETH VCC		
io/ta/ta/out	GROUP5 MIO SD D3	MGT TX	17	18	GROUP7 ETH MDIO2	MGT TX io/ta/out
io/ta/ta/out	GROUP5 MIO SD D2	MGT TX	19	20	GND	
io/ta/ta/ta	GROUP5 MIO SD D1	GND	21	22	GROUP7 ETH MDIO3	MGT RX io/ta/in
io/ta/ta/ta	GROUP5 MIO SD D0	GND	23	24	GROUP7 ETH MDIO3	MGT RX io/ta/in
io/ta/ta/in	GROUP5 MIO SD CMD	MGT RX	25	26	GND	
io/ta/ta/in	GROUP5 MIO SD CLK	MGT RX	27	28	SC_FEN1	in
		29	30	SC_PGOOD	io	
io	GROUP1	31	32	SC_BOOTMODE	in	
io	GROUP1	33	34	GND		
io	GROUP1	35	36	GROUP1	io	
io	GROUP1	37	38	GROUP1	io	
out	PWR_M2	39	40	GROUP1	io	
io	GROUP1	41	42	GROUP1	io	
io	GROUP1	43	44	GND		
io	GROUP1	45	46	GROUP1	io	
io	GROUP1	47	48	GROUP1	io	
io	GROUP1	49	50	GROUP1	io	
io	GROUP1	51	52	GROUP1	io	
	GND	53	54	GND		
io	GROUP1	55	56	GROUP1	io	
io	GROUP1	57	58	GROUP1	io	
io	GROUP1	59	60	GROUP1	io	
io	GROUP1	61	62	GROUP1	io	
	GND	63	64	GND		
io	GROUP1	65	66	GROUP1	io	
io	GROUP1	67	68	GROUP1	io	
io	GROUP1	69	70	GROUP1	io	
io	GROUP1	71	72	GROUP1	io	
	GND	73	74	GND		
io	GROUP1	75	76	GROUP1	io	
io	GROUP1	77	78	GROUP1	io	
in	PWR_VBAT	79	80	GROUP1	io	
io	GROUP1	81	82	GROUP1	io	
io	GROUP1	83	84	GND		
io/ta/out	GROUP5 MIO UART TX	85	86	GROUP1	io	
io/ta	GROUP5 MIO	87	88	GROUP1	io	
in	JTAGSEL	89	90	GND		
io/ta	GROUP5 MIO	91	92	GROUP5 MIO	UART RX io/ta/in	
io/ta	GROUP5 MIO	93	94	GROUP1	io	
io/ta	GROUP5 MIO	95	96	GROUP1	io	
io/ta	GROUP5 MIO	97	98	GROUP1	io	
io/ta	GROUP5 MIO	99	100	GROUP1	io	

Positions are displayed as Top View

Legend	
<span style="color: red;">■</span>	Power-VCC
<span style="color: orange;">■</span>	Power-GND
<span style="color: lightblue;">■</span>	GROUP1
<span style="color: lightblue;">■</span>	GROUP2
<span style="color: lightblue;">■</span>	GROUP3
<span style="color: lightblue;">■</span>	GROUP4
<span style="color: lightblue;">■</span>	GROUP5
<span style="color: lightblue;">■</span>	GROUP6
<span style="color: lightblue;">■</span>	GROUP7
<span style="color: lightblue;">■</span>	GROUP8
<span style="color: lightblue;">■</span>	GROUP9
<span style="color: lightblue;">■</span>	Special
<span style="color: yellow;">■</span>	VCCIOA
<span style="color: yellow;">■</span>	VCCIOB
<span style="color: yellow;">■</span>	VCCIOC
<span style="color: yellow;">■</span>	VCCIOD

JMI2					
Direction	Name	Pin	Pin	Name	Direction
in	VCCIOA	1	2	PWR_1	in
in	VCCIOA	3	4	PWR_1	in
in	VCCIOA	5	6	PWR_1	in
in	VCCIOD	7	8	PWR_1	in
in	VCCIOD	9	10	PWR_M1	out
io	GROUP3	11	12	PWR_M1	out
io	GROUP3	13	14	GROUP3	io
io	GROUP3	15	16	GROUP3	io
io	GROUP3	17	18	SC_nRST	in
	PWR_VBAT	19	20	GND	
io	GROUP3	21	22	GROUP3	io
io	GROUP3	23	24	GROUP3	io
io	GROUP3	25	26	GROUP3	io
io	GROUP3	27	28	GROUP3	io
	GND	29	30	GND	
io	GROUP3	31	32	GROUP4	io
io	GROUP3	33	34	GROUP4	io
io	GROUP3	35	36	GROUP4	io
io	GROUP3	37	38	GROUP4	io
	GND	39	40	GND	
io	GROUP4	41	42	GROUP4	io
io	GROUP4	43	44	GROUP4	io
io	GROUP4	45	46	GROUP4	io
io	GROUP4	47	48	GROUP4	io
	GND	49	50	GND	
io	GROUP4	51	52	GROUP4	io
io	GROUP4	53	54	GROUP4	io
io	GROUP4	55	56	GROUP4	io
io	GROUP4	57	58	GROUP4	io
	GND	59	60	GND	
io	GROUP4	61	62	GROUP4	io
io	GROUP4	63	64	GROUP4	io
io	GROUP4	65	66	GROUP4	io
io	GROUP4	67	68	GROUP4	io
	GND	69	70	GND	
io	GROUP4	71	72	GROUP4	io
io	GROUP4	73	74	GROUP4	io
io	GROUP4	75	76	GROUP4	io
io	GROUP4	77	78	GROUP4	io
	GND	79	80	GND	
io	GROUP4	81	82	GROUP4	io
io	GROUP4	83	84	GROUP4	io
io	GROUP4	85	86	GROUP4	io
io	GROUP4	87	88	GROUP4	io
io	GROUP4	89	90	GND	
out	PWR_JTAG	91	92	GROUP4	io
in	TMS	93	94	GROUP4	io
in	TDI	95	96	GROUP4	io
out	TDO	97	98	GROUP4	io
in	TCX	99	100	GROUP4	io

Module basic power and group pin assignment, recommended to verify with Schematics

Carrier Board Power Connection Table

IO Voltage		B2B Connector		Carrier Boards								
Name	Direction*	JB1	JB2	TE0701		TE0703 Rev01 - Rev04		TE0703 Rev 05		TE0705		TE0706
		Pin	Pin	Schematic Name	Value,Option,Comp.	Schematic Name	Value,Option,Comp.	Schematic Name	Value,Option,Comp.	Schematic Name	Value,Option,Comp.	Schematic Name
PWR_1	out	2,4,6	1,3,5,7	5V0	5V	3.3V	3.3V	3.3V	3.3V	5V0	5V	3.3V
VCCIOA	out	10,12		VIOTB	FMC_VADJ 2V5 3.3VOUT	VCCIO35	R23→M3.3VOUT J1B-B1	VCCIOA	J5→M3.3VOUT, M1.8VOUT R23→M3.3VOUT J1-B1	VIOTB	FMC_VADJ 2V5 3.3VOUT	VCCIOB
VCCIOD	out		8,10	VIOTB	FMC_VADJ 2V5 3.3VOUT	VCCIO13	R26→M3.3VOUT J2B-B1	VCCIOD	J10→M3.3VOUT, M1.8VOUT R26→M3.3VOUT J2B-B1	VIOTB	FMC_VADJ 2V5 3.3VOUT	VCCIOE
PWR_2	out	14,16		3V3IN	3.3V	3.3V	3.3V	3.3V	3.3V	3V3IN	3.3V	3.3V
VCCIOB	out		2,4	no name / VIOTA	FMC_VADJ 2V5 3.3VOUT	VCCIO34	J5→M3.3VOUT J1B-B32	VCCIOB	J8→M3.3VOUT,M1.8VOUT J2B-B32	VIOTB	FMC_VADJ 2V5 3.3VOUT	1.8V
VCCIOC	out		6	no name / VIOTA	FMC_VADJ 2V5 3.3VOUT	VCCIO33	R25→M3.3VOUT J2B-B32	VCCIOC	J9→M3.3VOUT, M1.8VOUT R25→M3.3VOUT J2B-B32	VIOTB	FMC_VADJ 2V5 3.3VOUT	VCCIOF
PWR_M1	in		9,11	3.3VOUT	3.3V	3.3VOUT	3.3V	M3.3VOUT	3.3V	3.3VOUT	3.3V	M3.3V
PWR_M2	in	40		VIOB	1.8V	M1.8VOUT	1.8V	M1.8VOUT	1.8V	VIOB	1.8V	M1.8V
PWR_M3	in		20	NC		NC		NC		NC		NC
PWR_VBAT	out	80		VBAT	B1	VBAT	J7	VBAT	J7	NC		VBAT
PWR_JTAG	in		92	VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG

Power comparison of all 4x5 carrier boards. \*Power direction based on carrier boards view. There are 4 variable user supplied I/O voltages (VCCIOA, VCCIOB, VCCIOC and VCCIOD). PWR\_1 and PWR\_2 are fixed from carrier boards. PWR\_M1 and PWR\_M2 normally use default value from module. NC=Not Connected

Attention: On some carrier boards the user supplied I/O voltages are connected together (red colored schematic names).  
Power Pin Connection on different Carrierboards

JB1					JB3					JB2				
Direction	Name	Pin	Pin	Direction	Direction	Name	Pin	Pin	Direction	Direction	Name	Pin	Pin	Direction
out	PWR_1	2	1	GND		IO	2	1	IO		out	VCCIOB	2	1
out	PWR_1	4	3	IO		IO	4	3	IO		out	VCCIOB	4	3
out	PWR_1	6	5	IO		IO	6	5	IO		out	VCCIOB	6	5
io	N0SEQ	8	7	GND		GND	8	7	GND		io	VCCIOB	8	7
out	VCCIOA	10	9	IO		IO	10	9	IO		out	VCCIOB	10	9
out	VCCIOA	12	11	IO		IO	12	11	IO		out	VCCIOB	12	11
out	PWR_2	14	13	ETH_VCC		GND	14	13	IO		out	VCCIOB	14	13
out	PWR_2	16	15	IO		IO	16	15	IO		out	VCCIOB	16	15
	IO	18	17	IO		IO	18	17	IO		out	VCCIOB	18	17
	IO	20	19	GND		IO	20	19	IO		out	VCCIOB	20	19
	IO	22	21	IO		IO	22	21	IO		out	VCCIOB	22	21
	IO	24	23	IO		IO	24	23	IO		out	VCCIOB	24	23
	IO	26	25	GND		IO	26	25	IO		out	VCCIOB	26	25
	IO	28	27	GND		IO	28	27	IO		out	VCCIOB	28	27
	IO	30	29	SC_EN1	out	IO	30	29	IO		out	VCCIOB	30	29
	IO	32	31	SC_PGOOD	io	IO	32	31	IO		out	VCCIOB	32	31
	IO	34	33	SC_BOOTMODE	out	IO	34	33	IO		out	VCCIOB	34	33
	IO	36	35	GND		IO	36	35	IO		out	VCCIOB	36	35
	IO	38	37	IO		IO	38	37	IO		out	VCCIOB	38	37
in	PWR_M1	40	39	IO		IO	40	39	IO		out	VCCIOB	40	39
	IO	42	41	IO		IO	42	41	IO		out	VCCIOB	42	41
	IO	44	43	GND		IO	44	43	IO		out	VCCIOB	44	43
	IO	46	45	IO		IO	46	45	IO		out	VCCIOB	46	45
	IO	48	47	IO		IO	48	47	IO		out	VCCIOB	48	47
	IO	50	49	IO		IO	50	49	IO		out	VCCIOB	50	49
	IO	52	51	IO		IO	52	51	IO		out	VCCIOB	52	51
	GND	54	53	GND		IO	54	53	IO		out	VCCIOB	54	53
	IO	56	55	IO		IO	56	55	IO		out	VCCIOB	56	55
	IO	58	57	IO		IO	58	57	IO		out	VCCIOB	58	57
	IO	60	59	IO		IO	60	59	IO		out	VCCIOB	60	59
	IO	62	61	IO		IO	62	61	IO		out	VCCIOB	62	61
	GND	64	63	GND		IO	64	63	IO		out	VCCIOB	64	63
	IO	66	65	IO		IO	66	65	IO		out	VCCIOB	66	65
	IO	68	67	IO		IO	68	67	IO		out	VCCIOB	68	67
	IO	70	69	IO		IO	70	69	IO		out	VCCIOB	70	69
	IO	72	71	IO		IO	72	71	IO		out	VCCIOB	72	71
	GND	74	73	GND		IO	74	73	IO		out	VCCIOB	74	73
	IO	76	75	IO		IO	76	75	IO		out	VCCIOB	76	75
	IO	78	77	IO		IO	78	77	IO		out	VCCIOB	78	77
out	ETH_M1	80	79	IO		IO	80	79	IO		out	VCCIOB	80	79
io	IO	82	81	IO		IO	82	81	IO		out	VCCIOB	82	81
io	IO	84	83	GND		IO	84	83	IO		out	VCCIOB	84	83
in	ID/UART TX	86	85	IO		IO	86	85	IO		out	VCCIOB	86	85
io	IO	88	87	IO		IO	88	87	IO		out	VCCIOB	88	87
out	JTAGSEL	90	89	GND		IO	90	89	IO		out	VCCIOB	90	89
io	IO	92	91	ID/UART RX	out	IO	92	91	IO		out	VCCIOB	92	91
io	IO	94	93	IO		IO	94	93	IO		out	VCCIOB	94	93
io	IO	96	95	IO		IO	96	95	IO		out	VCCIOB	96	95
io	IO	98	97	IO		IO	98	97	IO		out	VCCIOB	98	97
io	IO	100	99	IO		IO	100	99	IO		out	VCCIOB	100	99

Positions are displayed as Top View

Legend

Power-VCC

Power-GND

Special

IO / Special

VCCIOA

VCCIOB

VCCIOB

VCCIOB

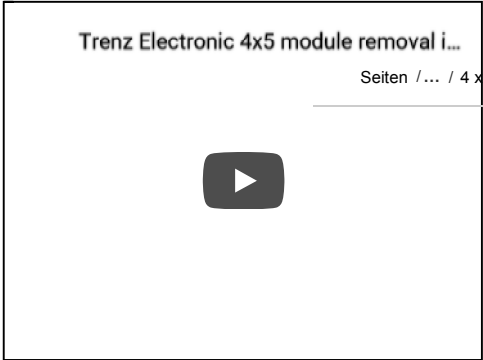
Carrierboard basic power and group pin assignment (Top View), recommended to verify with Schematics

4x5 Module Controller IOs

Name	Module B2B Pin	Carrier B2B Pin	Direction (Module view)	Description	Recommendation
JTAGSEL	JM1-89	JB1-90	in	JTAG Chain multiplexer. Low FPGA, High CPLD. For module with CPLD only.	Connect Pulldown on carrier. DIP switch possible.
SC_EN1	JM1-28	JB1-27	in	Module power. Set high to enable module power. Note: Power management depends on module. Sometimes this is a only used as Power ON Reset like SC_nRST	Connect Pullup on carrier. DIP switch possible
SC_NOSEQ	JM1-7	JB1-8	in / inout	Module Power management. Set high to disable CPLD power management. Note: Power management depends on module and not all modules support extended power management with CPLD.	Connect Pullup on carrier. DIP switch possible.
SC_PGOOD	JM1-30	JB1-29	out / inout	Power Good signal. Is Low, if SC_EN1 is set to zero or if power is not ready, otherwise high impedance output. Note: Power management depends on module.	Connect Pullup on carrier. Do <b>not</b> use this signal to enable FPGA Bank voltages. It's only for monitoring. To Enable FPGA Banks, use 3.3V(PWR_M1) or 1.8V(PWR_M2) module output.
SC_BOOTMODE	JM1-32	JB1-31	in	Boot Mode selection Pin for Zynq module only. Default low for primary SD boot and high for primary QSPI boot. Note: Depends also on module CPLD firmware	Connect Pullup on carrier. DIP switch possible.
SC_nRST	JM2-18	JB2-17	in	Low active module reset. Pin force Power one reset on FPGA/SoC. Note: Depending from module CPLD or voltage supervisor is used.	Connect Pullup on carrier. DIP switch possible.

4x5 Module Controller IOs

Remove 4x5 module



Seiten / ... / 4 x 5 SoM General Documentation

Always loosen the screws only a little step by step so that the module is evenly squeezed out. Otherwise solder contacts can break.

Compatibility Guide

Ethernet LED'S

TE07xx 4x5 modules do not have dedicated pins for the Ethernet PHY LED's, also there are no fix pins on the baseboards for the PHY LED's or any other LED's.  
If Ethernet JACKs on Baseboard have LED's then those should be connected to some free PL I/O pins, and then routed in the FPGA logic from the PHY to the I/O Pin in the B2B Connector.  
Recommended connections would be to use JM2.89 and JM2.100 for the PHY LED's, those positions support baseboard ETH LED's for TE0701 and TE0703 and TE0706.

JM2 pins 1, 3 (TE0720 Bank 34 Voltage)

To be compatible with TE0720 JM2 pins 1,3 must be connected to some valid VCCIO voltage.  
When JM2 pins 1, 3 are not powered TE0720 would not boot, and may not be recognized in JTAG chain as well.  
When those pins are not used on the module (TE0710) then to be compatible with TE0720:  
Solution A: connect to 3.3V out from the module, option compatible to all modules except those with HP banks (TE0715-01-30)  
Solution B: connect to 1.8V out from the module, option compatible with all modules.

Carrier Board Checklist

Schematic Checklist

1	Are B2B pin numbers on the connectors mirrored compared to the module pin numbers?	As B2B connectors are "unisex" type the do mirror pin numbers when connecting. That is pin1 connects to pin2, and pin2 to pin1, etc.
2	Are B2B connectors named JB1, JB2, JB3?	This is not a hard requirement, but it helps to use the same identifiers.
3	Are all GND pins connected to a common ground net?	
4	Are all VIN pins connected together?	
5	Is JB2 pin 92 pin used as VREF for the JTAG interface?	for future compatibility only, currently all modules have 3.3V JTAG
6	For 7 Series Zynq module only: Are external circuits/buffers connecting to MIO bank 1 pins powered from JB1 pin 40?	JB1 pins 18, 20, 22, 24, 26, 28 use voltage at pin 40 as VCCIO. Currently it is 1.8V for 4x5 Zynq Modules. Note: Different Power supply on TE0820(3.3V MIO Bank) and normal FPGA modules(check schematics)

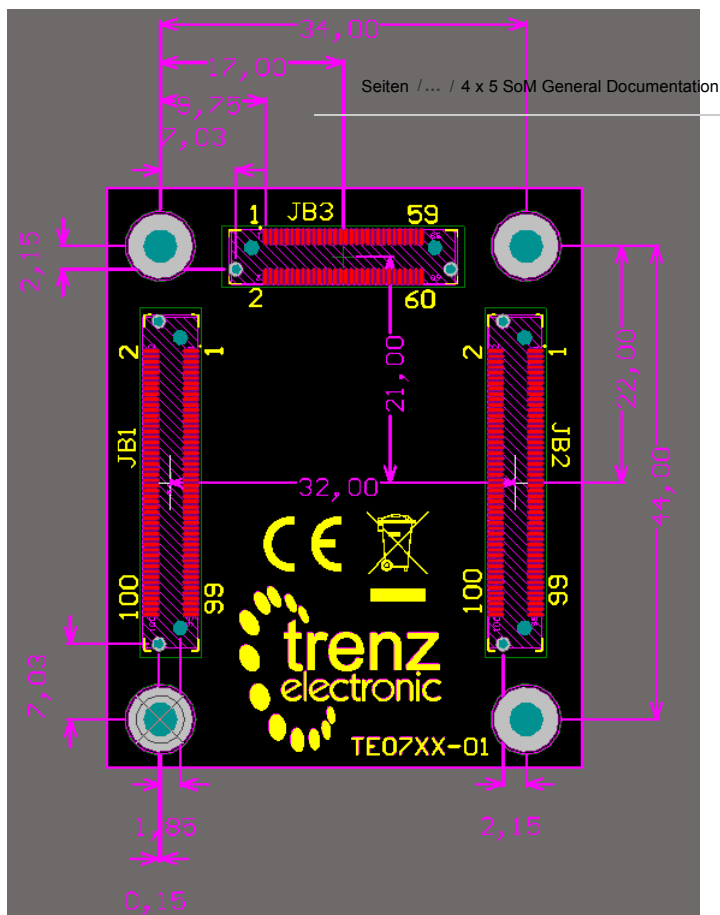
PCB Checklist

1	Are mounting holes placed properly?	Four Mounting holes should always be used. They are required for mounting screws and for module extraction. The mounting holes will also help in dissipating some heat from the module to the carried board PCB. Four holes with a 3.2mm diameter should be placed exactly at the corners of a 34mm by 44mm rectangle.
2	Are B2B headers properly placed?	B2B headers must be placed and aligned very precisely or the module will not align correctly (in the worst case module insertion could destroy the connectors or the PCB). The B2B headers should be locked on the PCB, and it is recommended that the position and placement be checked against placement dimensions before submitting the PCB files.
3	Are B2B headers rotated properly?	As B2B header pin numbers differ from module to the carrier (swap of odd and even numbers), it is recommended that the rotation is checked in the PCB design.
4	Height clearance below module	Components can be placed below the module but height clearance rules must be obeyed.
5	Power dissipation of components below module	It is not recommended to place any components with high power dissipation below the module, as there will be almost no airflow below the module.

Visual Check of Module placement

It is highly recommended to use the Base board Template designs as a starting point for new PCB designs. If that is not possible, then adding linear dimensions in the design helps to check that all connectors and mounting holes are properly placed.

This placement is same for all 4x5 Modules!



**Top view of the Carrier Board.**

Connector numbers as on base! (pin JB1.1 on base would mate to pin JM1.2 on module).