4 x 5 SoM Integration Guide

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Power and Signal Pin Assignment

How to Use This Guide

- This guide is split into two tables:
  - **Module Power Connection Table** section shows the power source of the different FPGA banks and components of the different module boards as well as the power and group location on the B2B connectors of the module site.
  - **Carrier Board Power Connection Table** section shows the power source of the B2B connectors with pins, schematic names and available options of the different carrier boards as well as the power location on the B2B connectors of the carrier site.
- The PCBs have fixed and variable user supplied I/O voltage pins. Variable power supply pins are colored in four groups (VCCIOA, VCCIOB, VCCIOC and VCCIOD).

1. Find your module model on the **Module Power Connection Table** and check the power supply of the different FPGA banks.
2. If the power supply is variable(colored), go to the **Carrier Board Power Connection Table** and see how it's connected on your carrier board. Often the power source can be selected by jumper, resistor or variable used from other connector pin of the carrier board. So use the schematic name or the component designator from the table to search for the available options in the PCB schematics or TRM.
3. Additional Master Pinout Viewer/XDC-Generator is available on Trenz Electronic Download - Pinout

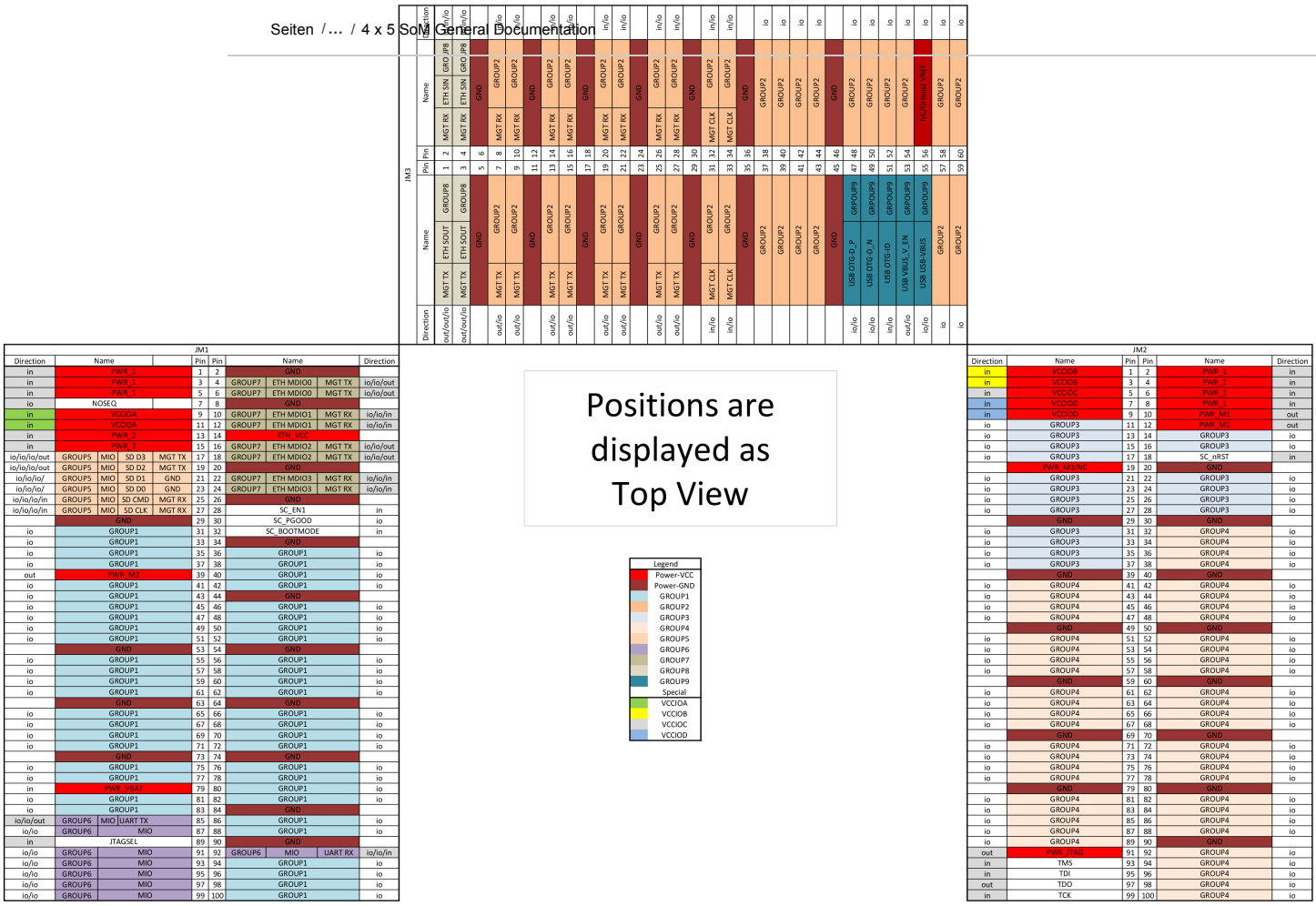
Module Power Connection Table

Group	1				2				3				4				5					
Module Model	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs	Type	Voltage	Bank	IOs
TE0710	B15	48	HR	VCCIOA	-	-	-	-	-	-	-	-	B34	50	HR	VCCIOD	B16	6	HR	3.3V	B14	8
TE0711	B15	48	HR	VCCIOA	B34	36	HR	VCCIOB	B14	18	HR	3.3V	B35	50	HR	VCCIOD	B16	6	HR	1.8V	B14	8
TE0712	B16	48	HR	VCCIOA	B13	20	HR	VCCIOB	B14	18	HR	3.3V	B15	50	HR	VCCIOD	B13	6	HR	VCCIOB	B14	8
TE0713																						
TE0715-xx-15	B13	48	HR	VCCIOA	B34	16	HR	VCCIOC	B34	18	HR	VCCIOC	B35	50	HR	VCCIOD	B501	6	MIO	1.8V	B500	8
TE0715-xx-30	B13	48	HR	VCCIOA	B34	16	HP	VCCIOC	B34	18	HP	VCCIOC	B35	50	HP	VCCIOD	B501	6	MIO	1.8V	B500	8
TE0720	B35	48	HR	VCCIOA	B34	36	HR	VCCIOB	B33	18	HR	VCCIOC	B13	50	HR	VCCIOD	B501	6	MIO	1.8V	B500	8
TE0820*	B66	48	HP	VCCIOA	B65	16	HP	VCCIOC	B65	18	HP	VCCIOC	B64	50	HP	VCCIOD	B501	6	MIO	3.3V	B501	8
TE0741	B13	48	HR	VCCIOA	B16	16	HR	VCCIOB	B15	18	HR	VCCIOC	B12	50	HR	VCCIOD	GTX	1 Lane			B14	8
TE0742*																						
TE0841	B64	48	HR	VCCIOA	B66	16	HP	VCCIOB	B68	18	HP	VCCIOC	B67	50	HP	VCCIOD	GTH	1 Lane			B65	8
TE0842*																						

I/O resource comparison for all 4x5 modules. There are maximum 4 user supplied I/O voltages (VCCIOA, VCCIOB, VCCIOC and VCCIOD).

Attention: Maximum supply voltage for HP banks is 1.8V.

Module B2B FPGA-Banks and Voltages



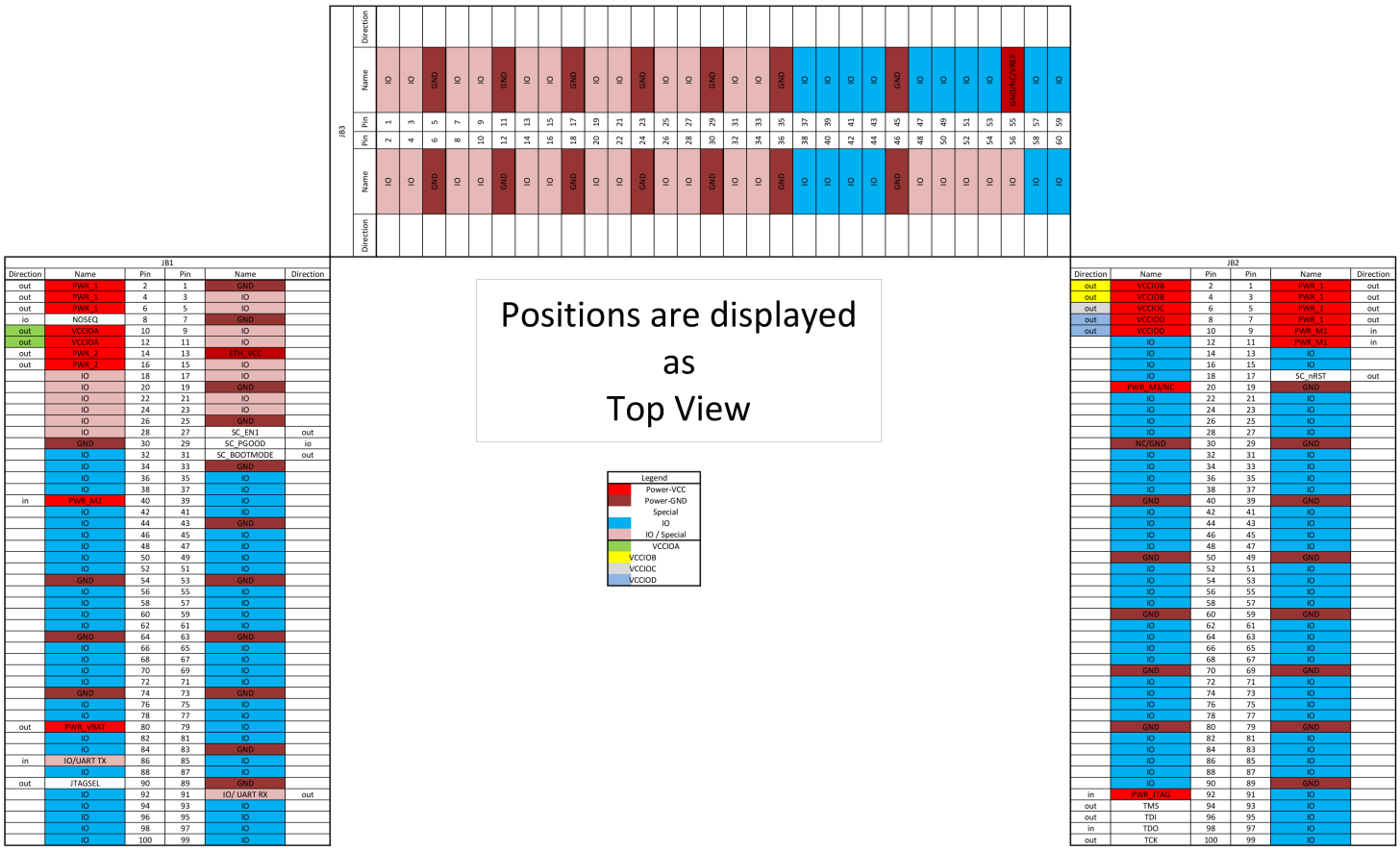
Module basic power and group pin assignment, recommended to verify with Schematics

Carrier Board Power Connection Table

IO Voltage		B2B Connector		Carrier Boards								
Name	**Direction***	JB1	JB2	TE0701		TE0703 Rev01 - Rev04		TE0703 Rev 05		TE0705		TE
		Pin	Pin	Schematic Name	Value,Option,Comp.	Schematic Name	Value,Option,Comp.	Schematic Name	Value,Option,Comp.	Schematic Name	Value,Option,Comp.	Sc Na
PWR_1	out	2,4,6	1,3,5,7	5V0	5V	3.3V	3.3V	3.3V	3.3V	5V0	5V	3.3
VCCIOA	out	10,12		VIOTB	FMC_VADJ 2V5 3.3VOUT	VCCIO35	R23→M3.3VOUT J1B-B1	VCCIOA	J5→M3.3VOUT, M1.8VOUT R23→M3.3VOUT J1-B1	VIOTB	FMC_VADJ 2V5 3.3VOUT	VC
VCCIOD	out		8,10	VIOTB	FMC_VADJ 2V5 3.3VOUT	VCCIO13	R26→M3.3VOUT J2B-B1	VCCIOD	J10→M3.3VOUT, M1.8VOUT R26→M3.3VOUT J2B-B1	VIOTB	FMC_VADJ 2V5 3.3VOUT	VC
PWR_2	out	14,16		3V3IN	3.3V	3.3V	3.3V	3.3V	3.3V	3V3IN	3.3V	3.3
VCCIOB	out		2,4	no name / VIOTA	FMC_VADJ 2V5 3.3VOUT	VCCIO34	J5→M3.3VOUT J1B-B32	VCCIOB	J8→M3.3VOUT,M1.8VOUT J2B-B32	VIOTB	FMC_VADJ 2V5 3.3VOUT	1.8
VCCIOC	out		6	no name / VIOTA	FMC_VADJ 2V5 3.3VOUT	VCCIO33	R25→M3.3VOUT J2B-B32	VCCIOC	J9→M3.3VOUT, M1.8VOUT R25→M3.3VOUT J2B-B32	VIOTB	FMC_VADJ 2V5 3.3VOUT	VC
PWR_M1	in		9,11	3.3VOUT	3.3V	3.3VOUT	3.3V	M3.3VOUT	3.3V	3.3VOUT	3.3V	M3
PWR_M2	in	40		VIOB	1.8V	M1.8VOUT	1.8V	M1.8VOUT	1.8V	VIOB	1.8V	M1
PWR_M3	in		20	NC		NC		NC		NC		NC
PWR_VBAT	out	80		VBAT	B1	VBAT	J7	VBAT	J7	NC		VB
PWR_JTAG	in		92	VCCJTAG		VCCJTAG		VCCJTAG		VCCJTAG		VC

Power comparison of all 4x5 carrier boards. ***Power direction based on carrier boards view.**There are 4 variable user supplied I/O voltages (VCCIOA, VCCIOB, VCCIOC and VCCIOD). PWR_1 and PWR_2 are fixed from carrier boards. PWR_M1 and PWR_M2 normally use default value from module. NC=Not Connected

Attention: On some carrier boards the user supplied I/O voltages are connected together (red colored schematic names).
Power Pin Connection on different Carrierboards



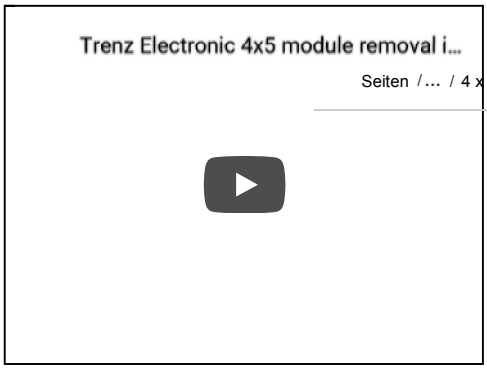
Carrierboard basic power and group pin assignment (Top View), recommended to verify with Schematics

4x5 Module Controller IOs

Name	Module B2B Pin	Carrier B2B Pin	Direction (Module view)	Description	Recommendation
JTAGSEL	JM1-89	JB1-90	in	JTAG Chain multiplexer. Low FPGA, High CPLD. For module with CPLD only.	Connect Pulldown on carrier. DIP switch possible.
SC_EN1	JM1-28	JB1-27	in	Module power. Set high to enable module power. Note: Power management depends on module. Sometimes this is a only used as Power ON Reset like SC_nRST	Connect Pullup on carrier. DIP switch possible
SC_NOSEQ	JM1-7	JB1-8	in / inout	Module Power management. Set high to disable CPLD power management. Note: Power management depends on module and not all modules support extended power management with CPLD.	Connect Pullup on carrier. DIP switch possible.
SC_PGOOD	JM1-30	JB1-29	out / inout	Power Good signal. Is Low, if SC_EN1 is set to zero or if power is not ready, otherwise high impedance output. Note: Power management depends on module.	Connect Pullup on carrier. Do **not** use this signal to enable FPGA Bank voltages. It's only for monitoring. To Enable FPGA Banks, use 3.3V(PWR_M1) or 1.8V(PWR_M2) module output.
SC_BOOTMODE	JM1-32	JB1-31	in	Boot Mode selection Pin for Zynq module only. Default low for primary SD boot and high for primary QSPI boot. Note: Depends also on module CPLD firmware	Connect Pullup on carrier. DIP switch possible.
SC_nRST	JM2-18	JB2-17	in	Low active module reset. Pin force Power one reset on FPGA/SoC. Note: Depending from module CPLD or voltage supervisor is used.	Connect Pullup on carrier. DIP switch possible.

4x5 Module Controller IOs

Remove 4x5 module



Always loosen the screws only a little step by step so that the module is evenly squeezed out. Otherwise solder contacts can break.

Compatibility Guide

Ethernet LED'S

TE07xx 4x5 modules do not have dedicated pins for the Ethernet PHY LED's, also there are no fix pins on the baseboards for the PHY LED's or any other LED's.

If Ethernet JACKs on Baseboard have LED's then those should be connected to some free PL I/O pins, and then routed in the FPGA logic from the PHY to the I/O Pin in the B2B Connector.

Recommended connections would be to use JM2.89 and JM2.100 for the PHY LED's, those positions support baseboard ETH LED's for TE0701 and TE0703 and TE0706.

JM2 pins 1, 3 (TE0720 Bank 34 Voltage)

To be compatible with TE0720 JM2 pins 1,3 must be connected to some valid VCCIO voltage.

When JM2 pins 1, 3 are not powered TE0720 would not boot, and may not be recognized in JTAG chain as well.

When those pins are not used on the module (TE0710) then to be compatible with TE0720:

Solution A: connect to 3.3V out from the module, option compatible to all modules except those with HP banks (TE0715-01-30)

Solution B: connect to 1.8V out from the module, option compatible with all modules.

Carrier Board Checklist

Schematic Checklist

1	Are B2B pin numbers on the connectors mirrored compared to the module pin numbers?	As B2B connectors are "unisex" type the do mirror pin numbers when connecting. That is pin1 connects to pin2, and pin2 to pin1, etc.
2	Are B2B connectors named JB1, JB2, JB3?	This is not a hard requirement, but it helps to use the same identifiers.
3	Are all GND pins connected to a common ground net?	
4	Are all VIN pins connected together?	
5	Is JB2 pin 92 pin used as VREF for the JTAG interface?	for future compatibility only, currently all modules have 3.3V JTAG
6	For 7 Series Zynq module only: Are external circuits/buffers connecting to MIO bank 1 pins powered from JB1 pin 40?	JB1 pins 18, 20, 22, 24, 26, 28 use voltage at pin 40 as VCCIO. Currently it is 1.8V for 4x5 Zynq Modules. Note: Different Power supply on TE0820(3.3V MIO Bank) and normal FPGA modules(check schematics)

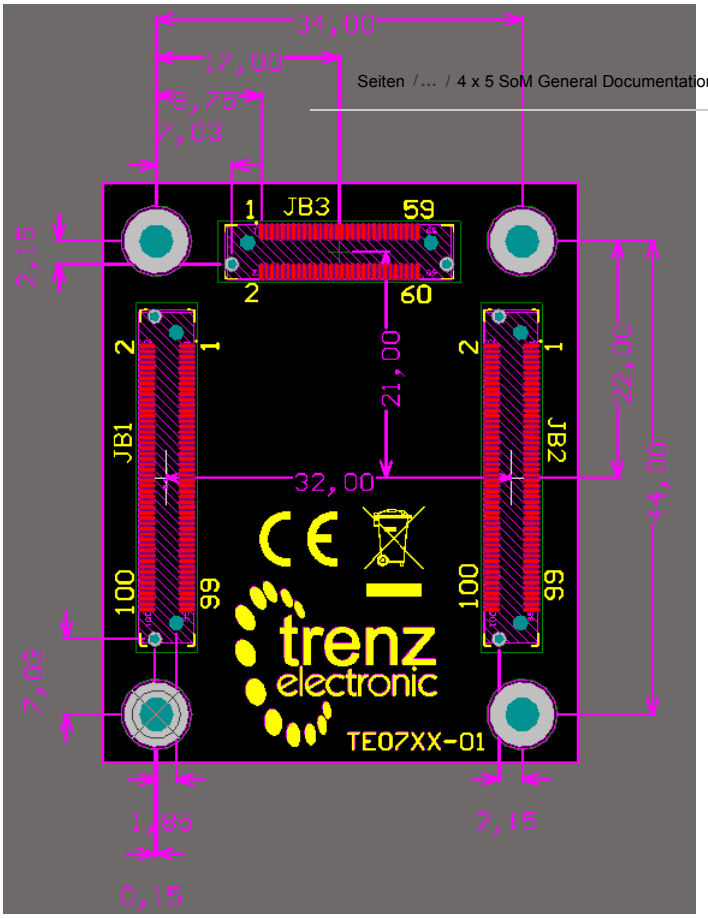
PCB Checklist

1	Are mounting holes placed properly?	Four Mounting holes should always be used. They are required for mounting screws and for module extraction. The mounting holes will also help in dissipating some heat from the module to the carried board PCB. Four holes with a 3.2mm diameter should be placed exactly at the corners of a 34mm by 44mm rectangle.
2	Are B2B headers properly placed?	B2B headers must be placed and aligned very precisely or the module will not align correctly (in the worst case module insertion could destroy the connectors or the PCB). The B2B headers should be locked on the PCB, and it is recommended that the position and placement be checked against placement dimensions before submitting the PCB files.
3	Are B2B headers rotated properly?	As B2B header pin numbers differ from module to the carrier (swap of odd and even numbers), it is recommended that the rotation is checked in the PCB design.
4	Height clearance below module	Components can be placed below the module but height clearance rules must be obeyed.
5	Power dissipation of components below module	It is not recommended to place any components with high power dissipation below the module, as there will be almost no airflow below the module.

Visual Check of Module placement

It is highly recommended to use the Base board Template designs as a starting point for new PCB designs. If that is not possible, then adding linear dimensions in the design helps to check that all connectors and mounting holes are properly placed.

This placement is same for all 4x5 Modules!



Top view of the Carrier Board.

Connector numbers as on base! (pin JB1.1 on base would mate to pin JM1.2 on module).

Keine Stichwörter