mDOM Mainboard Rev.1, Status

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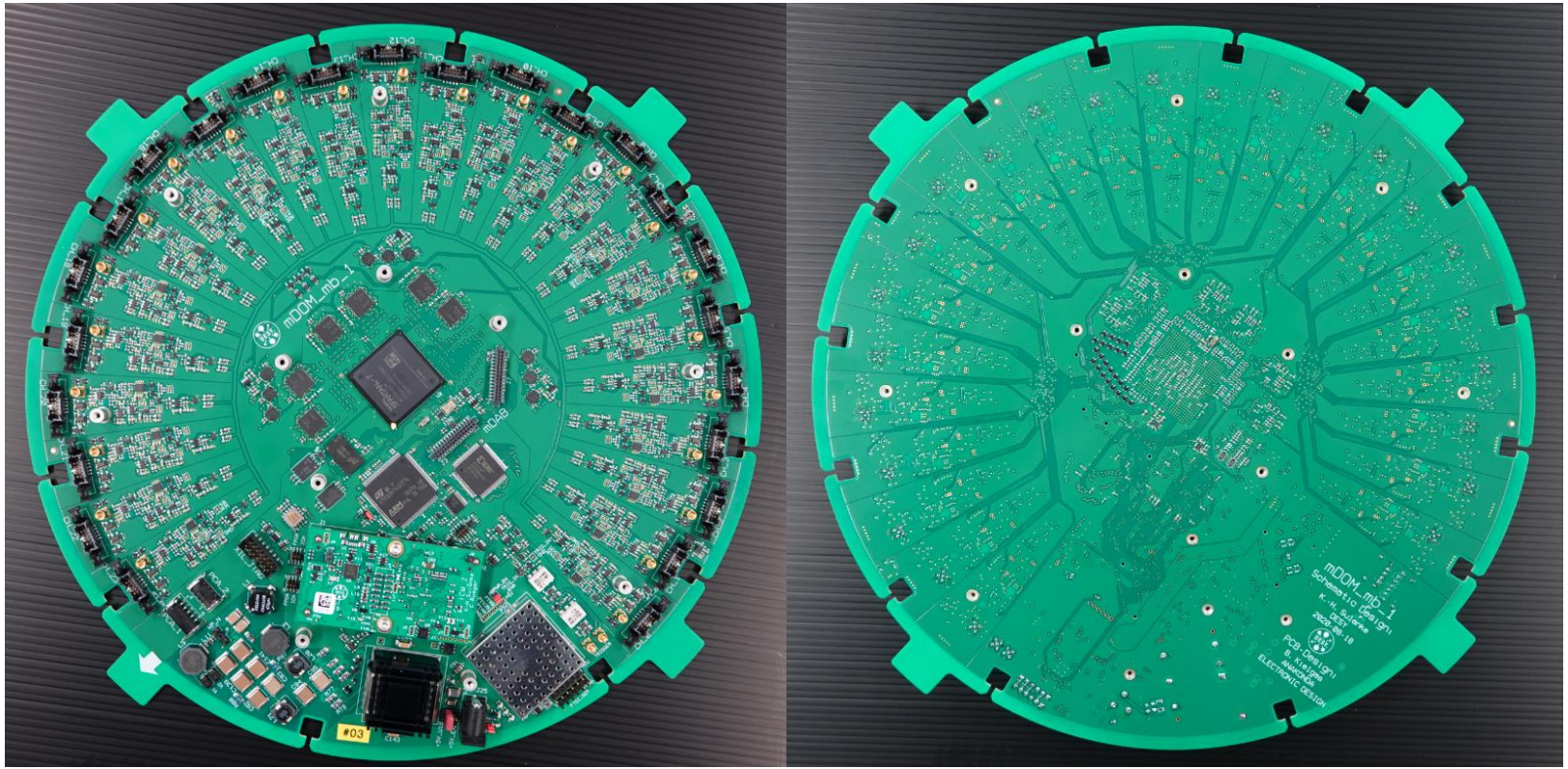
December 2020

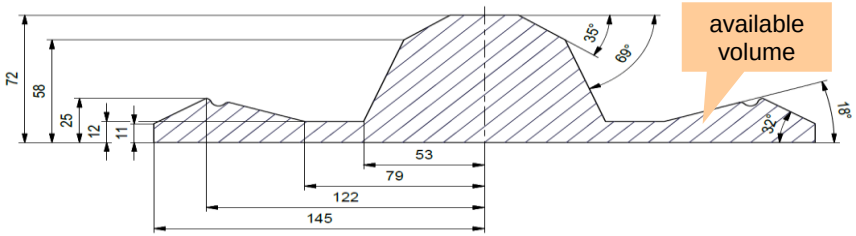
mDOM Mainboard Rev.1

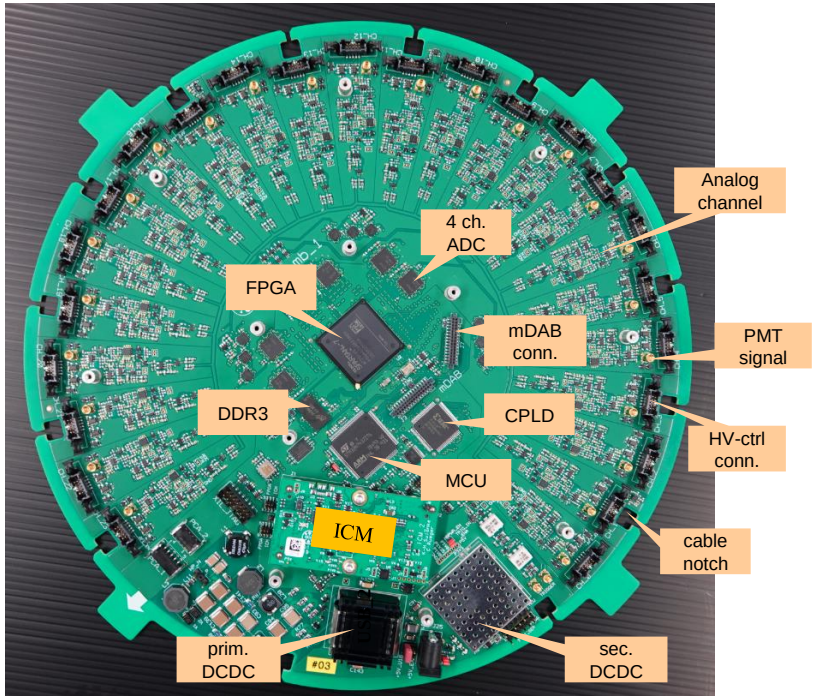
available volume



mDOM Mainboard Rev.1

- PCB routing by Brigitte Kielgas, Anakonda GmBH
- Assembled by Mandy Hemp & colleagues (DESY workshop)
- 8 layers, 1.6 mm thick
- 24 analog sectors, 11.25°
- 1 „noisy“ sector, 90°
- notches for lower sphere – cabling
- ➢ all cables plugged from the top side



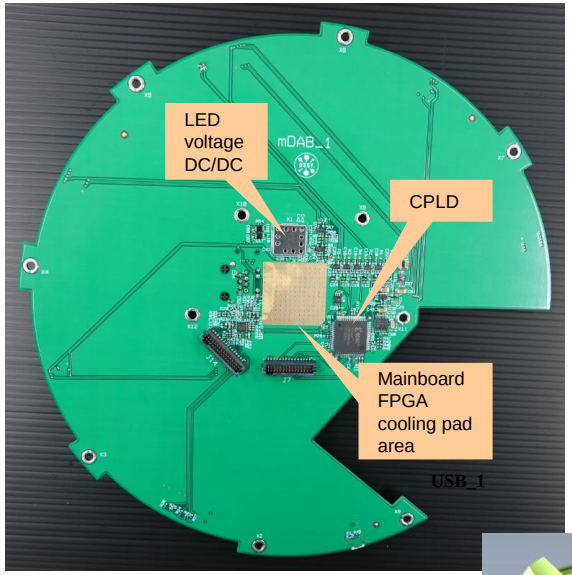


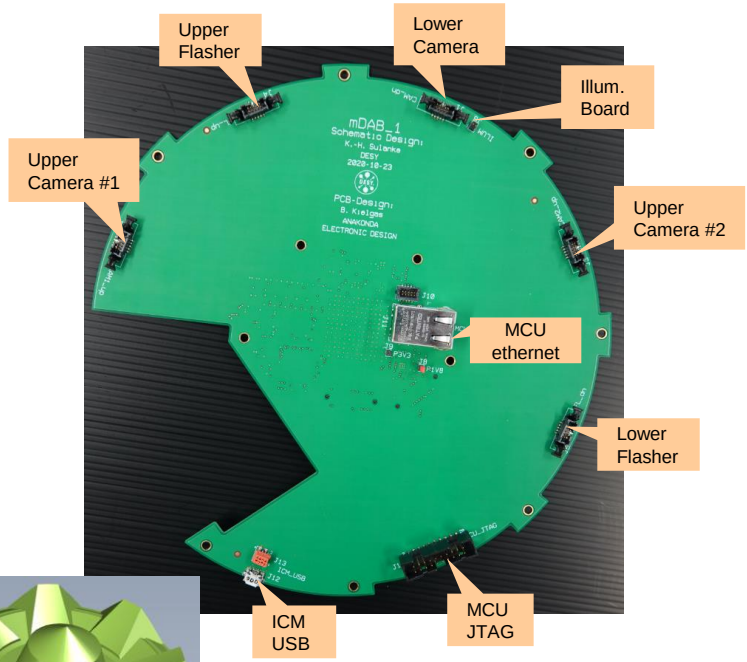
FPGA

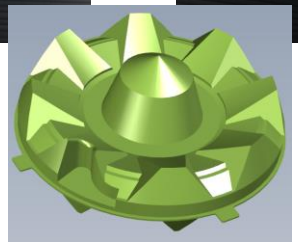
- Xilinx Spartan 7, XC7S100, BGA, 676 pins
- Firmware by Aaron Fienberg
- Rev1
  - DAC setting
    - ADC baseline
    - Trigger threshold
    - Test pulse
  - 24 ADC channel readout
  - ADC sampling rate of 125 MSPS (max. possible)
  - …

mDAB Rev.1

- PCB routing by Brigitte Kielgas, Anakonda GmBH
- 4 layers, 1.6 mm thick
- Most parts on bottom side
- ➢ all cables plugged from the top side



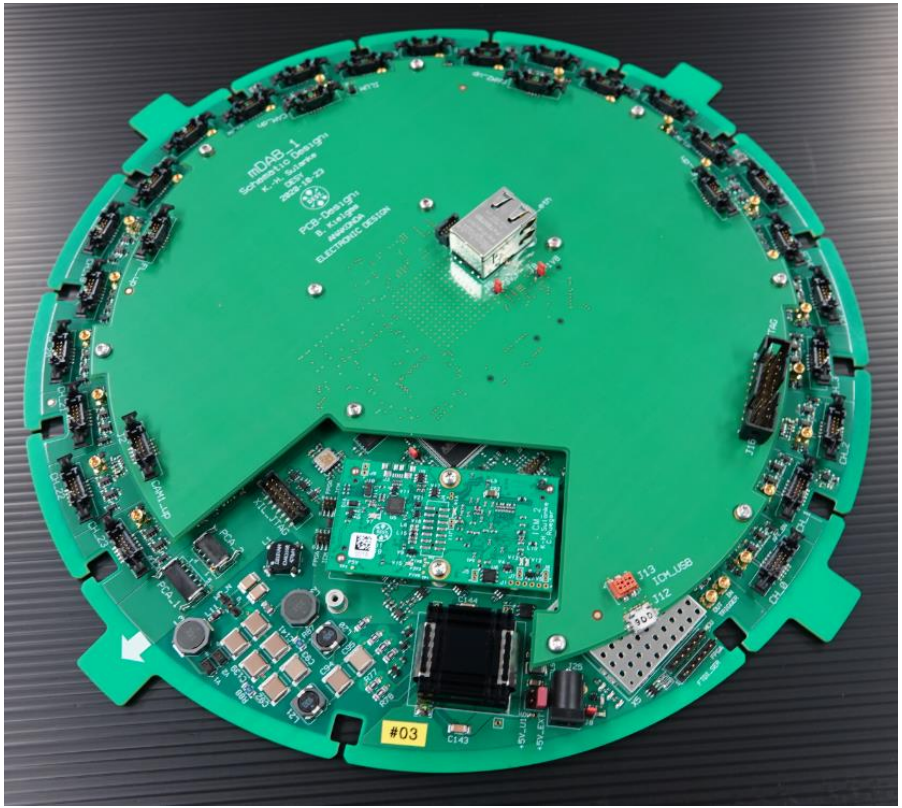




- Connectors on the top side positioned in the „hills“ of the 3D available-volume-model

Mainboard – mDAB Sandwich

- Increased stiffness
- Shielding of AFE
- PMT protection against noise, caused by the mainboard
- Mainboards FPGA cooling (required?)
- Mainboard protection (assembly phase)



Successfully tested so far

- power supplies
- Full JTAG chain, Mainboard_FPGA -> ICM_FPGA -> HV-ctrl_CPLD -> mDAB_CPLD
- comm. to FPGA through ICM and via local UART connector
- comm. to MCU through ICM
- DOM-ID readout
- AFE channel on / off by CPLD (by loading different images)
- AFE preamplifier (by scope)
- All ADC channels, tested by Aaron
- mDAB – some mainboard connections,
  - MCUs flash programming

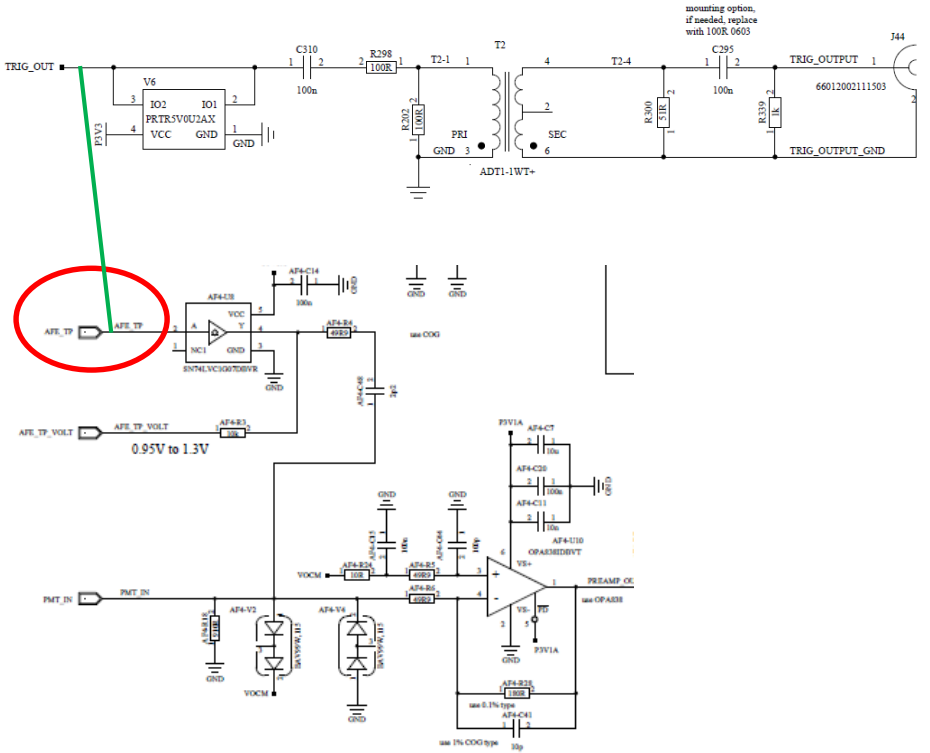
Power Consumption, preliminary

- Firmware Rev.1, w/o PMT bases

rail	current	power	remark	eff.
1.0 V	0.53 A	0.530 W	FPGA core voltage	
1.35 V	0.07 A	0.095 W	DDR3 RAM quiet	
1.8 V	1.11 A	1.998 W	ADCs part and MCU	
1.8 VA	0.97 A	1.764 W	ADCs	
3.3 V	0.44 A	1.452 W	AFE and FPGA bank 3 (slow control)	
		5.839 W	Power consumption after sec. DC/DC	0.90
5 V	1.30 A	6.500 W	Power consumption after prim. DC/DC	0.90
70 V	0.103A	7.210 W	mDOM Power consumption	0.81

Schematic Bug

- Missing the AFE test pulse sources (FPGA outputs)
- Wired connection of TRIG_OUT to channels 0..3 as workaround



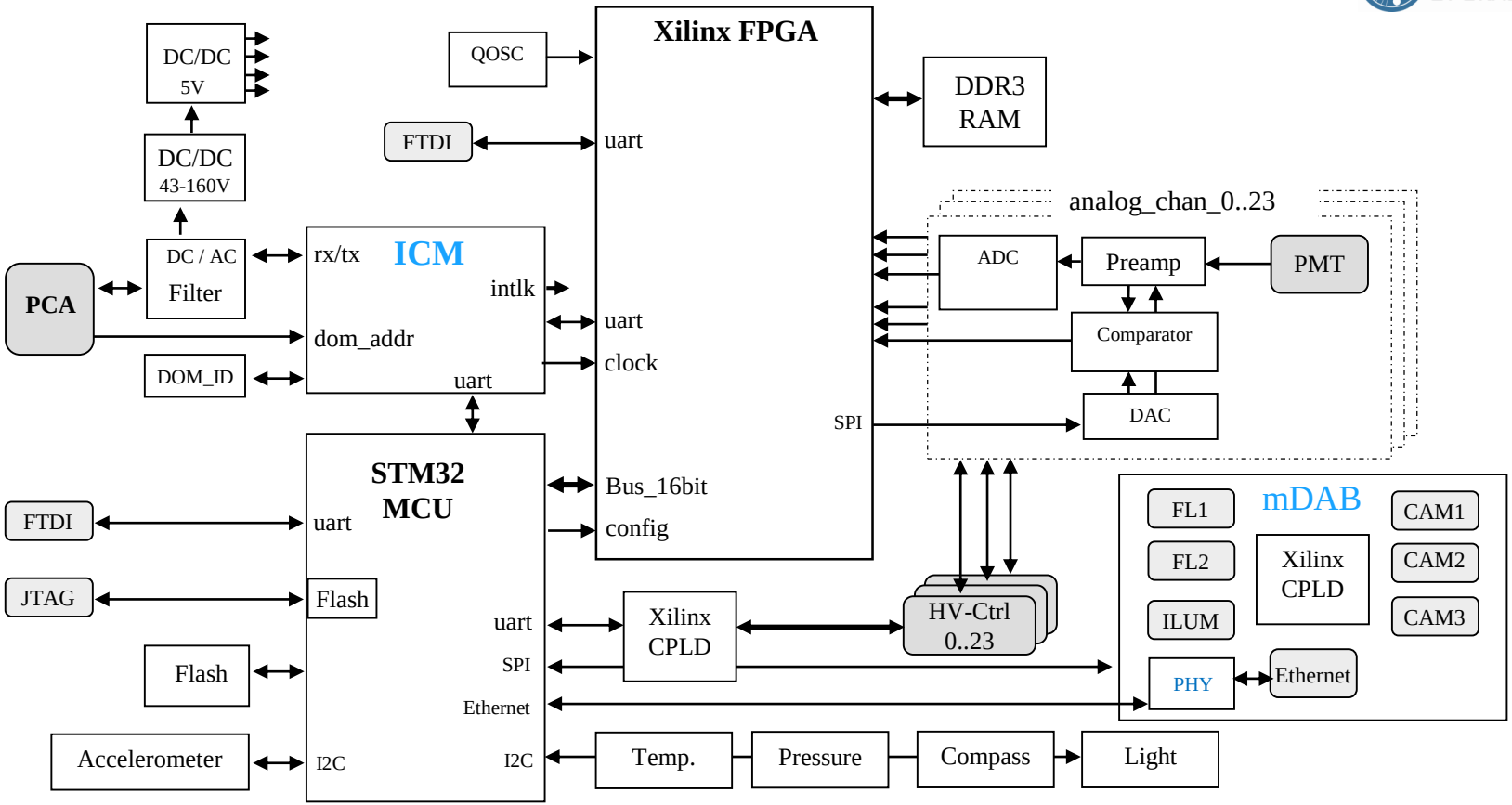
Assembly Status and Distribution

- 12 mainboards assembled
  - 3 of them roughly tested
- 1 mDAB assembled
  - 11 more will be ready next week
- Distribution planned:

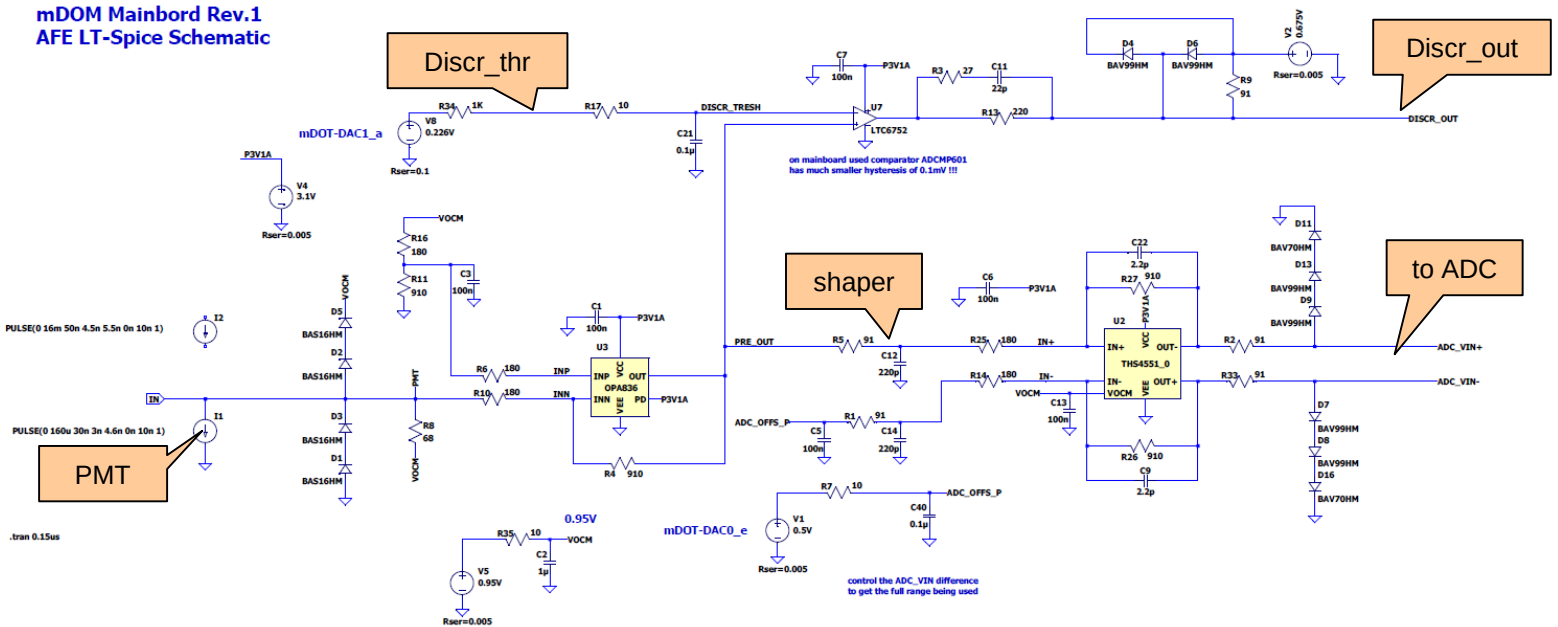
Qty.	Destination	Req. Date	Revision / Requirements
1	PSU	ASAP	Firmware development
2	WIPAC	ASAP	Software development and remote test system
2	DESY		general testing
2	DESY		STF development
1	Aachen		Development of PMT Acceptance Testing

back up slides

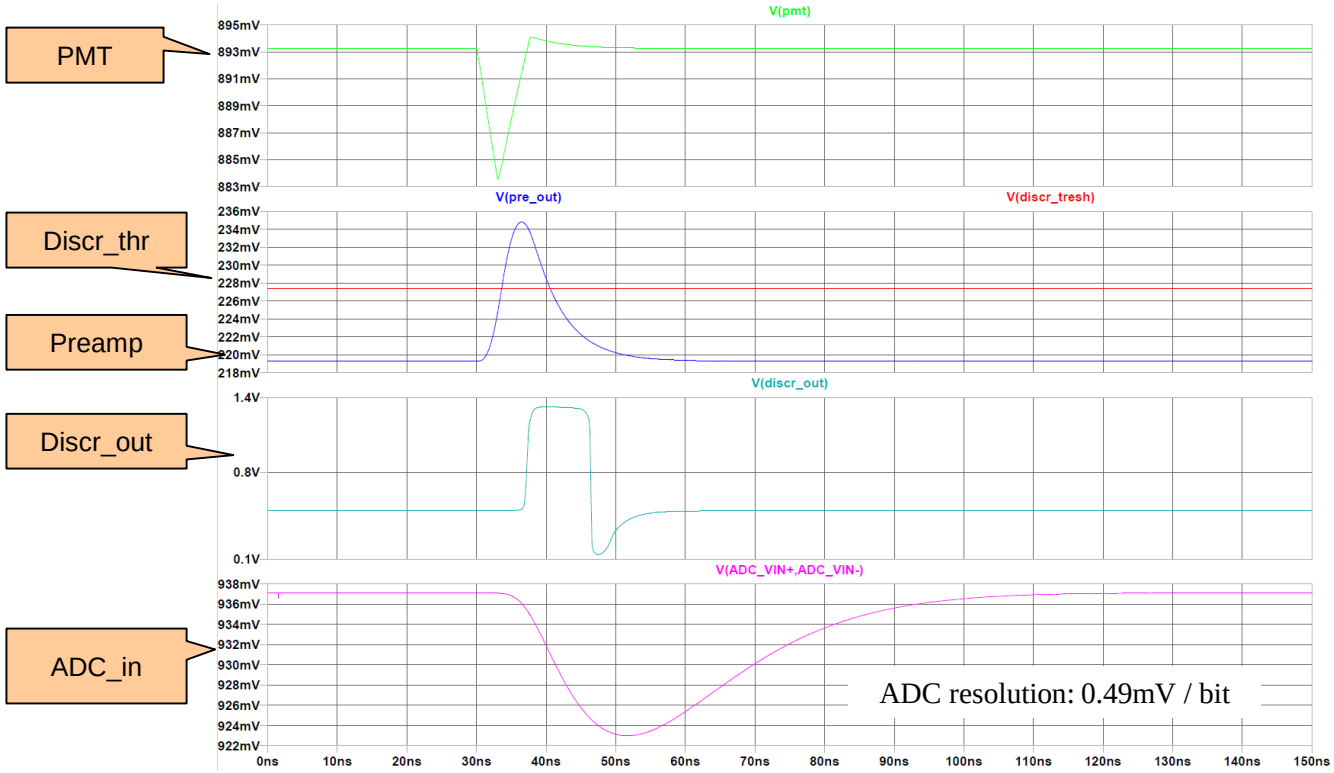
mDOM Mainboard Blockdiagram



AFE channel, simulation (LTspice)



1 SPE input signal, simulated



~100 SPE input signal, simulated