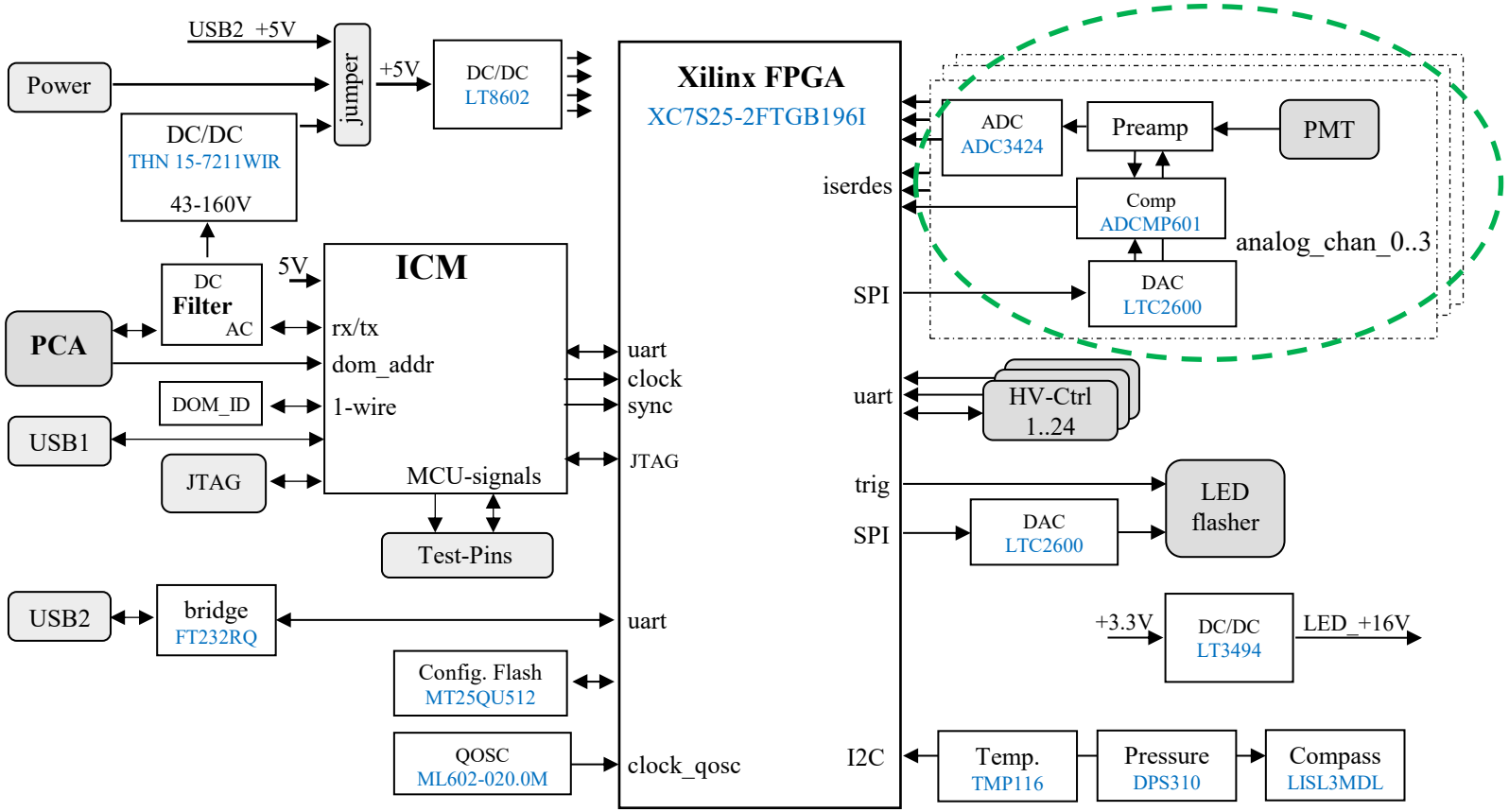
Front End Design for the mDOM Mainbord

Kalle Sulanke
April 2020

Introduction

- mDOT = mDOM Testboard
- 4 different analog channels, optimized for very low power
  - Trade off with bandwidth
- ADC Sampling rate is 100MSPS (max. is 125 MSPS)
  - Pulse shaping required
- At channel #0,2,3, looking for:
  - ADC baseline noise
  - Minimum signal level required, to get a trigger
  - Dynamic range
  - Power consumption

mDOT Blockdiagram

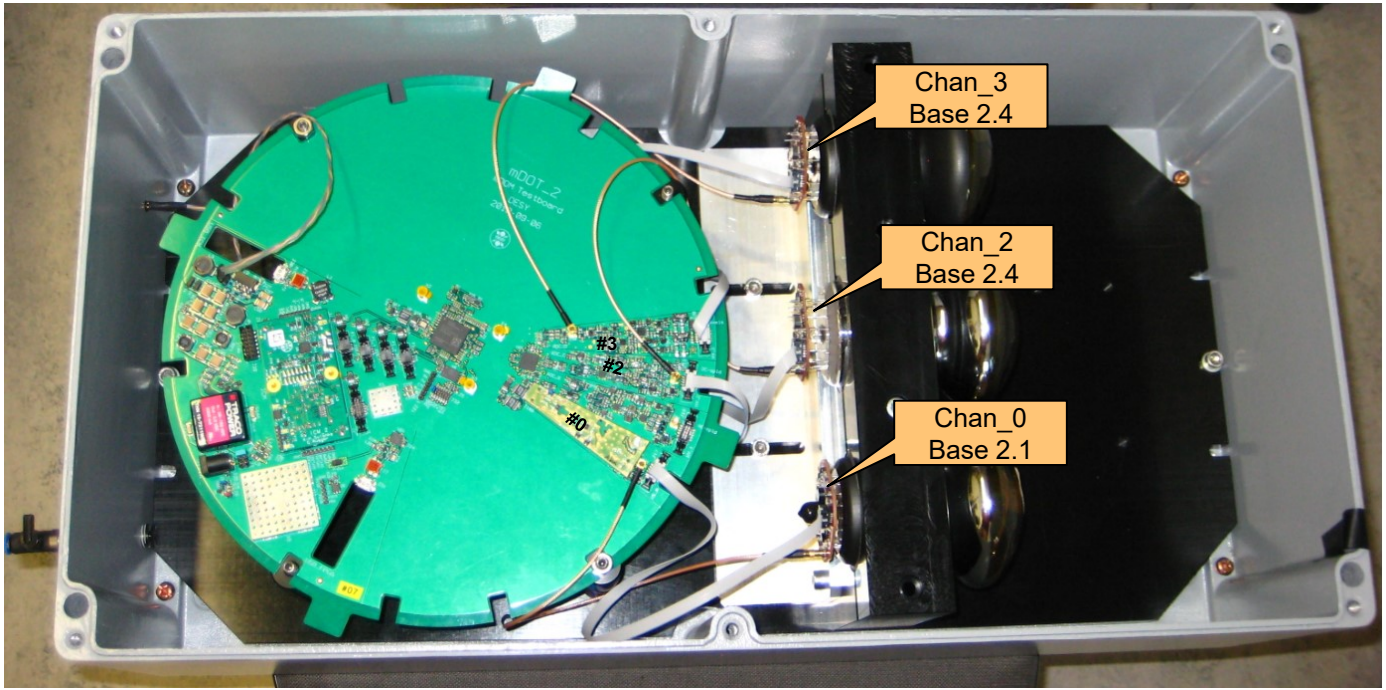


Test Setup

- mini_Fieldhub + 1.5m cable + mDOT
- mDOT firmware by Tyler Anderson, Aaron Fienberg
  - Python scripts by Aaron Fienberg and Timo Karg
- Pulse generator Stanford DG 645, to get faked PMT pulses
  - Plus attenuator, 0 to 40 dB
- Tektronix scope MDO3104
- Self made isolating analog coupler, amplitudes from 1mV pk to 0.35V pk
  - Based on RF transformer ADT1-1WT (0.4 to 800MHz bandwidth)
  - To avoid DC/DC noise by capacitive coupled ground loops
- Massive, light-tight aluminum box (BERNSTEIN CA-480)
  - 600 x 310 x 180 mm, 4 mm wall thickness

Test Box

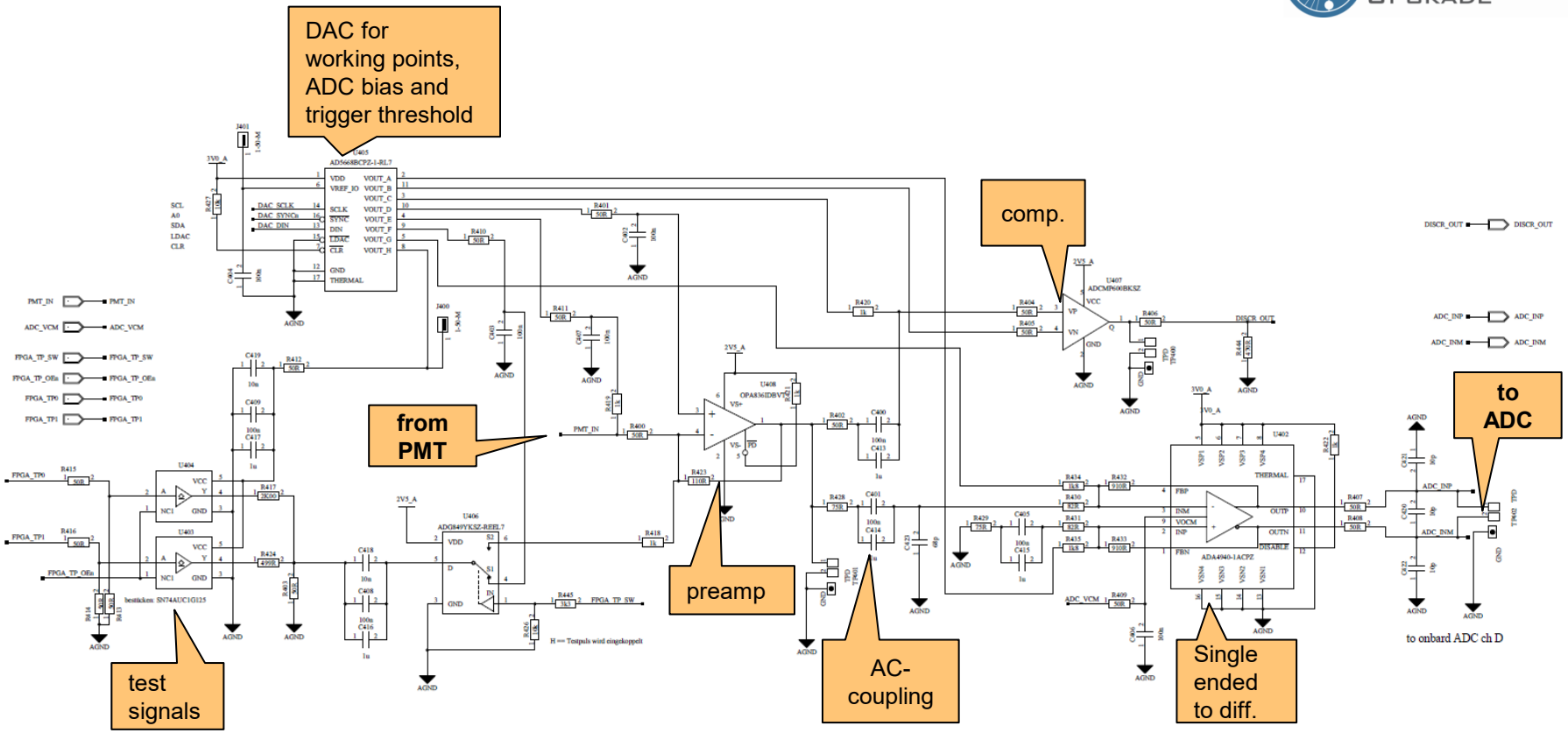
- channels 0, 2, 3 connected, setup also used for the first cold tests



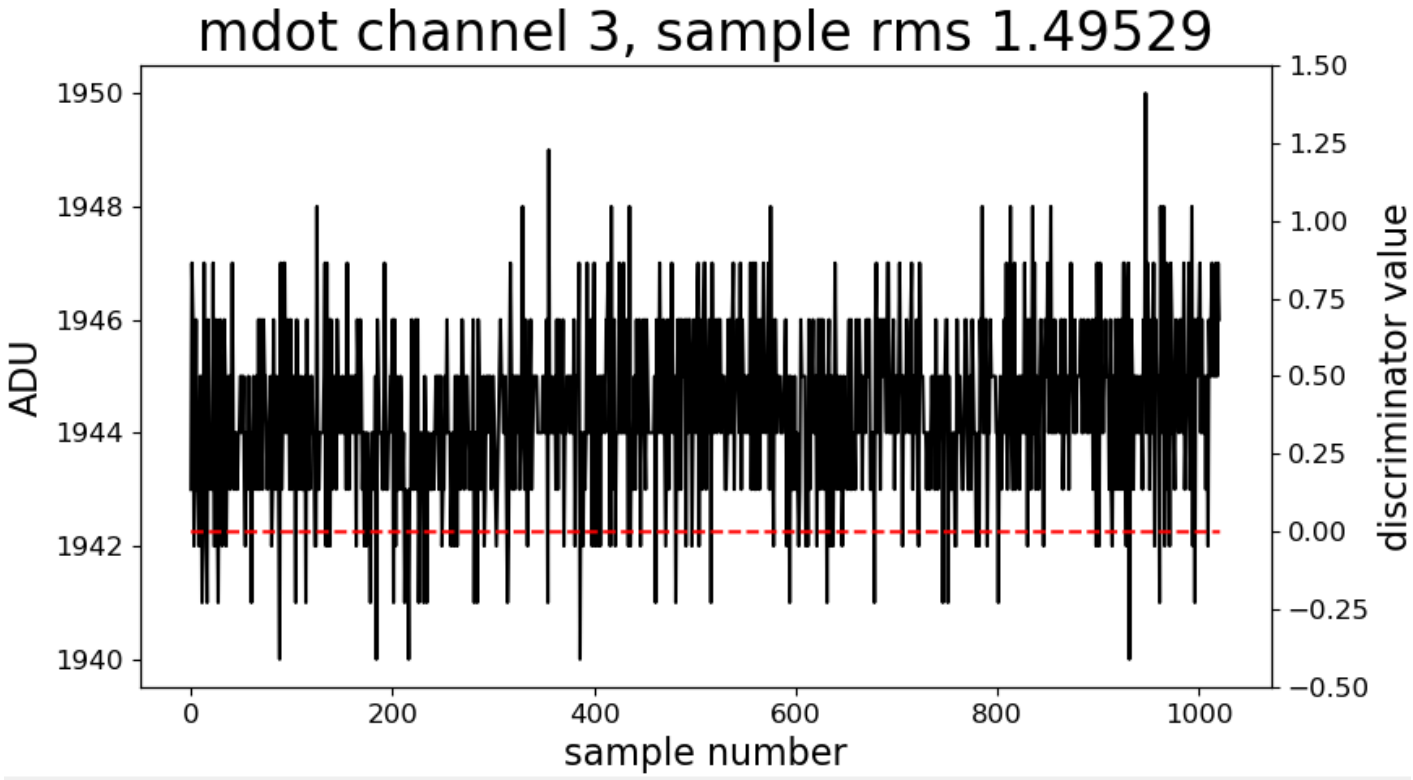
Original mDOT Channels #1, #2

- Original channels #1 and #2 have a bit weak preamplifier stages
- Therefore channel #2 modified
- These modification resulted in the design of channel #0 (piggyback)
- Shown test results basically focus on channel #3 and #0
- Channel #3 designed and simulated by Axel Kretschmann
  - For optimization, several test boards have been used in the past

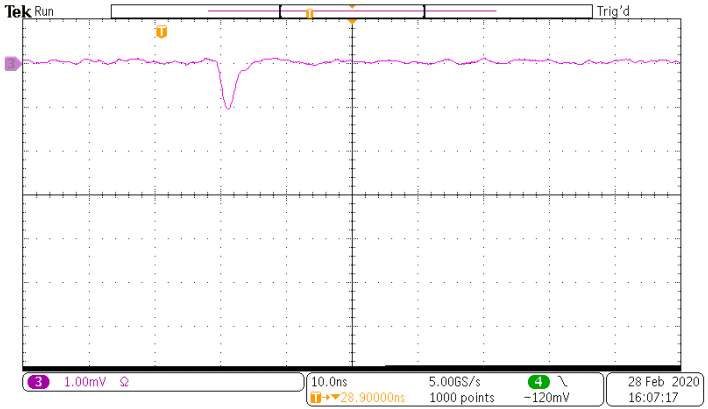
Channel #3, Schematic (by Axel Kretzschmann)



Channel #3, typical noise, with open input

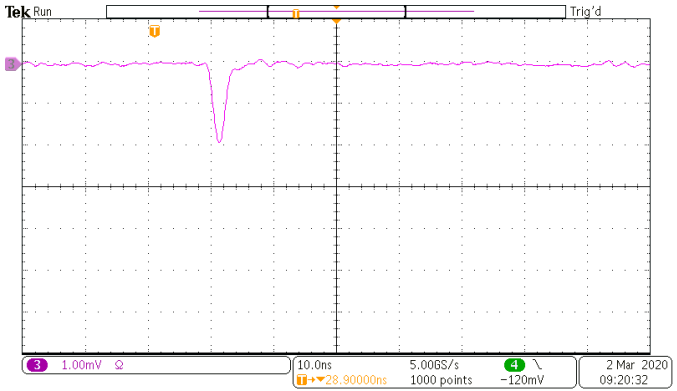


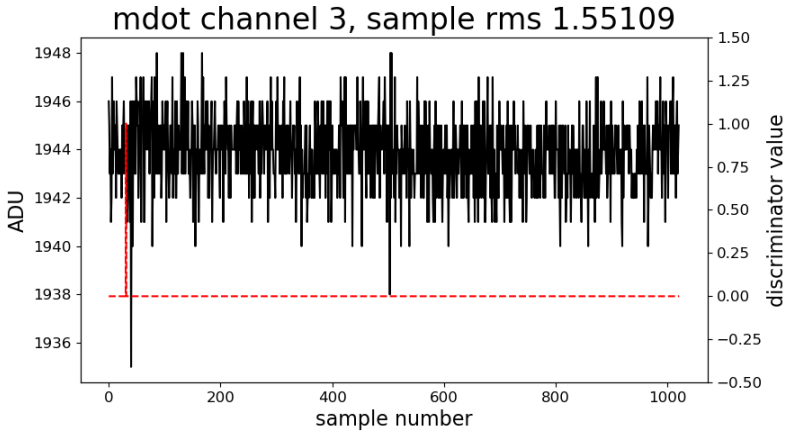
Channel #3, 1mV input

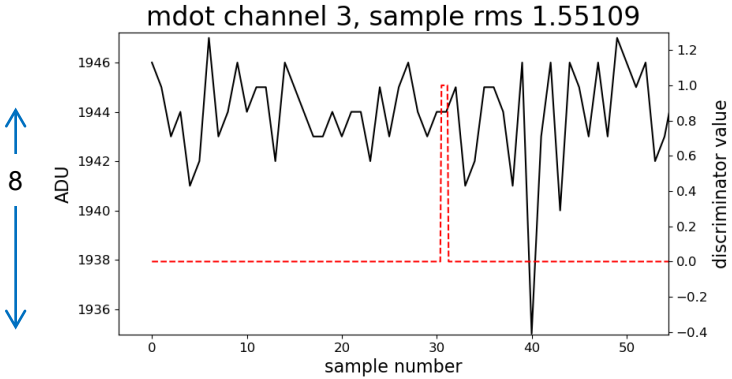


- No safe trigger condition found

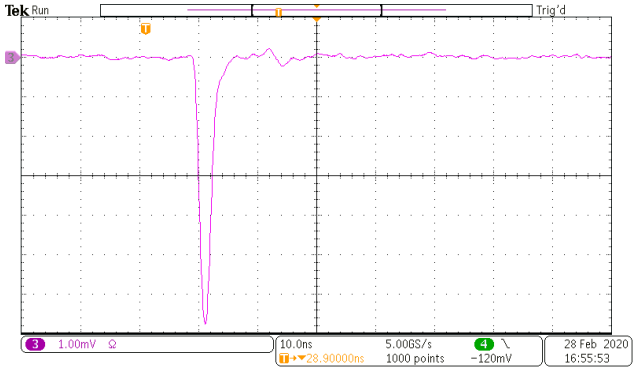
Channel #3, 2mV input

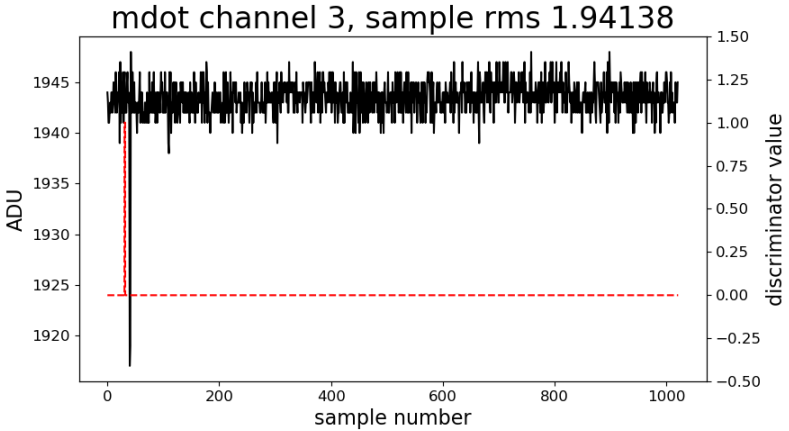


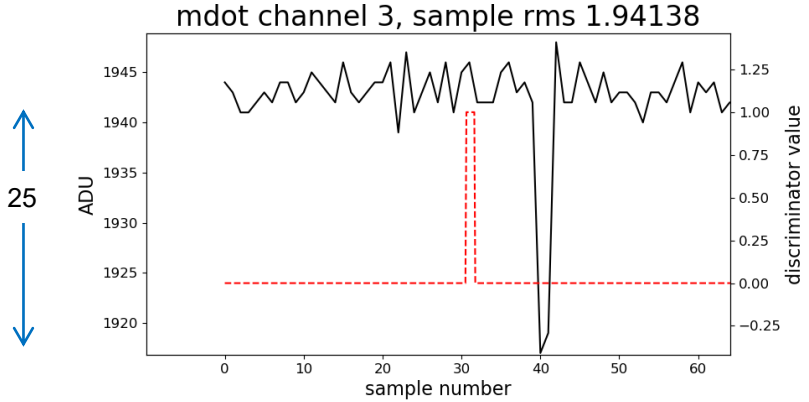




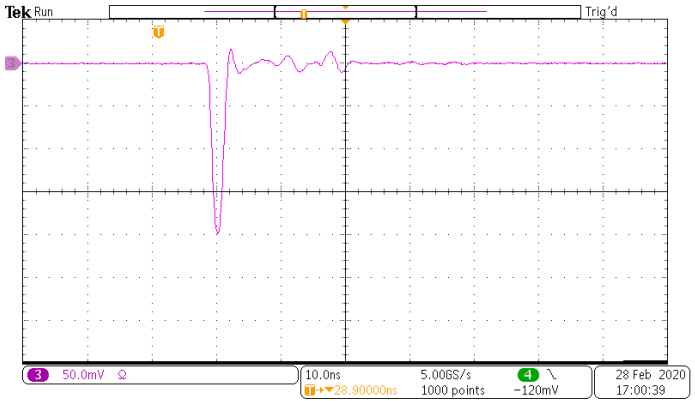
Channel #3, 7mV input

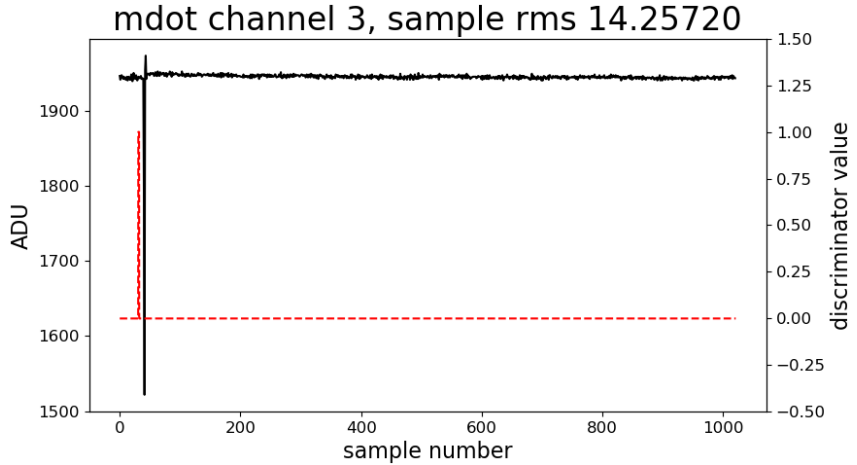


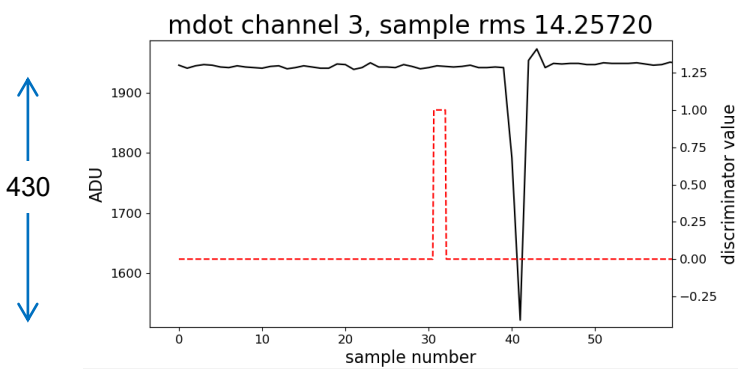




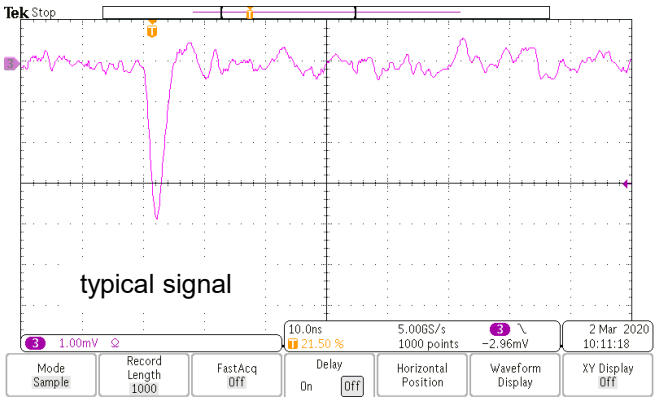
Channel #3, 200mV input

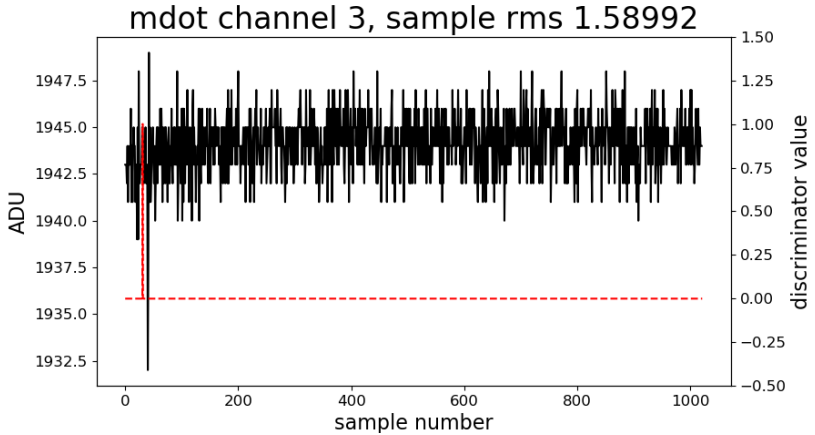


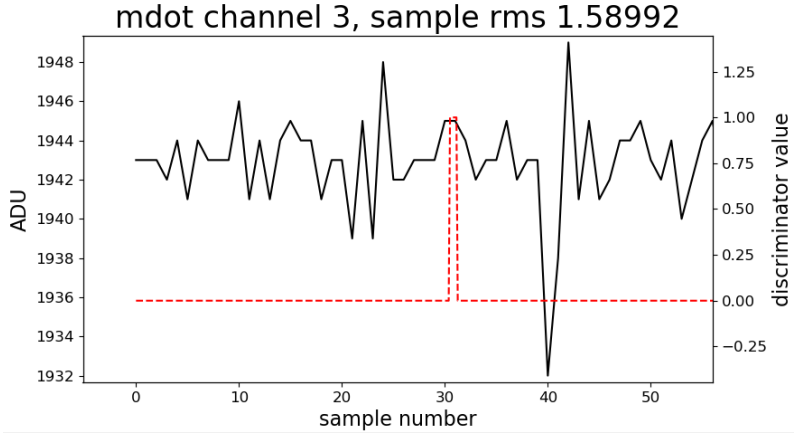




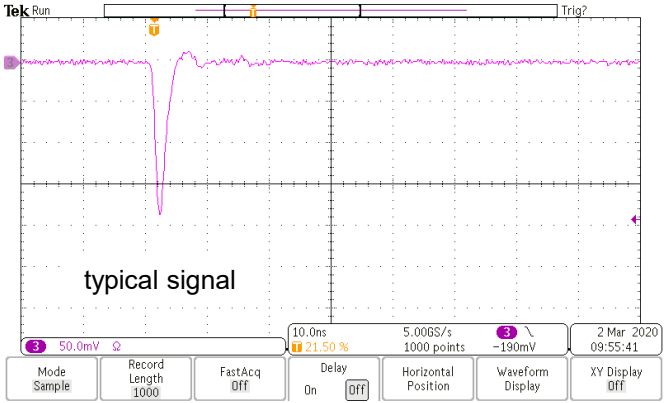
Channel #3, 4mV PMT signal, HV = 567V

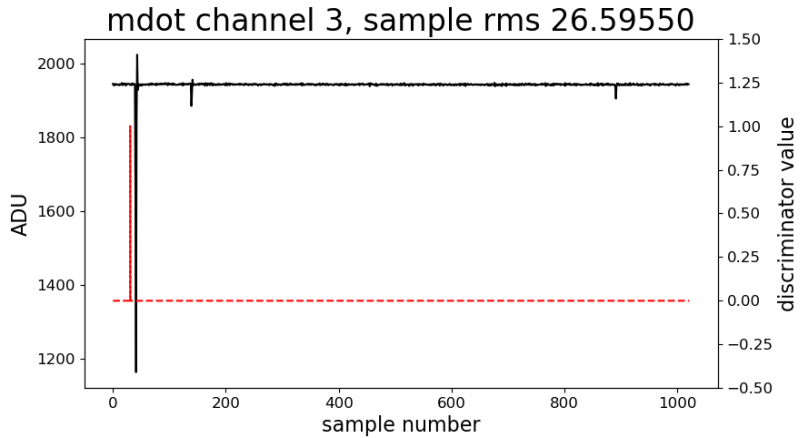


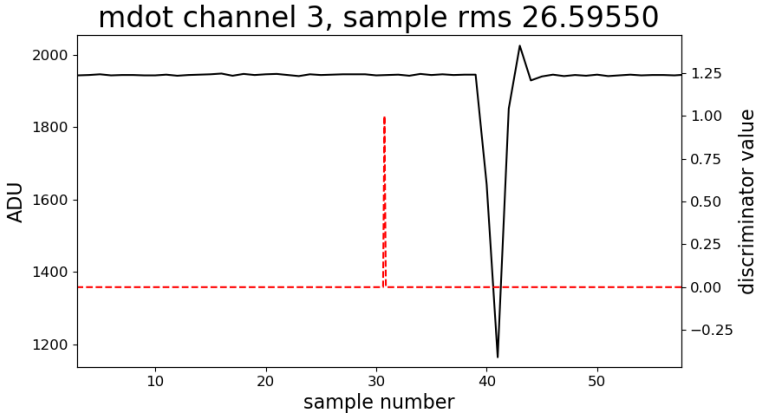




Channel #3, 200mV PMT signal, HV = 846V

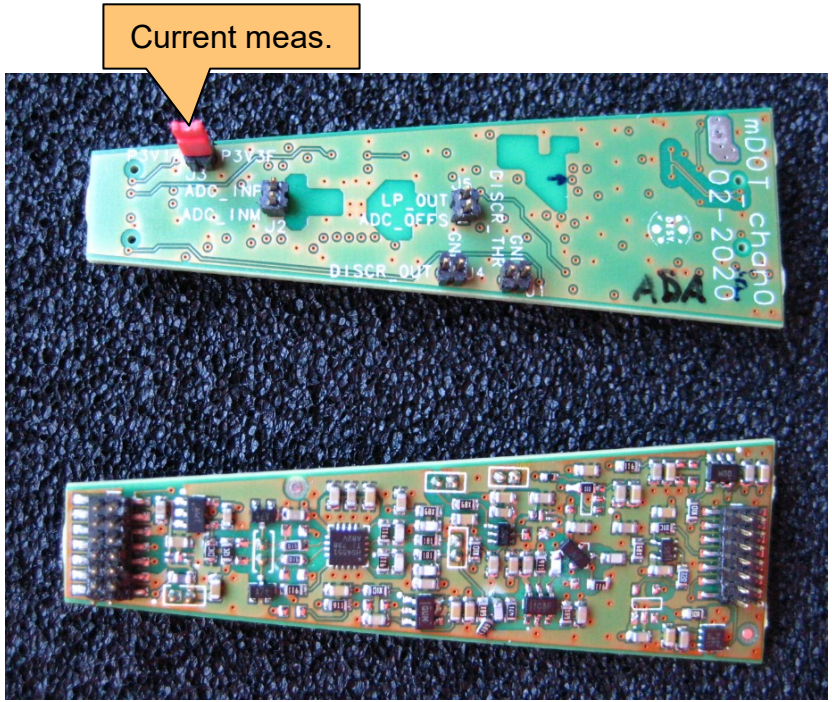




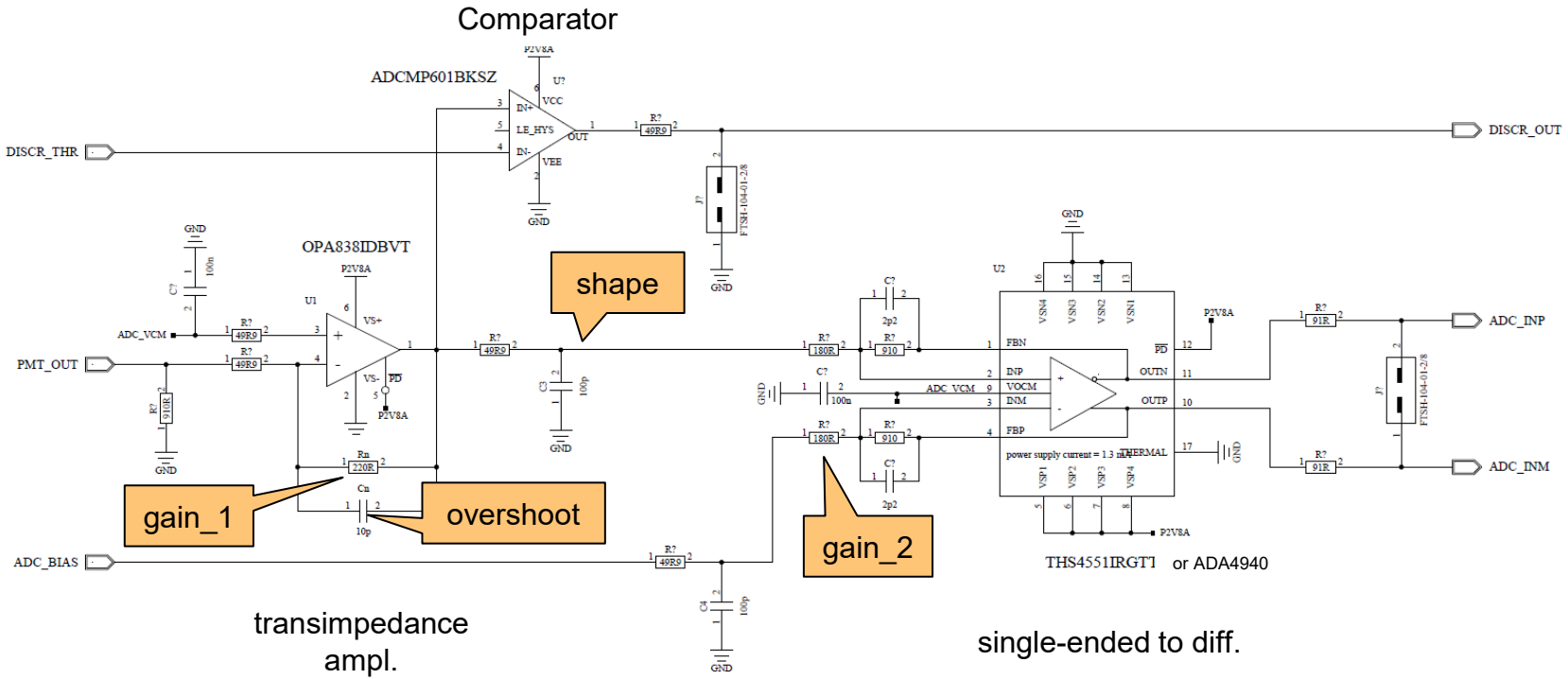


Channel #0, the Piggyback Module

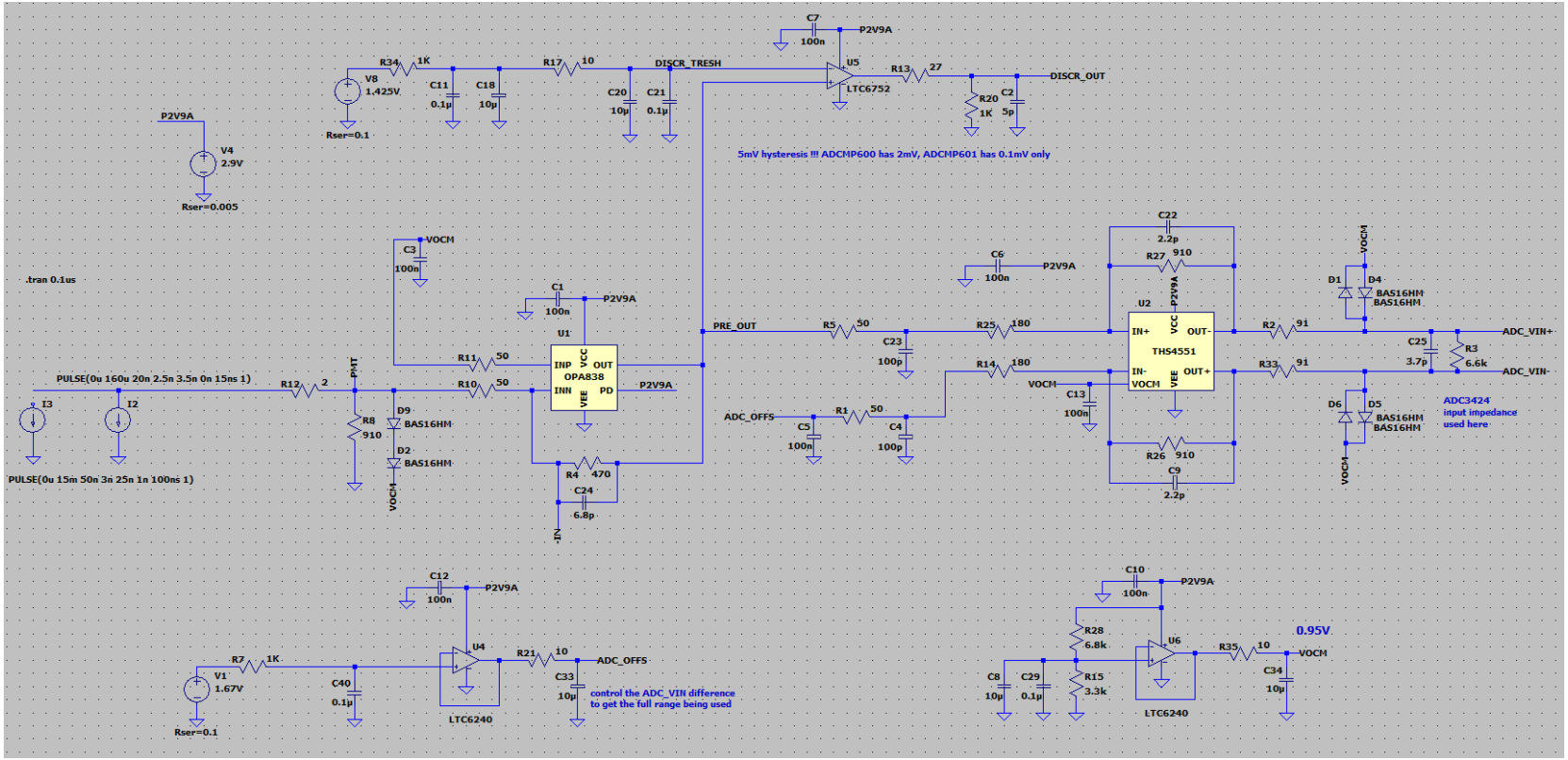
- PCB design by Carola Rueger, assembled by Mandy Hemp (DESY workshop)



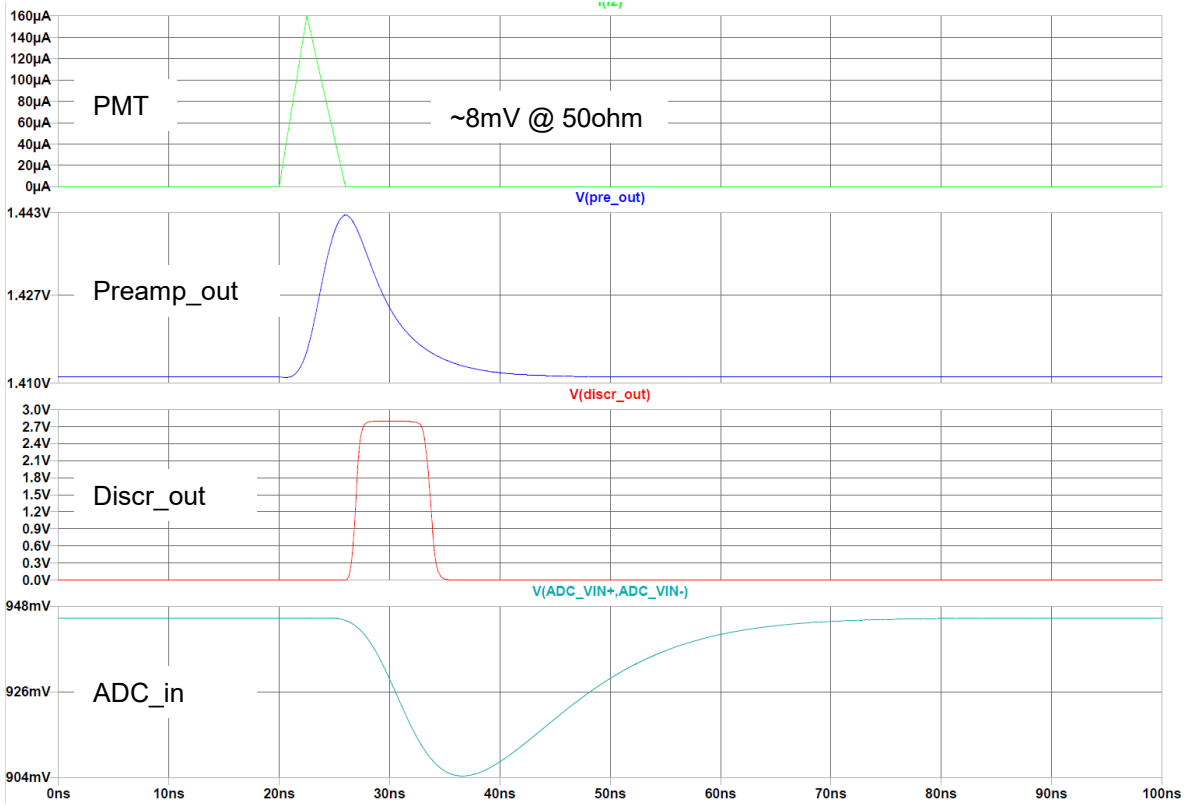
DC-coupled Channel #0, basic Schematic



LTSpice Schematic used

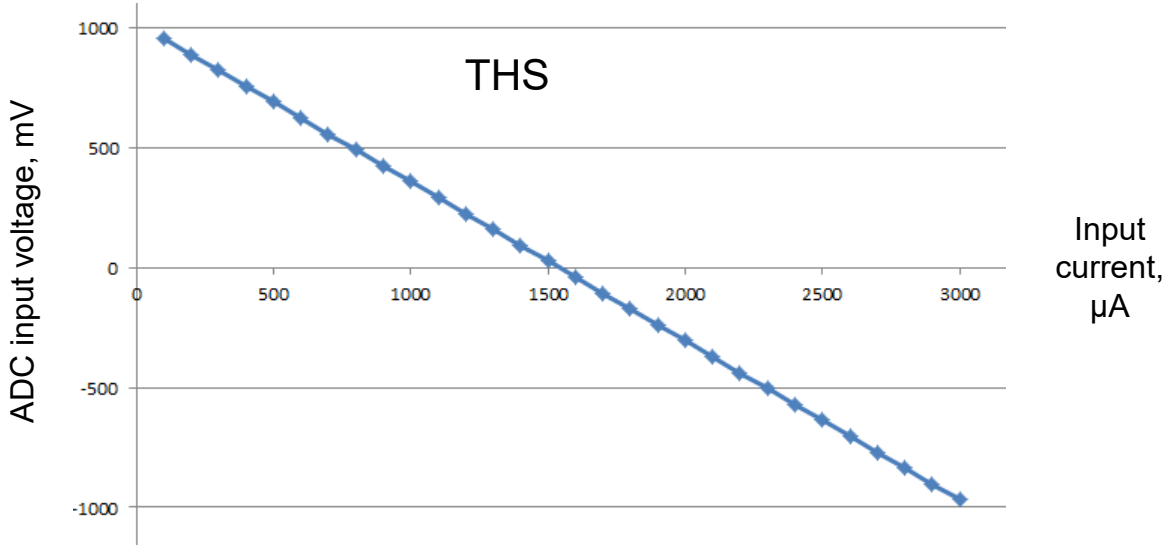


SPE Signal, LTSpice Simulation Results



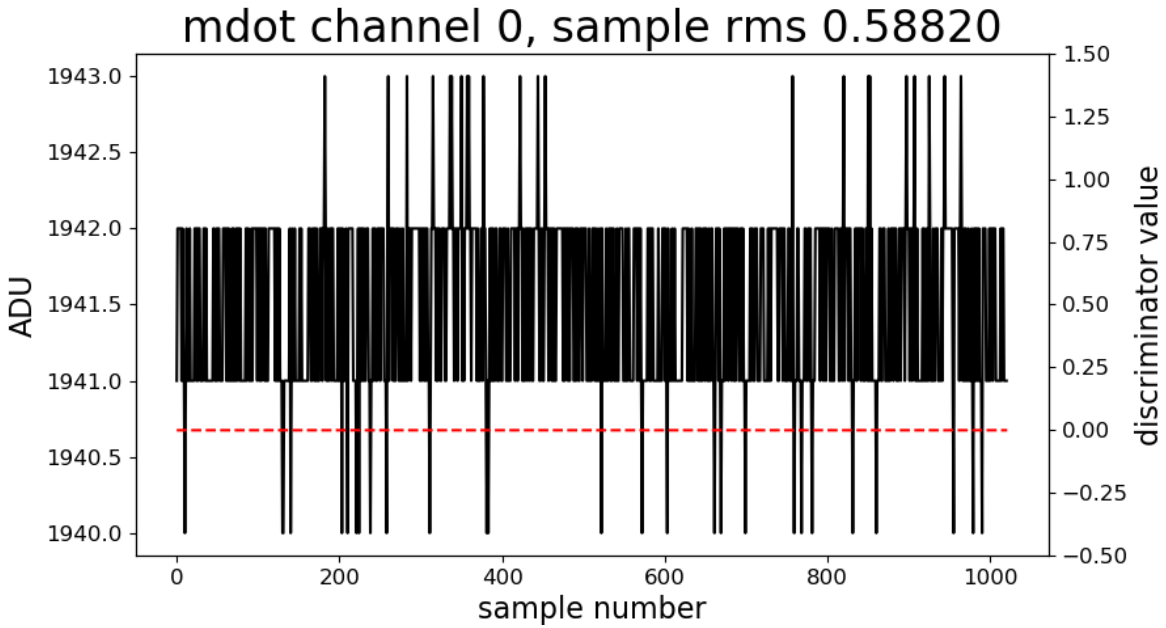
DC Linearity Test

- Modules „THS“ and „ADA“, (different, pin-compatible opamps in front of the ADC)
- Injecting a DC current 100µA to 3 mA, to get a diff. ADC input voltage of +1V to -1V
- 20K resistor + 0 to 75V power supply as current source
- Voltage vs. current, using two multimeters, …perfectly linear, both for THS and ADA modules



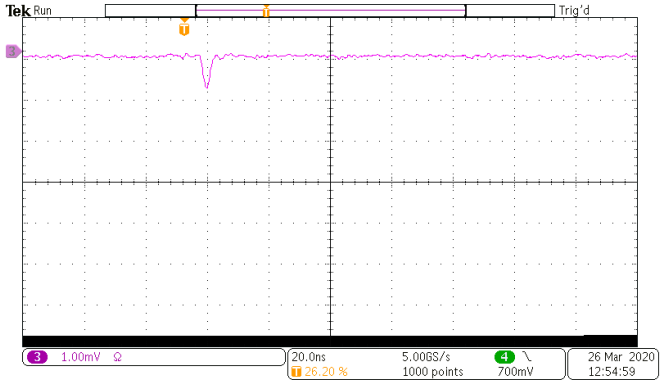
Typical noise, with open input

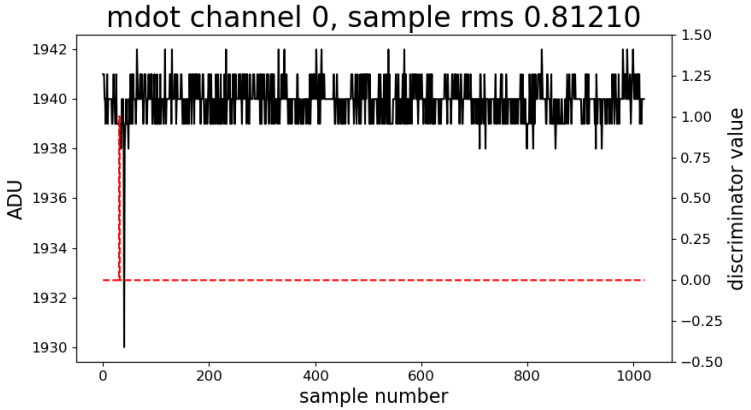
- Using the ADC driver THS4551

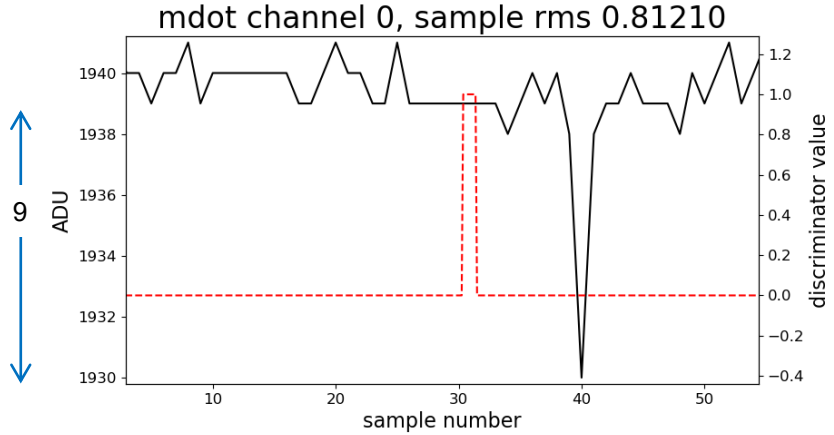


Rin=910R, Rn = **470R**, Cn=6.8p, LP = 51R x **100p**, gain_2 ~ 5, DAC0_e = 44000, DAC1_a = 37200

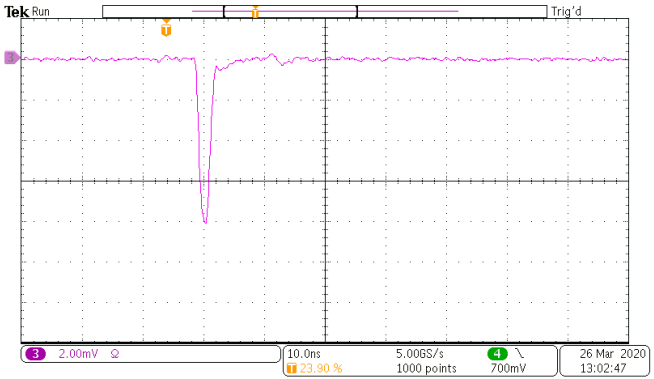
1/10 SPE input (0.8mV pk)

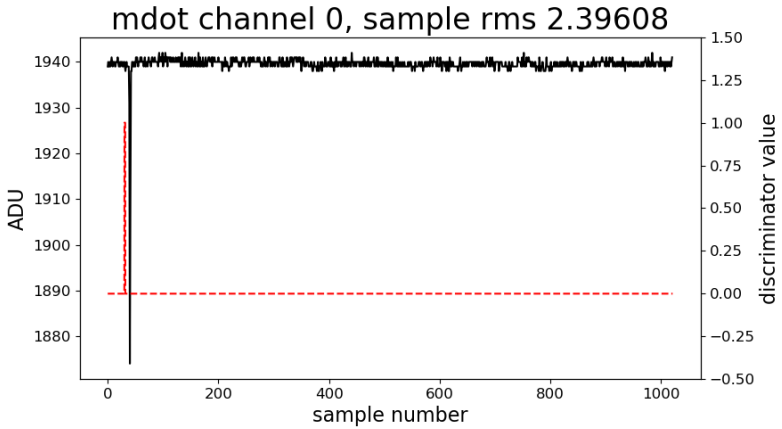




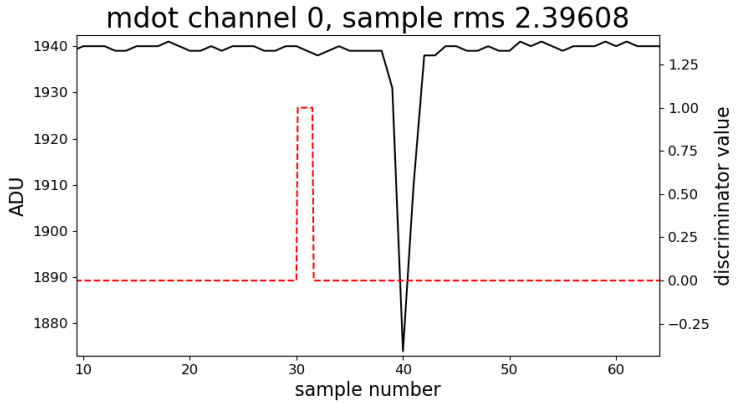


1SPE input (8mV pk)

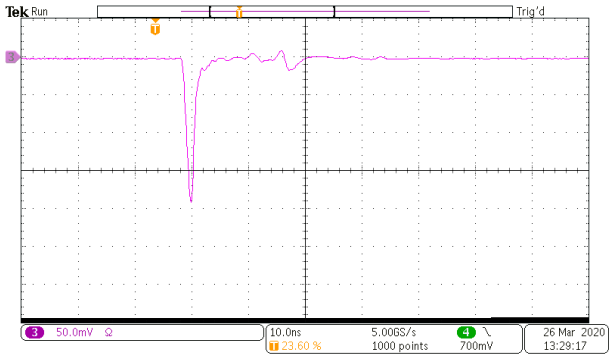


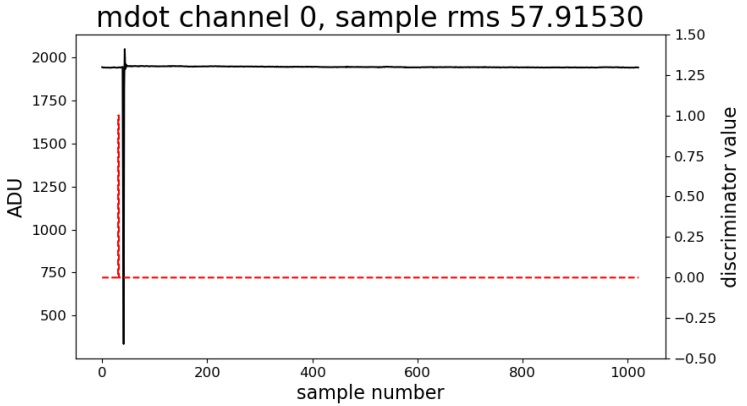


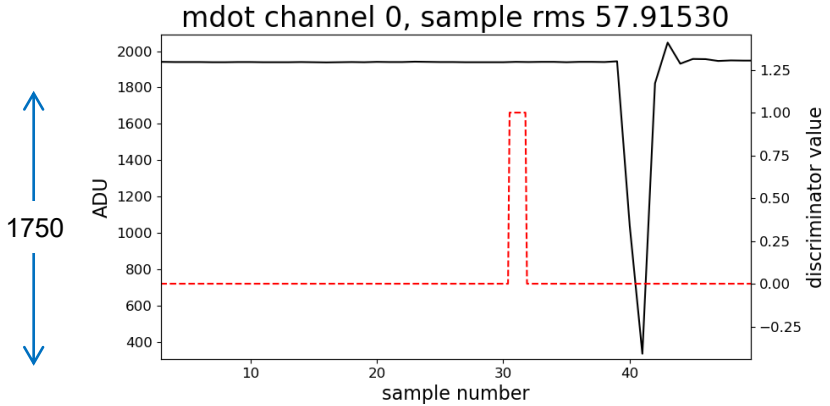
65



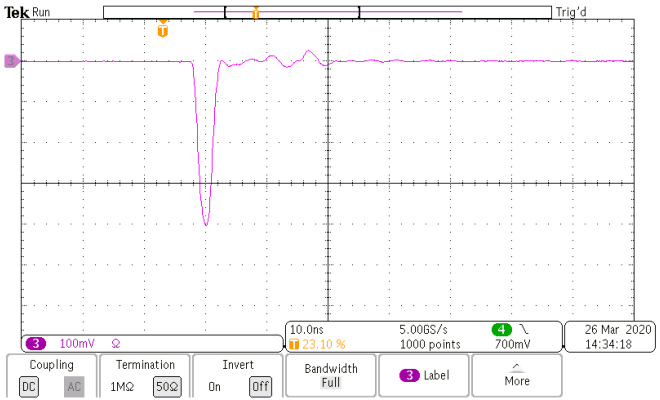
200mV input

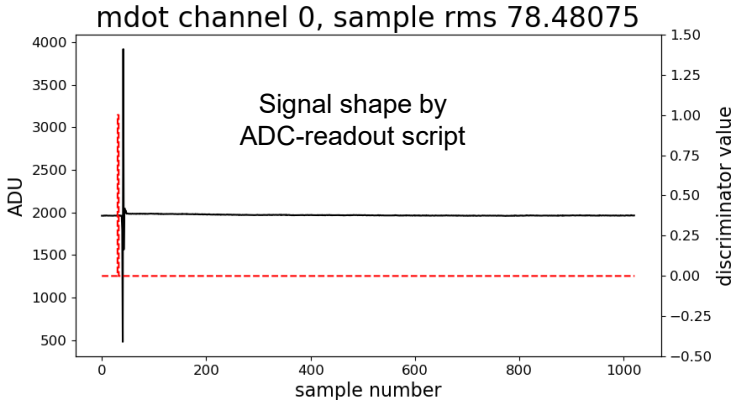

Tek Run
Trig'd
50.0mV
10.0ns
23.60 %
5.00GS/s
1000 points
700mV
26 Mar 2020
13:29:17

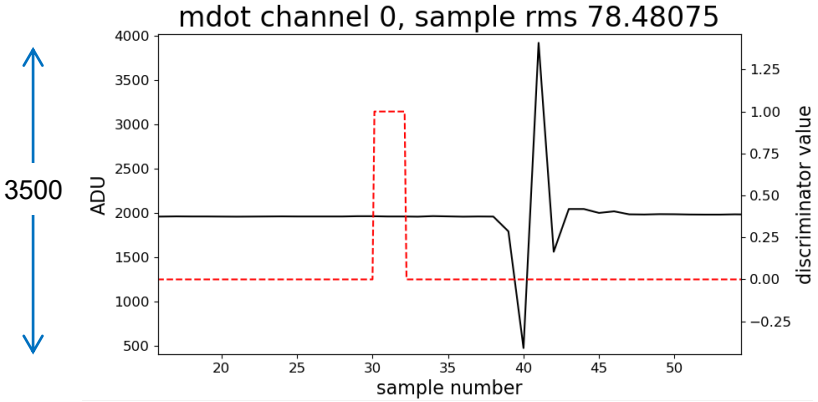

mdot channel 0, sample rms 57.91530
ADU
discriminator value
sample number


1750
mdot channel 0, sample rms 57.91530
ADU
discriminator value
sample number

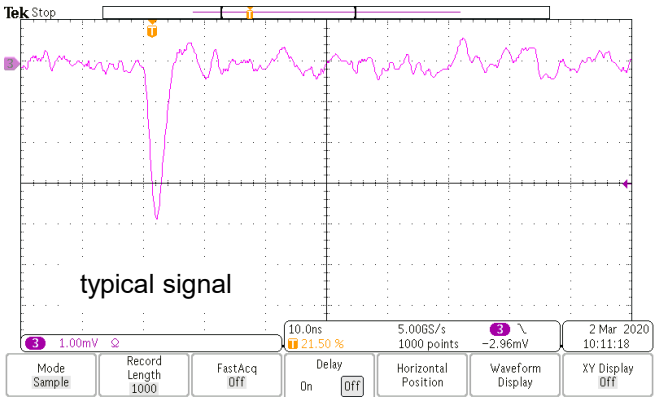
400mV input

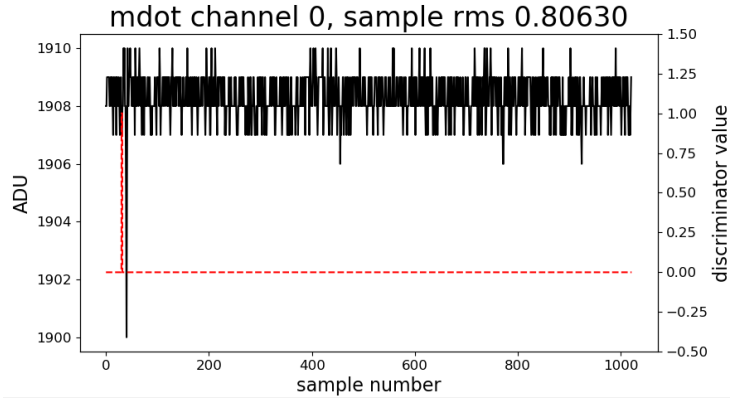

Tek Run
Trig'd
100mV
10.0ns
23.10 %
5.00GS/s
1000 points
700mV
26 Mar 2020
14:34:18
Coupling
DC
AC
Termination
1MΩ
50Ω
Invert
On
Off
Bandwidth
Full
Label
More


mdot channel 0, sample rms 78.48075
Signal shape by
ADC-readout script
ADU
discriminator value
sample number

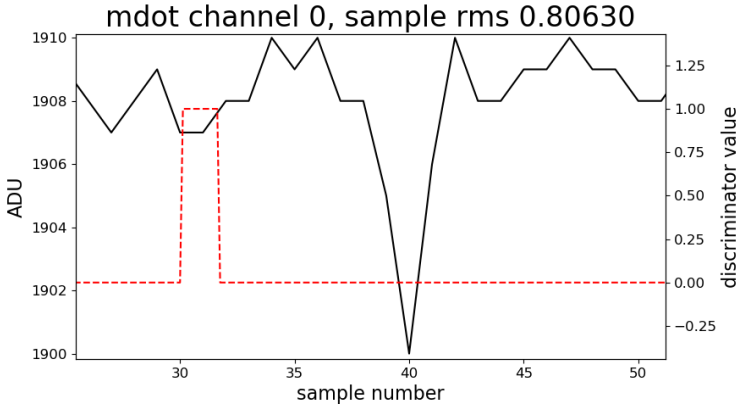

3500
mdot channel 0, sample rms 78.48075
ADU
discriminator value
sample number

PMT signal, 4mV, HV = 566V

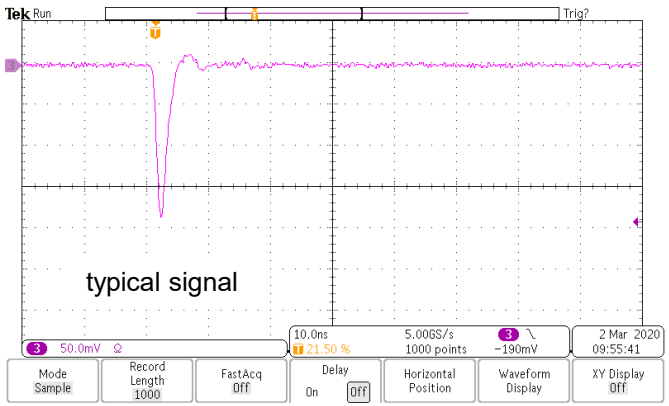


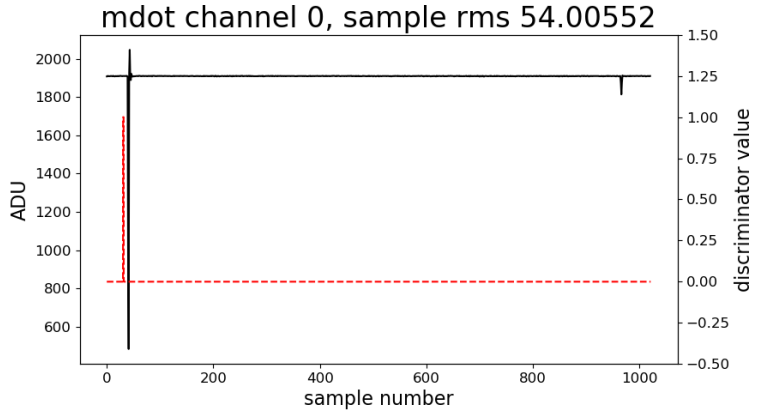


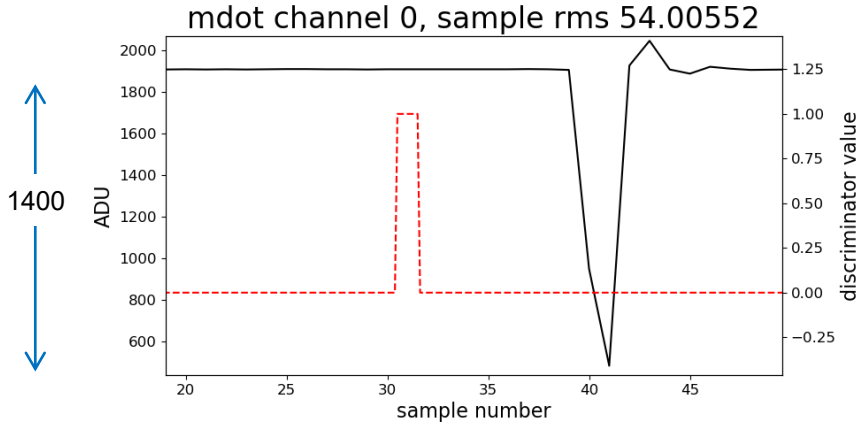
8



PMT signal, 200mV, HV = 846V



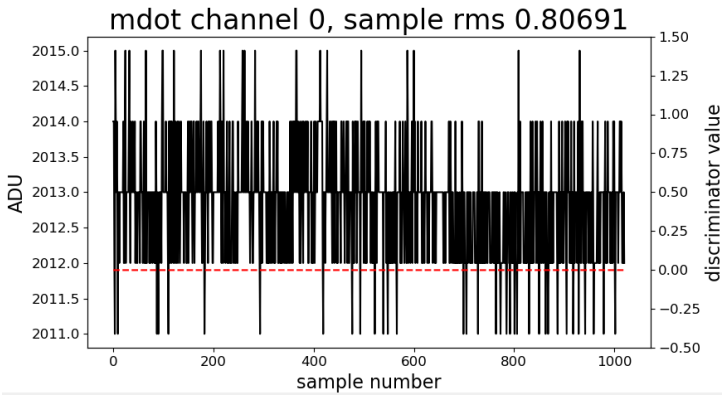




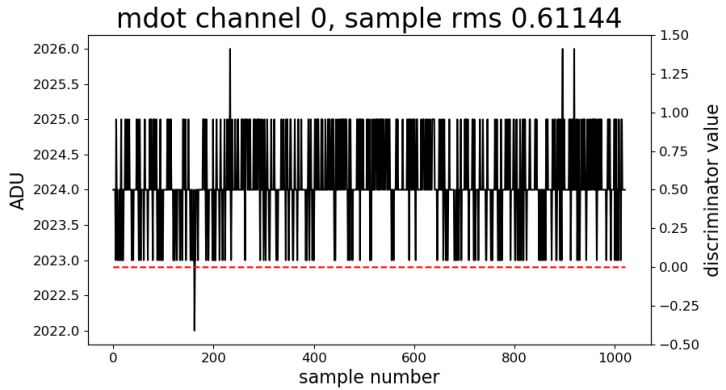
Noise Comparison, Amplifiers THS4551 vs. ADA4940

- Singel ended to diff. Amplifier, ADC driver

ADA4940



THS4551



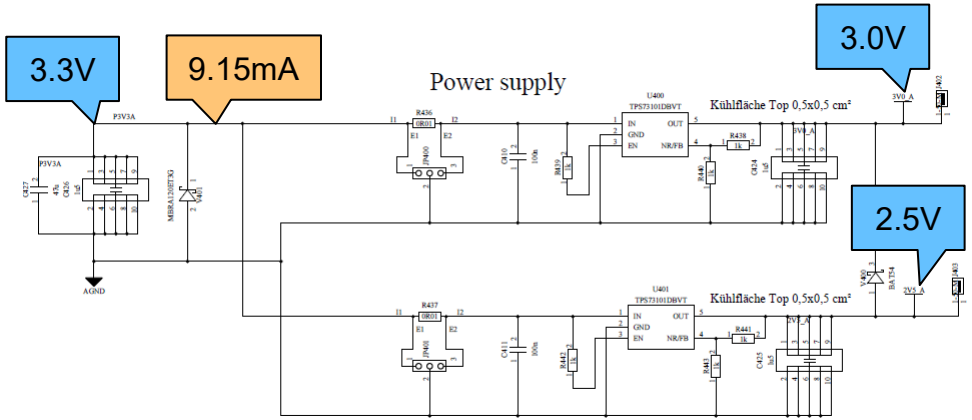
Power Consumption of Channel #3

- Used default DAC settings

  3.3V * 9.15mA= 30.2 mW

- After power supply modification:

  3.0V => **27.5 mW**



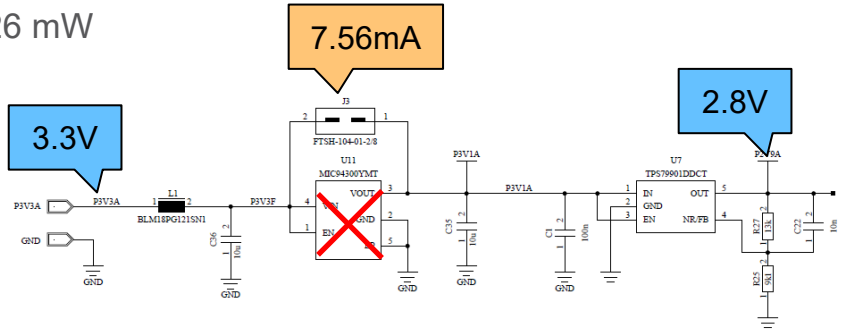
Power Consumption of Channel #0

- with default DAC setting

  3.3V * 7,56mA + 1mW (1/4 DAC)= 26 mW

- After power supply modification:

  3.0V => **23.7 mW**



- mDOM, overall analog power consumption with ADC at 100MSPS:

  6*350mW (ADC) + 24*23.7mW (analog chan.)

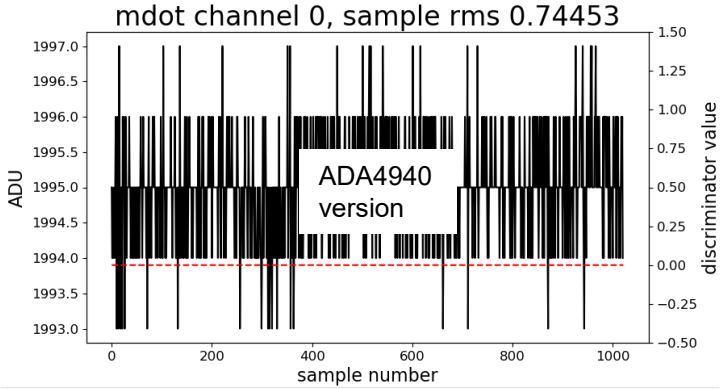
  = 2100mW + 567mW = **2667 mW**

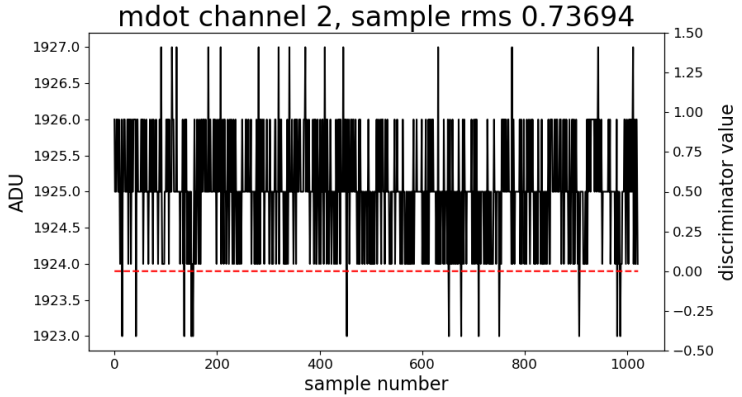
  ~ 111 mW / channel

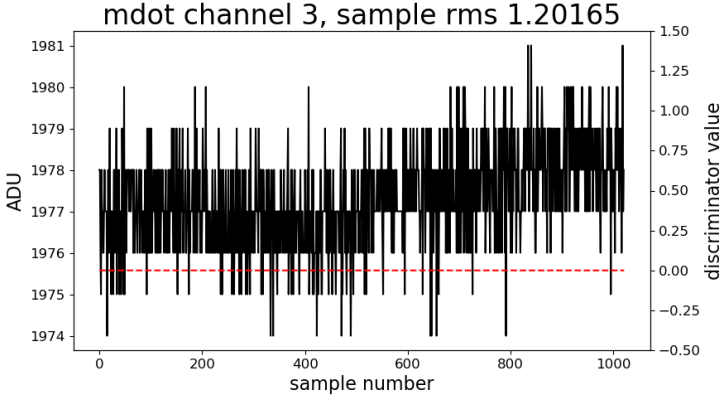
Low Temperature Test, first Results

- Temperature measurement using sensors on channel #3 and #0
- mDOT power off at -60°C (board temp.), fridge was at -70°C
- Repowering after 2 hours at -62°C
  - ICM / mDOT FPGAs, load from flash w/o problems
- analog channels 0, 2 and 3 are functioning at -60°C
- ADC (FPGA) recalibration was not required
  - FPGA internal delays are slightly temperature depending

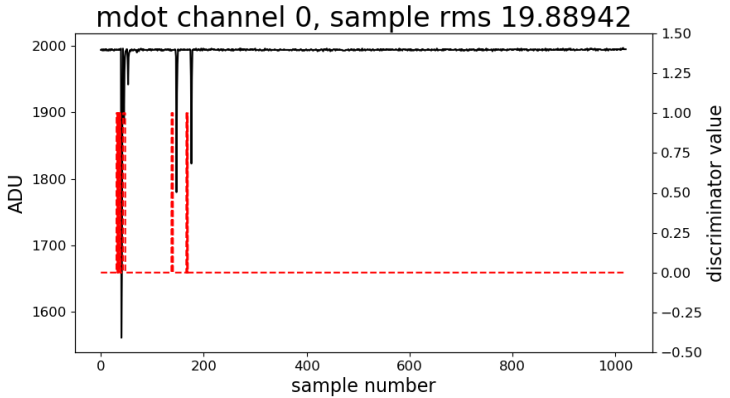
Baseline Noise at -35°C, PMTs connected, HV = off,

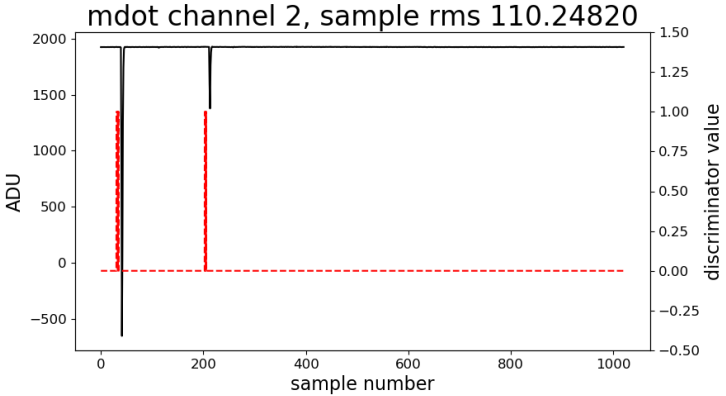


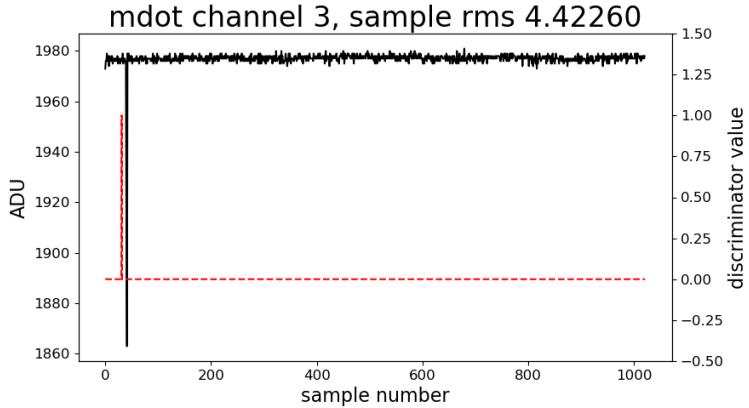




Random PMT Signals at -35°C







Chan_0, Baseline shift vs. Temp., preliminary

Temp. /°C	Baseline	DAC0_e
-15.85	1991	38500
-9.1	1988	
-7.5	1987	
-5.5	1987	
-4.5	1985	
+4.0	1980	
+11.25	1975	
+16,56	1970	

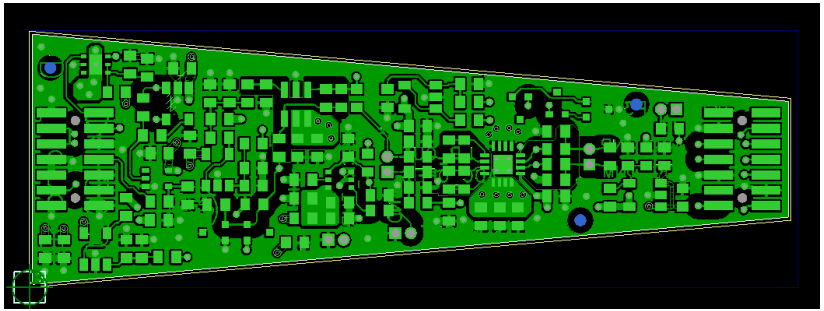
- Baseline shift of ~-0.5% / 30°C (ADC bins, 21 / 4095)
- More careful resistor (gain), V_ref and DAC selection might reduce this value

Comparison, Channel_0 vs. Channel_3

	Chan_0	Chan_3	remark
Input protection	yes	no	To prevent the damage of the preamplifier stage
Coupling, PMT to ADC	DC	AC	Chan_3 with AC-coupling after preamp.
Power consumption	23.7 mW	27.5 mW	Assuming 3.0V will be used at mDOM
mDOM, DAC channels	54	192	mDOM, 9 vs. 26 FPGA pins
Baseline noise	0.6	1.5	Typical RMS, with open input
Min. trig. thr.	1/16 SPE	1/4 SPE	0.5mV vs. 2mV
Dynamic range	1/800 (?)	1/200 (?)	About, to be measured exactly
Test pulse resolution	16bit	16bit	DAC resolution
Test pulse width	1ns * n	1ns * n	Assuming FPGA – oserdes stage is used, Not yet tested

Channel #0b

- Allows to adjust the working point of the preamp stage
  - Wider output range
  - More flexible, could also handle positíve pulses
- Improved ADC input protection
- PCB production started
- 10 modules will be available in first week of May



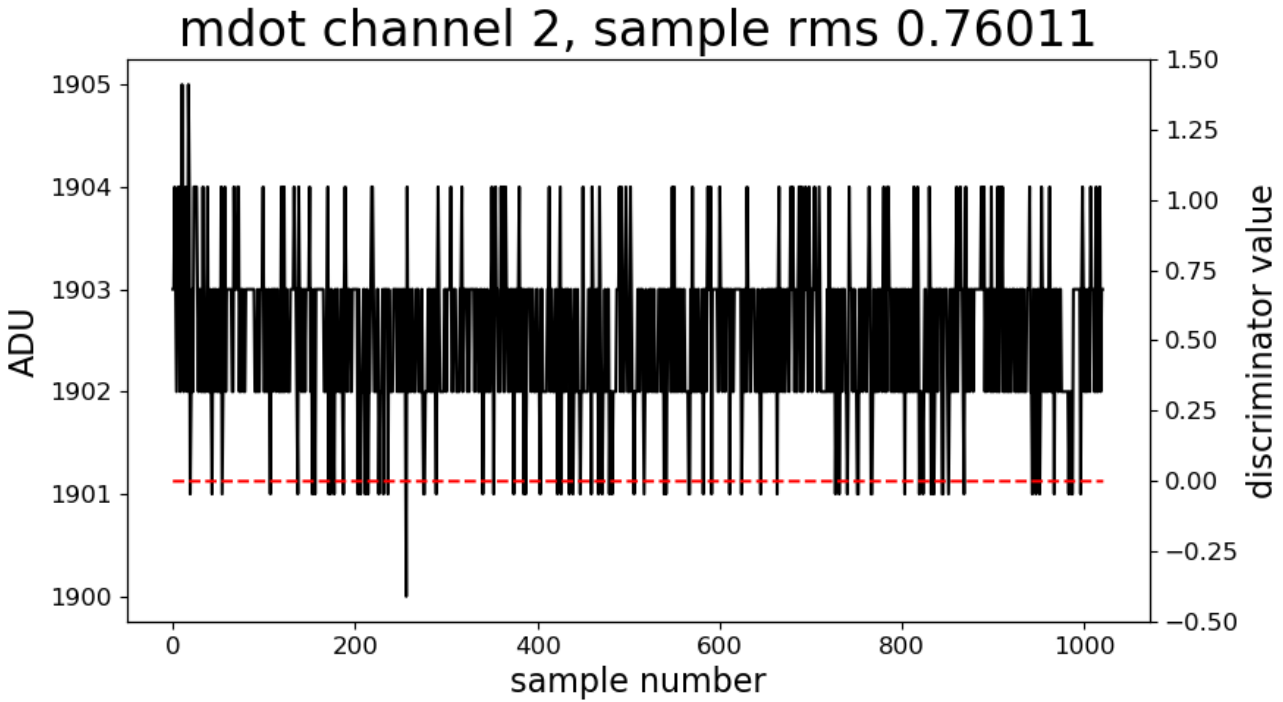
Conclusions

- The FPGA firmware is very stable, a good starting point for the final design
- The transformer based test adapter is useful to get rid of distortions, caused by DC/DC converter + AC-coupled ground loops
- All analog channels work in the cold
- The mDOT power filtering and PCB design can be copied to the final mDOM design
- All channels show a fairly low baseline noise
- the piggyback slot allows fast, low cost analog channel optimization
- further optimization of R,C values might improve the (partial) linearity

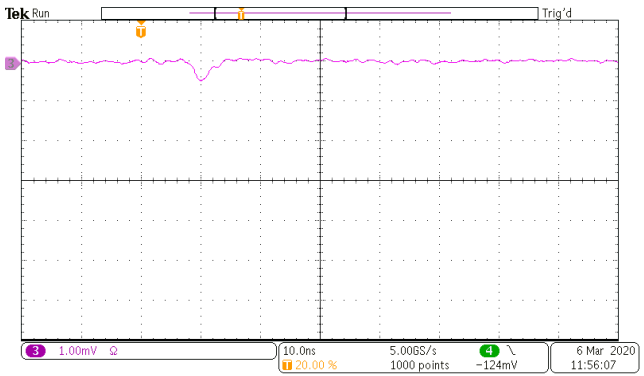
Backup Slides

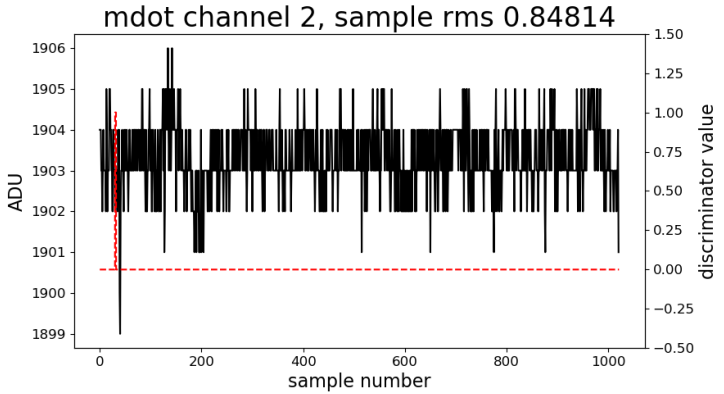
Channel #2, typical noise, with open input

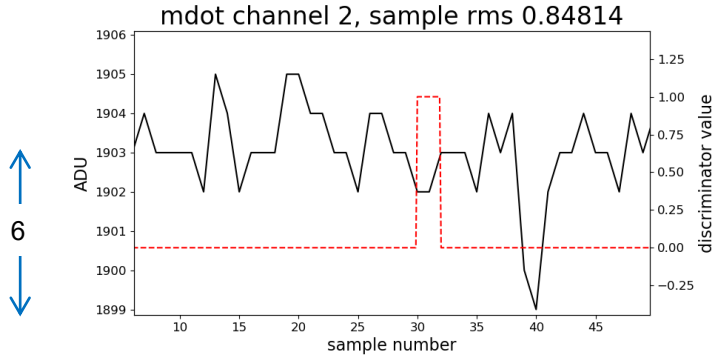
Rin=910R, Rn = **470R**, Cn=10p, LP = 51R x **100p**, DAC0_h = 40000, DAC1_c = 18380



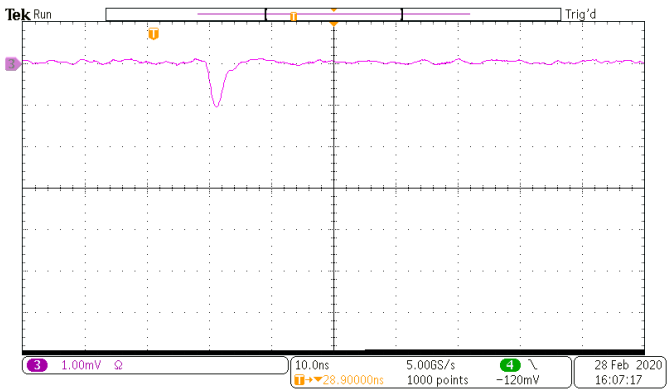
Channel #2, 0.5mV input

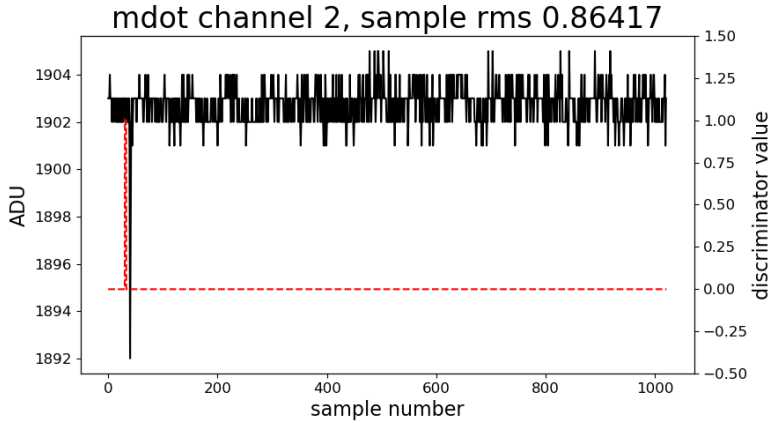


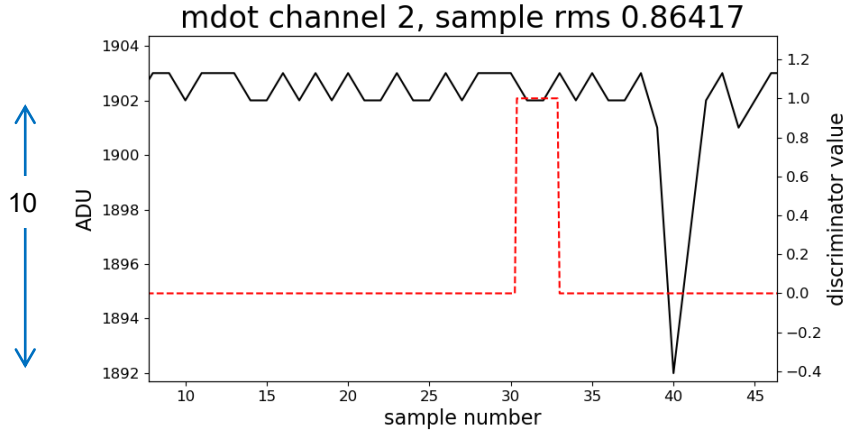




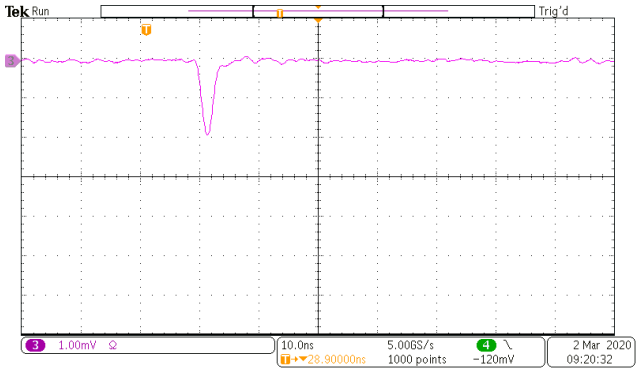
Channel #2, 1mV input

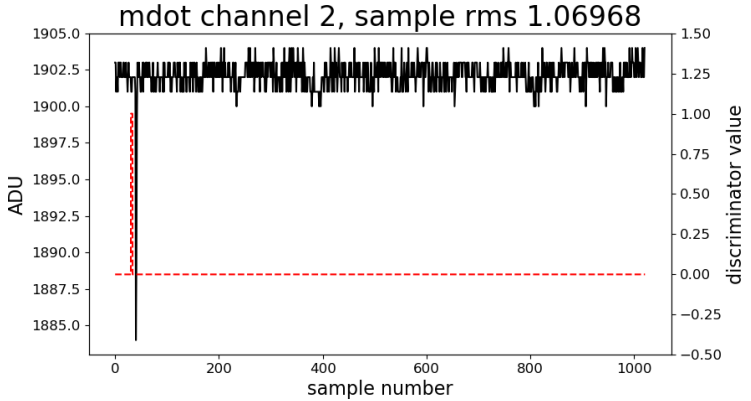




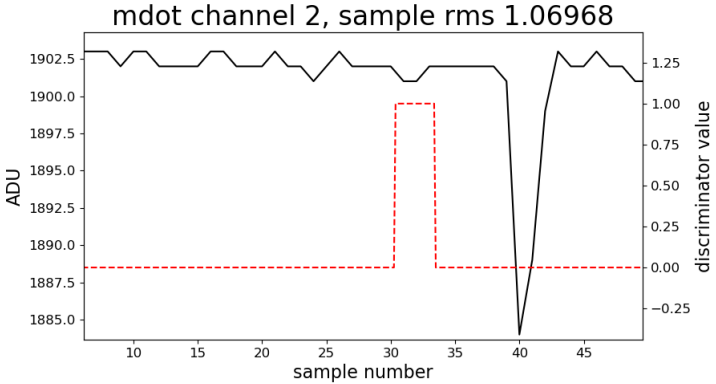


Channel #2, 2mV input

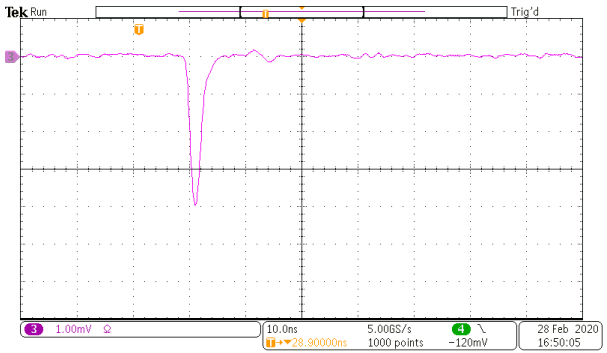


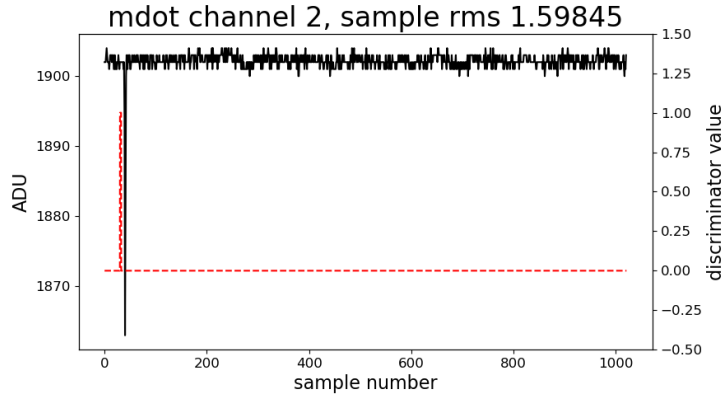


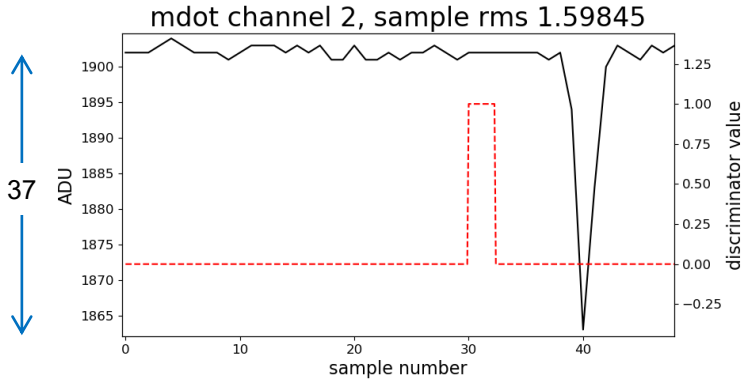
17



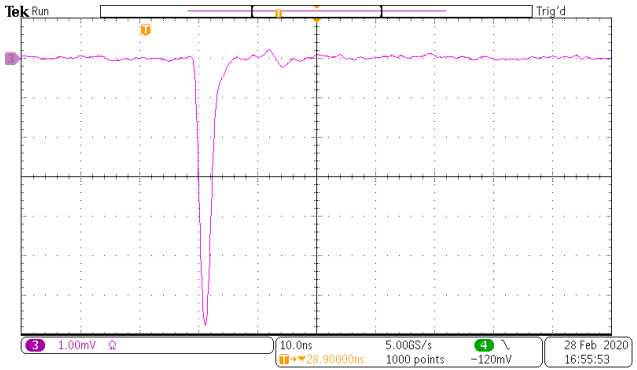
Channel #2, 4mV input

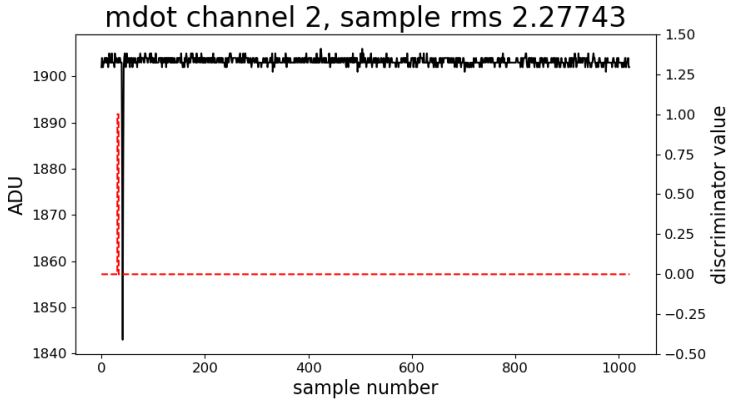


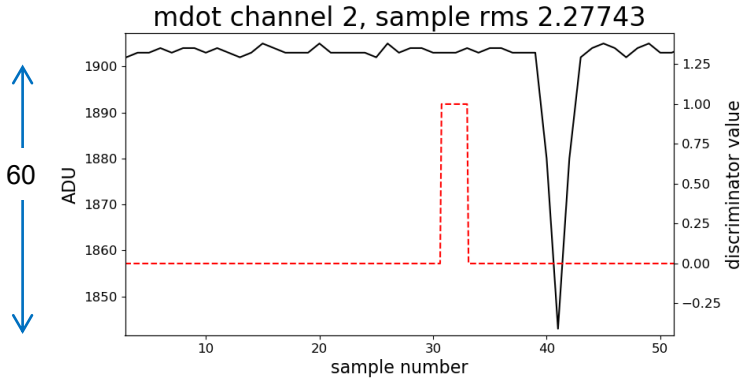




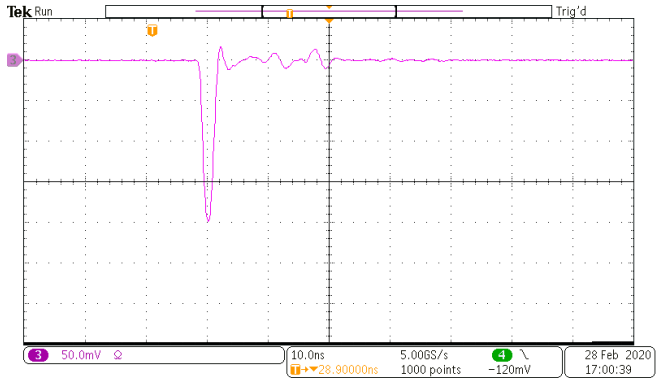
Channel #2, 7mV input

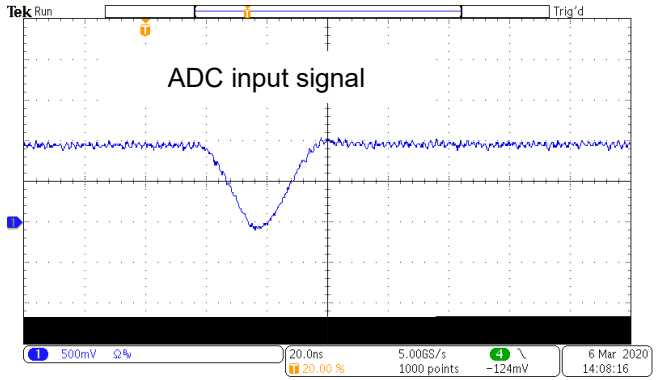




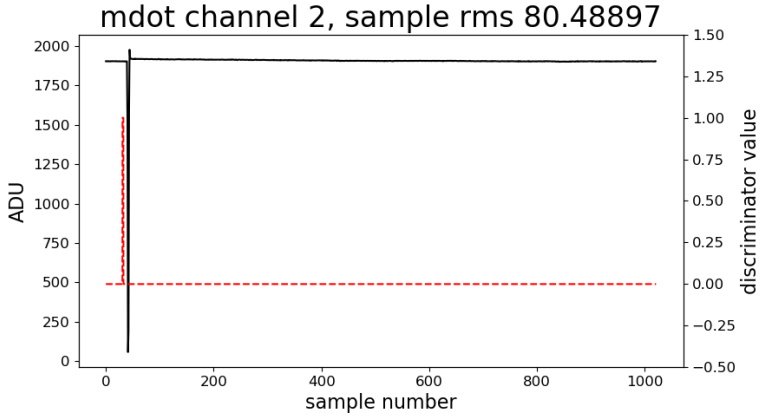


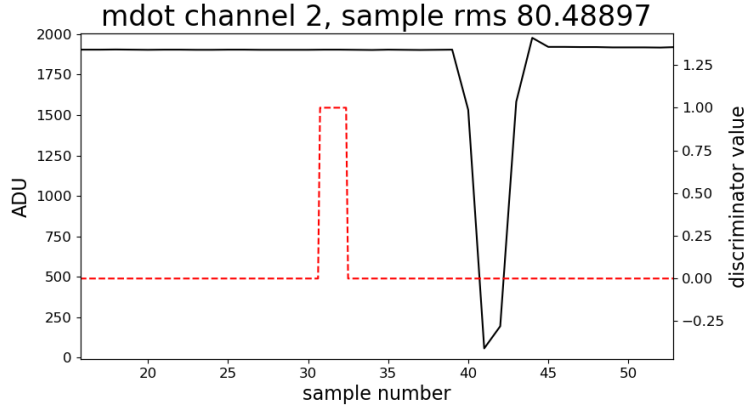
Channel #2, 200mV input



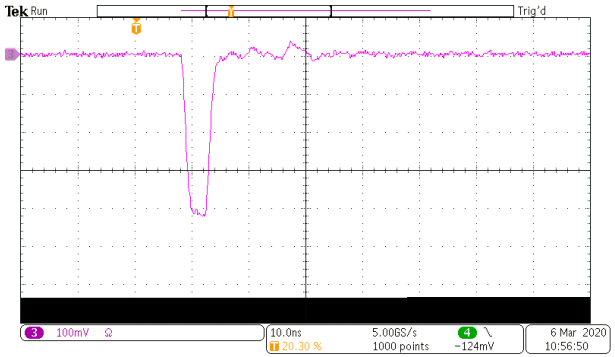


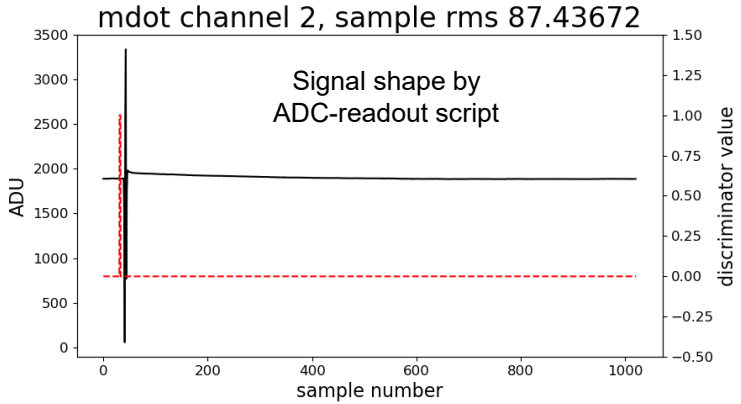
1V

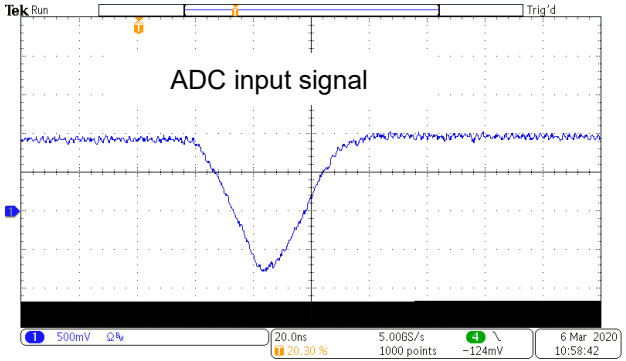




Channel #2, 400mV input

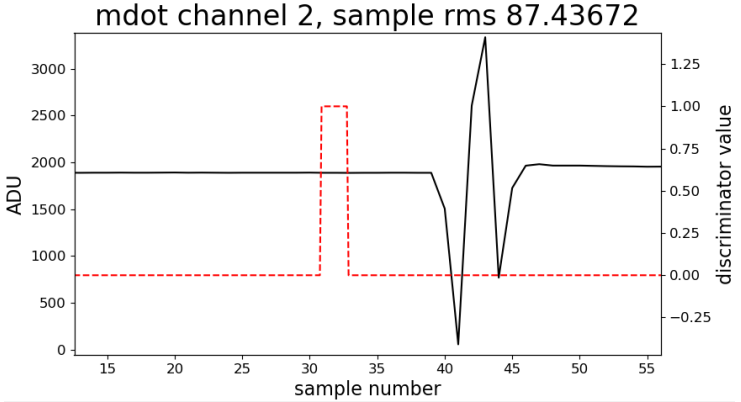




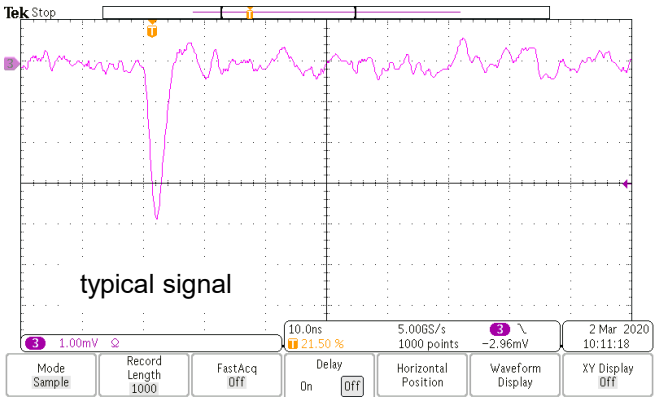


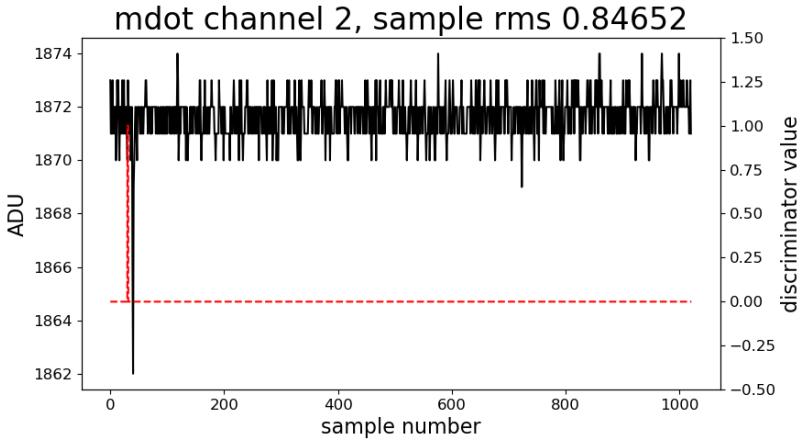
1.7V

3400

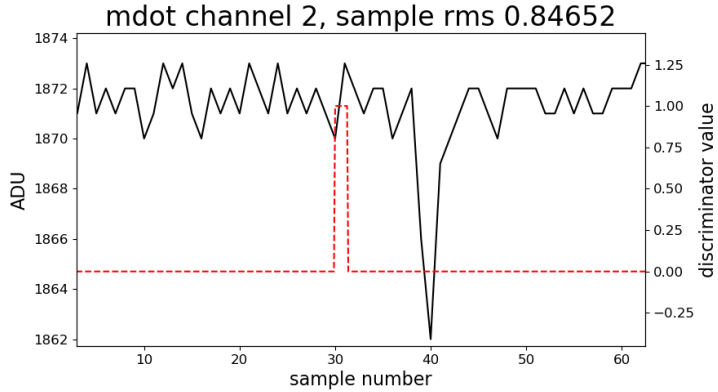


Channel #2, 4mV PMT signal, HV = 567V





9



Channel #2, 200mV PMT signal, HV = 846V