

mDOM Mainbord Rev.2 AFE LT-Spice Schematic Rev.01 with 75ohm input termination

last change:
2021-05-19, R4 1.1k->1k; R14, R25 180R->200R; R26, R27 910R->1k

FPGA input:
use VCC_IO=1.35V
IO_standard= SSTL135
(+/-90mV at Vref=0.675V)

