mDOM mainboard, rev1 to rev2, new FPGA signals

Signal	FPGA-Pin	remark
MCU_CAL_A1	A13	New, keep in tristate
MCU_CAL_A2	A15	New, keep in tristate
MCU_CAL_A3	C18	New, keep in tristate
MCU_CAL_A4	B15	New, keep in tristate
AFE0_TPR	AD20	1.8V, test pulse outputs
AFE1_TPR	AE25	
AFE2_TPR	U24	
AFE3_TPR	H24	
AFE4_TPR	B25	
AFE5_TPR	D19	