# mDOM\_mainboard, MCU Signals

### Introduction

Signals of the D-Egg design have been adopted whenever it was possible.

Some additional signals are defined now, to accommodate the mDOM-special needs.

### Signals removed

|  |  |  |
| --- | --- | --- |
| **MCU** | **mDOM-name** | **Remark** |
| PD7 | MCU\_HVS1\_PWR\_EN | not needed |
| PD12 | MCU\_AUX\_I2C4\_SCL | not used on DEgg either |
| PD13 | MCU\_AUX\_I2C4\_SDA | not used on DEgg either |

### Signals added

|  |  |  |
| --- | --- | --- |
| **MCU** | **mDOM-name** | **Remark** |
| PA6 | MCU\_CAL\_RST |  |
| PA9 | MCU\_AFE\_SEL | to distinguish between CAL-board and AFE-control |
| PA10 | MCU\_AFE\_RST |  |
|  |  |  |
| PC0 | MCU\_HV\_BOOT\_CTRL | needed for PMT base firmware update |
|  |  |  |
| PB0 | MCU\_CAL\_A4 |  |
|  |  |  |
| PC13 | ICM\_PLUGGED | to detect the ICM |

### Signals Name changed

|  |  |  |  |
| --- | --- | --- | --- |
| **MCU** | **DEgg- name** | **mDOM-name** | **remark** |
| PA0 | ICM\_MCU\_SYNC | FPGA\_SYNC |  |
| PA3 | MCU\_CAL\_P5V0\_EN | MCU\_CAL\_P5V\_EN |  |
| PA8 | ICM\_MCU\_USART\_CK | MCU\_USART\_CK |  |
| PA11 | ICM\_MCU\_USART\_CTS | MCU\_USART\_CTS |  |
| PA12 | ICM\_MCU\_USART\_RTS | MCU\_USART\_RTS |  |
|  |  |  |  |
| PB2 | MCU\_SPI3\_MOSI | MCU\_FPGA\_DIN |  |
| PB14 | ICM\_MCU\_USART\_TX | MCU\_USART\_TX |  |
| PB15 | ICM\_MCU\_USART\_RX | MCU\_USART\_RX |  |
|  |  |  |  |
| PC10 | MCU\_SPI3\_SCLK | MCU\_FPGA\_CCLK |  |
|  |  |  |  |
| PD6 | MCU\_HVS0\_PWR\_EN | MCU\_HV\_EN |  |
|  |  |  |  |
| PF6 | MCU\_FPGA\_CONFIG\_DONE | FPGA\_DONE | Xilinx names |
| PF7 | MCU\_FPGA\_nCONFIG | FPGA\_PROG\_B |  |
| PF8 | MCU\_FPGA\_nSTATUS | FPGA\_INIT\_B |  |
|  |  |  |  |
| PG4 | INTLK\_0\_LV | INTLK\_0\_P1V8 |  |
| PG5 | INTLK\_1\_LV | INTLK\_1\_P1V8 |  |
| PG6 | INTLK\_2\_LV | INTLK\_2\_P1V8 |  |
| PG7 | INTLK\_3\_LV | INTLK\_3\_P1V8 |  |
| PG9 | MCU\_FPGA\_UART\_RX | MCU\_USART6\_RX |  |
| PG14 | MCU\_FPGA\_UART\_TX | MCU\_USART6\_TX |  |