

SN54AHC594, SN74AHC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

SCLS423F – JUNE 1998 – REVISED SEPTEMBER 2003

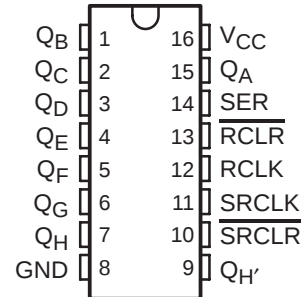
- Operating Range 2-V to 5.5-V V_{CC}
- 8-Bit Serial-In, Parallel-Out Shift Registers With Storage
- Independent Direct Overriding Clears on Shift and Storage Registers
- Independent Clocks for Shift and Storage Registers
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

description/ordering information

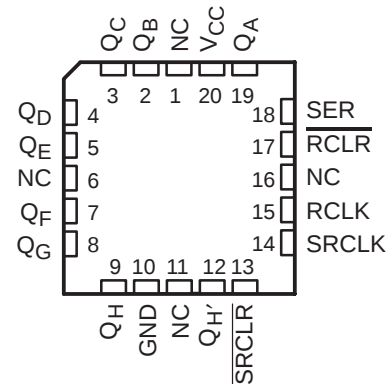
The 'AHC594 devices contain an 8-bit serial-in, parallel-out shift register that feeds an 8-bit D-type storage register. Separate clocks and direct overriding clear ($\overline{SRCLR}$, $\overline{RCLR}$) inputs are provided on the shift and storage registers. A serial (Q_H) output is provided for cascading purposes.

The shift register (SRCLK) and storage register (RCLK) clocks are positive-edge triggered. If the clocks are tied together, the shift register always is one clock pulse ahead of the storage register.

SN54AHC594 . . . J OR W PACKAGE
SN74AHC594 . . . D, DB, N, NS, OR PW PACKAGE
(TOP VIEW)



SN54AHC594 . . . FK PACKAGE
(TOP VIEW)



NC – No internal connection

ORDERING INFORMATION

T_A	PACKAGE [†]		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	PDIP – N	Tube	SN74AHC594N	SN74AHC594N
	SOIC – D	Tube	SN74AHC594D	AHC594
		Tape and reel	SN74AHC594DR	
	SOP – NS	Tape and reel	SN74AHC594NSR	AHC594
	SSOP – DB	Tape and reel	SN74AHC594DBR	HA594
	TSSOP – PW	Tube	SN74AHC594PW	HA594
		Tape and reel	SN74AHC594PWR	
–55°C to 125°C	CDIP – J	Tube	SNJ54AHC594J	SNJ54AHC594J
	CFP – W	Tube	SNJ54AHC594W	SNJ54AHC594W
	LCCC – FK	Tube	SNJ54AHC594FK	SNJ54AHC594FK

[†] Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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**TEXAS
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SN54AHC594, SN74AHC594

8-BIT SHIFT REGISTERS

WITH OUTPUT REGISTERS

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FUNCTION TABLE

INPUTS					FUNCTION
SER	SRCLK	$\overline{\text{SRCLR}}$	RCLK	$\overline{\text{RCLR}}$	
X	X	L	X	X	Shift register is cleared.
L	↑	H	X	X	First stage of shift register goes low. Other stages store the data of previous stage, respectively.
H	↑	H	X	X	First stage of shift register goes high. Other stages store the data of previous stage, respectively.
L	↓	H	X	X	Shift register state is not changed.
X	X	X	X	L	Storage register is cleared.
X	X	X	↑	H	Shift register data is stored in the storage register.
X	X	X	↓	H	Storage register state is not changed.

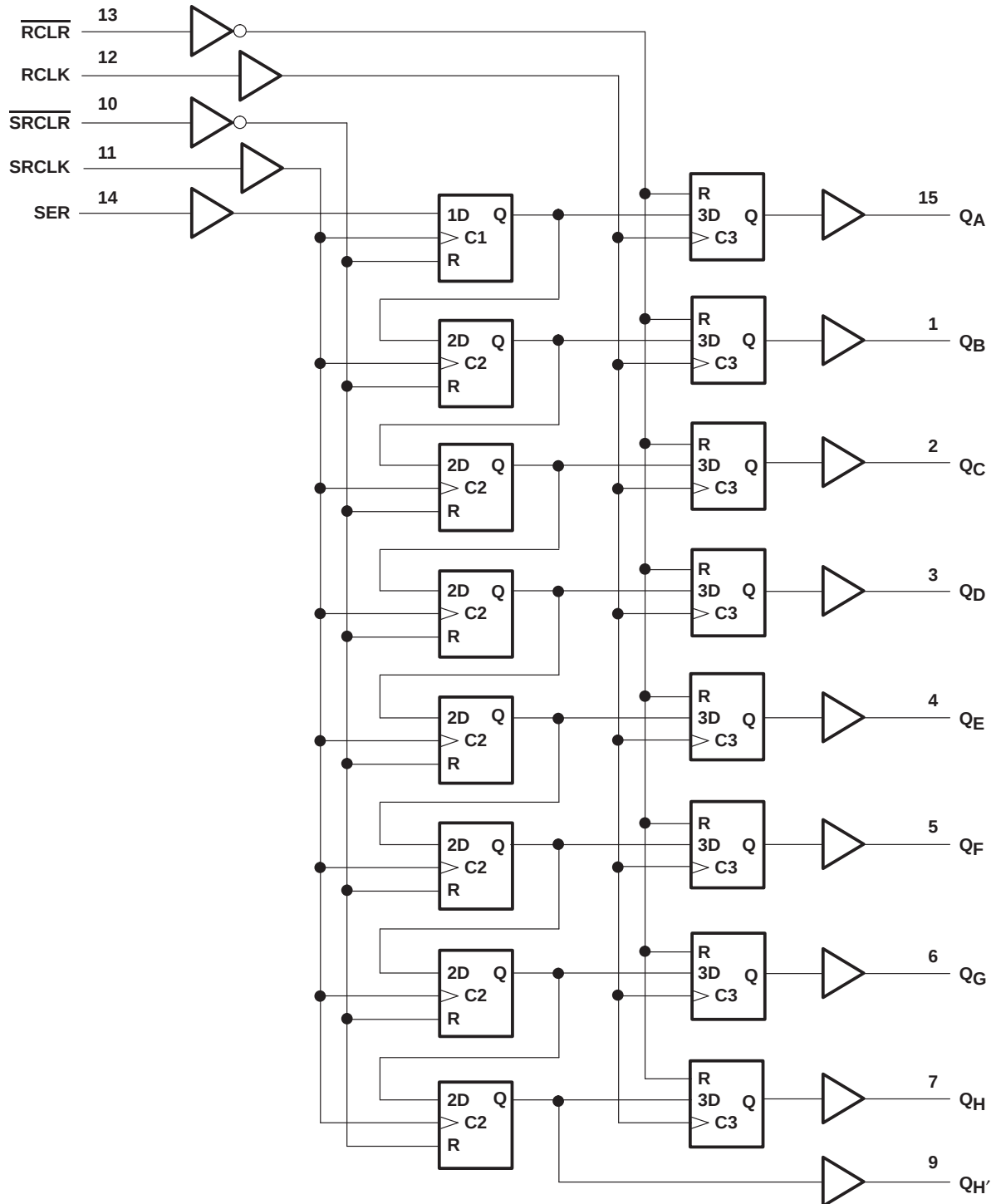
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logic diagram (positive logic)



Pin numbers shown are for the D, DB, J, N, NS, PW, and W packages.

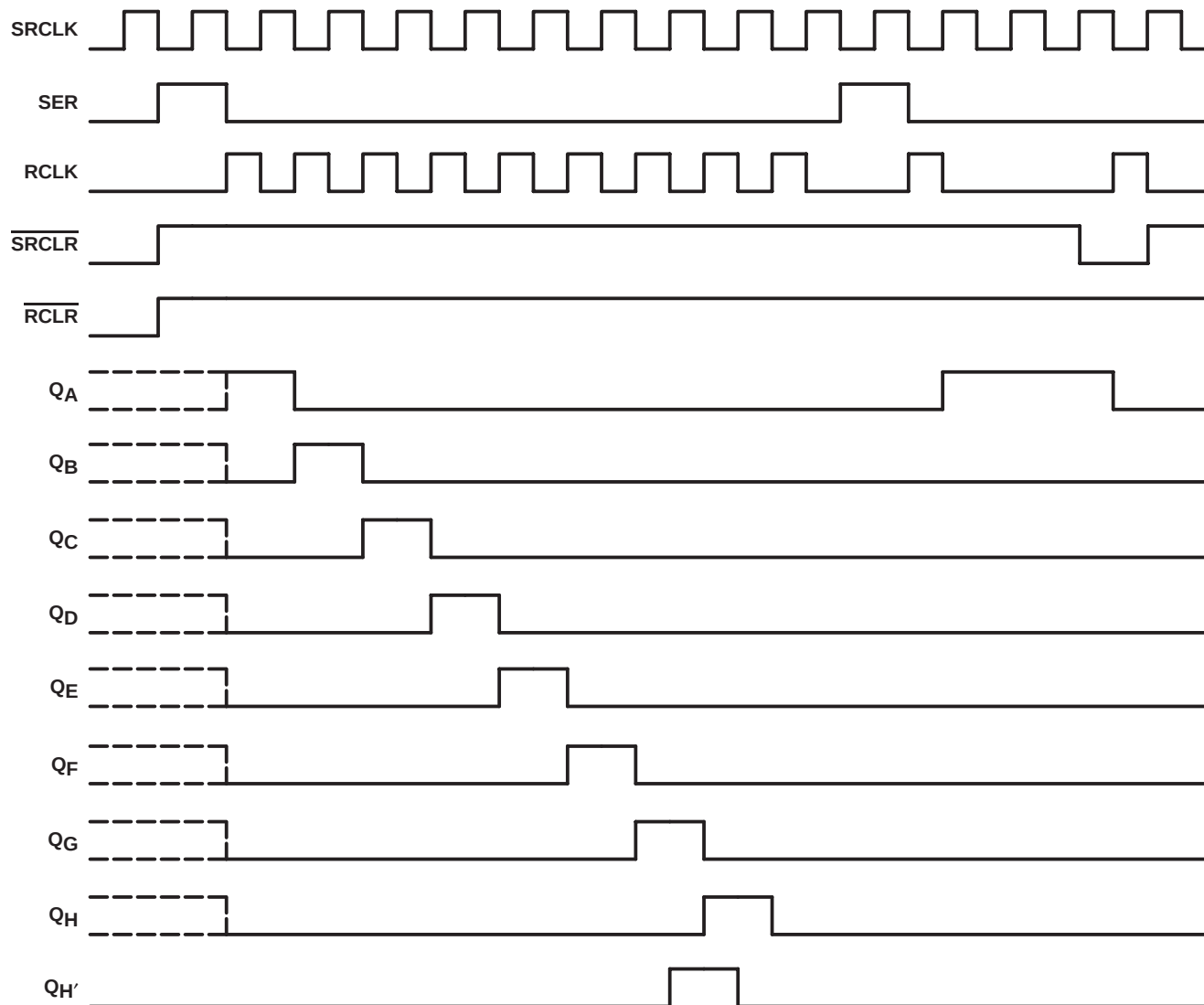
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timing diagram



SN54AHC594, SN74AHC594 8-BIT SHIFT REGISTERS WITH OUTPUT REGISTERS

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absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CC}	–0.5 V to 7 V
Input voltage range, V_I (see Note 1)	–0.5 V to 7 V
Output voltage range, V_O (see Note 1)	–0.5 V to $V_{CC} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–20 mA
Output clamp current, I_{OK} ($V_O < 0$ or $V_O > V_{CC}$)	±20 mA
Continuous output current, I_O ($V_O = 0$ to V_{CC})	±25 mA
Continuous current through V_{CC} or GND	±75 mA
Package thermal impedance, θ_{JA} (see Note 2): D package	73°C/W
DB package	82°C/W
N package	67°C/W
NS package	64°C/W
PW package	108°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

recommended operating conditions (see Note 3)

			SN54AHC594		SN74AHC594		UNIT
			MIN	MAX	MIN	MAX	
V_{CC}	Supply voltage		2	5.5	2	5.5	V
V_{IH}	High-level input voltage	$V_{CC} = 2$ V	1.5		1.5		V
		$V_{CC} = 3$ V	2.1		2.1		
		$V_{CC} = 5.5$ V	3.85		3.85		
V_{IL}	Low-level input voltage	$V_{CC} = 2$ V		0.5		0.5	V
		$V_{CC} = 3$ V		0.9		0.9	
		$V_{CC} = 5.5$ V		1.65		1.65	
V_I	Input voltage		0	5.5	0	5.5	V
V_O	Output voltage		0	V_{CC}	0	V_{CC}	V
I_{OH}	High-level output current	$V_{CC} = 2$ V		–50		–50	µA
		$V_{CC} = 3.3$ V ± 0.3 V		–4		–4	mA
		$V_{CC} = 5$ V ± 0.5 V		–8		–8	
I_{OL}	Low-level output current	$V_{CC} = 2$ V		50		50	µA
		$V_{CC} = 3.3$ V ± 0.3 V		4		4	mA
		$V_{CC} = 5$ V ± 0.5 V		8		8	
$\Delta t/\Delta v$	Input transition rise or fall rate	$V_{CC} = 3.3$ V ± 0.3 V		100		100	ns/V
		$V_{CC} = 5$ V ± 0.5 V		20		20	
T_A	Operating free-air temperature		–55	125	–40	85	°C

NOTE 3: All unused inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V _{CC}	T _A = 25°C			SN54AHC594		SN74AHC594		UNIT
			MIN	TYP	MAX	MIN	MAX	MIN	MAX	
V _{OH}	I _{OH} = -50 µA	2 V	1.9	2		1.9		1.9		V
		3 V	2.9	3		2.9		2.9		
		4.5 V	4.4	4.5		4.4		4.4		
	I _{OH} = -4 mA	3 V	2.58			2.48		2.48		
	Q _H ', I _{OH} = -4 mA	4.5 V	3.94			3.8		3.8		
	Q _A -Q _H , I _{OH} = -8 mA		3.94			3.8		3.8		
V _{OL}	I _{OL} = 50 µA	2 V			0.1		0.1		0.1	V
		3 V			0.1		0.1		0.1	
		4.5 V			0.1		0.1		0.1	
	I _{OL} = 4 mA	3 V			0.36		0.5		0.44	
	Q _H ', I _{OL} = 4 mA	4.5 V			0.36		0.5		0.44	
	Q _A -Q _H , I _{OL} = 8 mA				0.36		0.5		0.44	
I _I	V _I = 5.5 V or GND	0 V to 5.5 V			±0.1		±1*		±1	µA
I _{CC}	V _I = V _{CC} or GND, I _O = 0	5.5 V			4		40		40	µA
C _i	V _I = V _{CC} or GND	5 V		2	10				10	pF

* On products compliant to MIL-PRF-38535, this parameter is not production tested at V_{CC} = 0 V.

timing requirements over recommended operating free-air temperature range, V_{CC} = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

		T _A = 25°C		SN54AHC594		SN74AHC594		UNIT
		MIN	MAX	MIN	MAX	MIN	MAX	
t _w	Pulse duration	RCLK or SRCLK high or low		5.5		5.5		ns
		RCLR or SRCLR low		5		5		
t _{su}	Setup time	SER before SRCLK↑		3.5		3.5		ns
		SRCLK↑ before RCLK↑†		8		8.5		
		SRCLR low before RCLK↑		8		9		
		SRCLR high (inactive) before SRCLK↑		4.2		4.8		
		RCLR high (inactive) before RCLK↑		4.6		5.3		
t _h	Hold time	SER after SRCLK↑		1.5		1.5		ns

† This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

PRODUCT PREVIEW information concerns products in the formative or design phase of development. Characteristic data and other specifications are design goals. Texas Instruments reserves the right to change or discontinue these products without notice.



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timing requirements over recommended operating free-air temperature range, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

			$T_A = 25^\circ\text{C}$		SN54AHC594		SN74AHC594		UNIT
			MIN	MAX	MIN	MAX	MIN	MAX	
t_w	Pulse duration	RCLK or SRCLK high or low	5		5		5		ns
		$\overline{\text{RCLR}}$ or $\overline{\text{SRCLR}}$ low	5.2		5.2		5.2		
t_{su}	Setup time	SER before SRCLK $\uparrow$	3		3		3		ns
		SRCLK $\uparrow$ before RCLK $\uparrow$ [†]	5		5		5		
		$\overline{\text{SRCLR}}$ low before RCLK $\uparrow$	5		5		5		
		$\overline{\text{SRCLR}}$ high (inactive) before SRCLK $\uparrow$	2.9		3.3		3.3		
		$\overline{\text{RCLR}}$ high (inactive) before RCLK $\uparrow$	3.2		3.7		3.7		
t_h	Hold time	SER after SRCLK $\uparrow$	2		2		2		ns

[†] This setup time allows the storage register to receive stable data from the shift register. The clocks can be tied together, in which case the shift register is one clock pulse ahead of the storage register.

switching characteristics over recommended operating free-air temperature range, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC594		SN74AHC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	80*	120*		70*		70		MHz
			$C_L = 50\text{ pF}$	55	105		50		50		
t_{PLH}	RCLK	$Q_A - Q_H$	$C_L = 15\text{ pF}$	4.6*	8*		1*	8.5*	1	8.5	ns
t_{PHL}				4.9*	8.2*		1*	8.8*	1	8.8	
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 15\text{ pF}$	5.4*	9.1*		1*	9.7*	1	9.7	ns
t_{PHL}				5.5*	9.2*		1*	9.9*	1	9.9	
t_{PHL}	$\overline{\text{RCLR}}$	$Q_A - Q_H$	$C_L = 15\text{ pF}$	6*	9.8*		1*	10.6*	1	10.6	ns
t_{PHL}	$\overline{\text{SRCLR}}$	$Q_{H'}$	$C_L = 15\text{ pF}$	5.6*	9.2*		1*	10*	1	10	ns
t_{PLH}	RCLK	$Q_A - Q_H$	$C_L = 50\text{ pF}$	6.9	10.5		1	11.1	1	11.1	ns
t_{PHL}				8.1	11.9		1	13.1	1	13.1	
t_{PLH}	SRCLK	$Q_{H'}$	$C_L = 50\text{ pF}$	7.7	11.7		1	12.4	1	12.4	ns
t_{PHL}				8.4	12.5		1	13.9	1	13.9	
t_{PHL}	$\overline{\text{RCLR}}$	$Q_A - Q_H$	$C_L = 50\text{ pF}$	9.1	13.1		1	14.4	1	14.4	ns
t_{PHL}	$\overline{\text{SRCLR}}$	$Q_{H'}$	$C_L = 50\text{ pF}$	8.5	12.4		1	14	1	14	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

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8-BIT SHIFT REGISTERS

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switching characteristics over recommended operating free-air temperature range,
 $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ (unless otherwise noted) (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	$T_A = 25^\circ\text{C}$			SN54AHC594		SN74AHC594		UNIT
				MIN	TYP	MAX	MIN	MAX	MIN	MAX	
f_{max}			$C_L = 15\text{ pF}$	135*	170*		115*		115		MHz
			$C_L = 50\text{ pF}$	120	140		95		95		
t_{PLH}	RCLK	Q_A-Q_H	$C_L = 15\text{ pF}$		3.3*	6.2*	1*	6.5*	1	6.5	ns
t_{PHL}					3.7*	6.5*	1*	6.9*	1	6.9	
t_{PLH}	SRCLK	Q_H'	$C_L = 15\text{ pF}$		3.7*	6.8*	1*	7.2*	1	7.2	ns
t_{PHL}					4.1*	7.2*	1*	7.6*	1	7.6	
t_{PHL}	$\overline{\text{RCLR}}$	Q_A-Q_H	$C_L = 15\text{ pF}$		4.5*	7.6*	1*	8.2*	1	8.2	ns
t_{PHL}	$\overline{\text{SRCLR}}$	Q_H'	$C_L = 15\text{ pF}$		4.1*	7.1*	1*	7.6*	1	7.6	ns
t_{PLH}	RCLK	Q_A-Q_H	$C_L = 50\text{ pF}$		4.9	7.8	1	8.3	1	8.3	ns
t_{PHL}					5.8	8.9	1	9.7	1	9.7	
t_{PLH}	SRCLK	Q_H'	$C_L = 50\text{ pF}$		5.5	8.6	1	9.1	1	9.1	ns
t_{PHL}					6	9.2	1	10.1	1	10.1	
t_{PHL}	$\overline{\text{RCLR}}$	Q_A-Q_H	$C_L = 50\text{ pF}$		6.6	10	1	10.7	1	10.7	ns
t_{PHL}	$\overline{\text{SRCLR}}$	Q_H'	$C_L = 50\text{ pF}$		6	9.2	1	10.1	1	10.1	ns

* On products compliant to MIL-PRF-38535, this parameter is not production tested.

noise characteristics, $V_{CC} = 5\text{ V}$, $C_L = 50\text{ pF}$, $T_A = 25^\circ\text{C}$ (see Note 4)

PARAMETER	SN74AHC594			UNIT
	MIN	TYP	MAX	
$V_{OL(P)}$ Quiet output, maximum dynamic V_{OL}		1		V
$V_{OL(V)}$ Quiet output, minimum dynamic V_{OL}		-0.6		V
$V_{OH(V)}$ Quiet output, minimum dynamic V_{OH}		3.8		V
$V_{IH(D)}$ High-level dynamic input voltage		3.5		V
$V_{IL(D)}$ Low-level dynamic input voltage			1.5	V

NOTE 4: Characteristics are for surface-mount packages only.

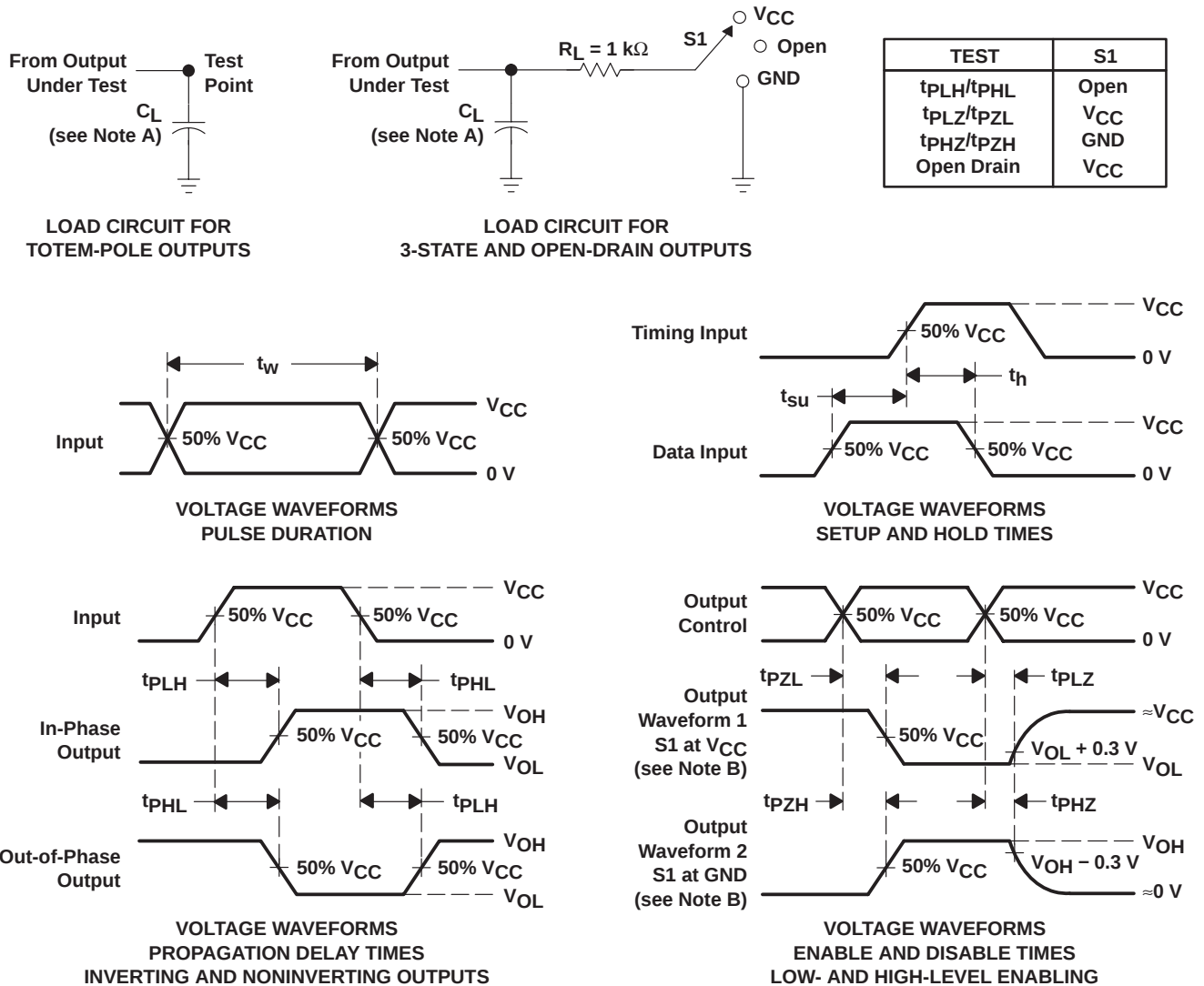
operating characteristics, $V_{CC} = 5\text{ V}$, $T_A = 25^\circ\text{C}$

PARAMETER	TEST CONDITIONS	TYP	UNIT
C_{pd} Power dissipation capacitance	No load, $f = 1\text{ MHz}$	112	pF

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PARAMETER MEASUREMENT INFORMATION



- NOTES: A. C_L includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 1\text{ MHz}$, $Z_O = 50\ \Omega$, $t_r \leq 3\text{ ns}$, $t_f \leq 3\text{ ns}$.
- D. The outputs are measured one at a time with one input transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

Orderable Device	Status ⁽¹⁾	Package Type	Package Drawing	Pins	Package Qty	Eco Plan ⁽²⁾	Lead/Ball Finish	MSL Peak Temp ⁽³⁾
SN74AHC594D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594DBR	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594DBRE4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594DBRG4	ACTIVE	SSOP	DB	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594DE4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594DR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594DRE4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594DRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594N	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHC594NE4	ACTIVE	PDIP	N	16	25	Pb-Free (RoHS)	CU NIPDAU	N / A for Pkg Type
SN74AHC594NSR	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594NSRE4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594NSRG4	ACTIVE	SO	NS	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594PWE4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594PWG4	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594PWR	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594PWRE4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM
SN74AHC594PWRG4	ACTIVE	TSSOP	PW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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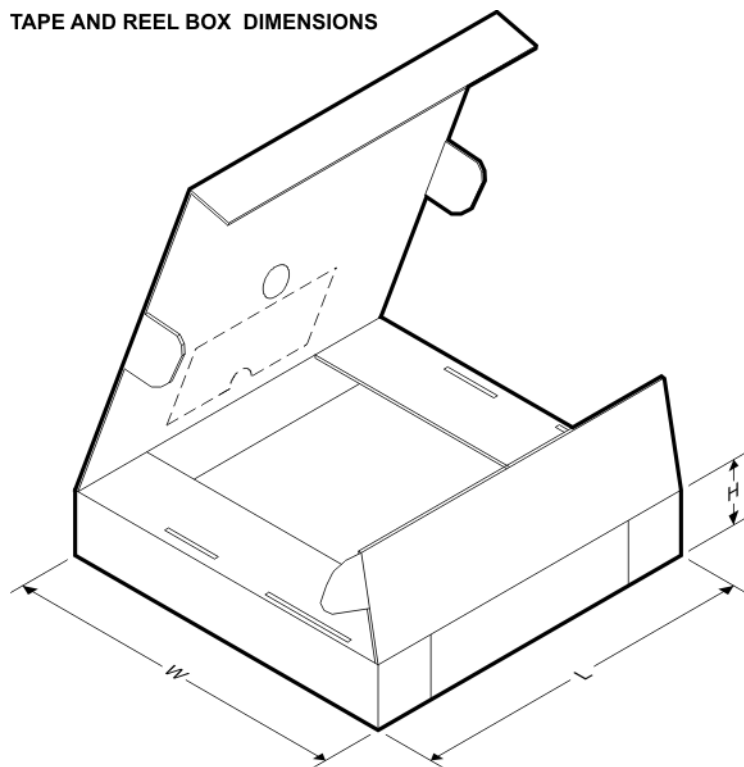
TAPE AND REEL INFORMATION



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74AHC594DBR	SSOP	DB	16	2000	330.0	16.4	8.2	6.6	2.5	12.0	16.0	Q1
SN74AHC594DR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
SN74AHC594NSR	SO	NS	16	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74AHC594PWR	TSSOP	PW	16	2000	330.0	12.4	7.0	5.6	1.6	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74AHC594DBR	SSOP	DB	16	2000	346.0	346.0	33.0
SN74AHC594DR	SOIC	D	16	2500	333.2	345.9	28.6
SN74AHC594NSR	SO	NS	16	2000	346.0	346.0	33.0
SN74AHC594PWR	TSSOP	PW	16	2000	346.0	346.0	29.0

DB (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



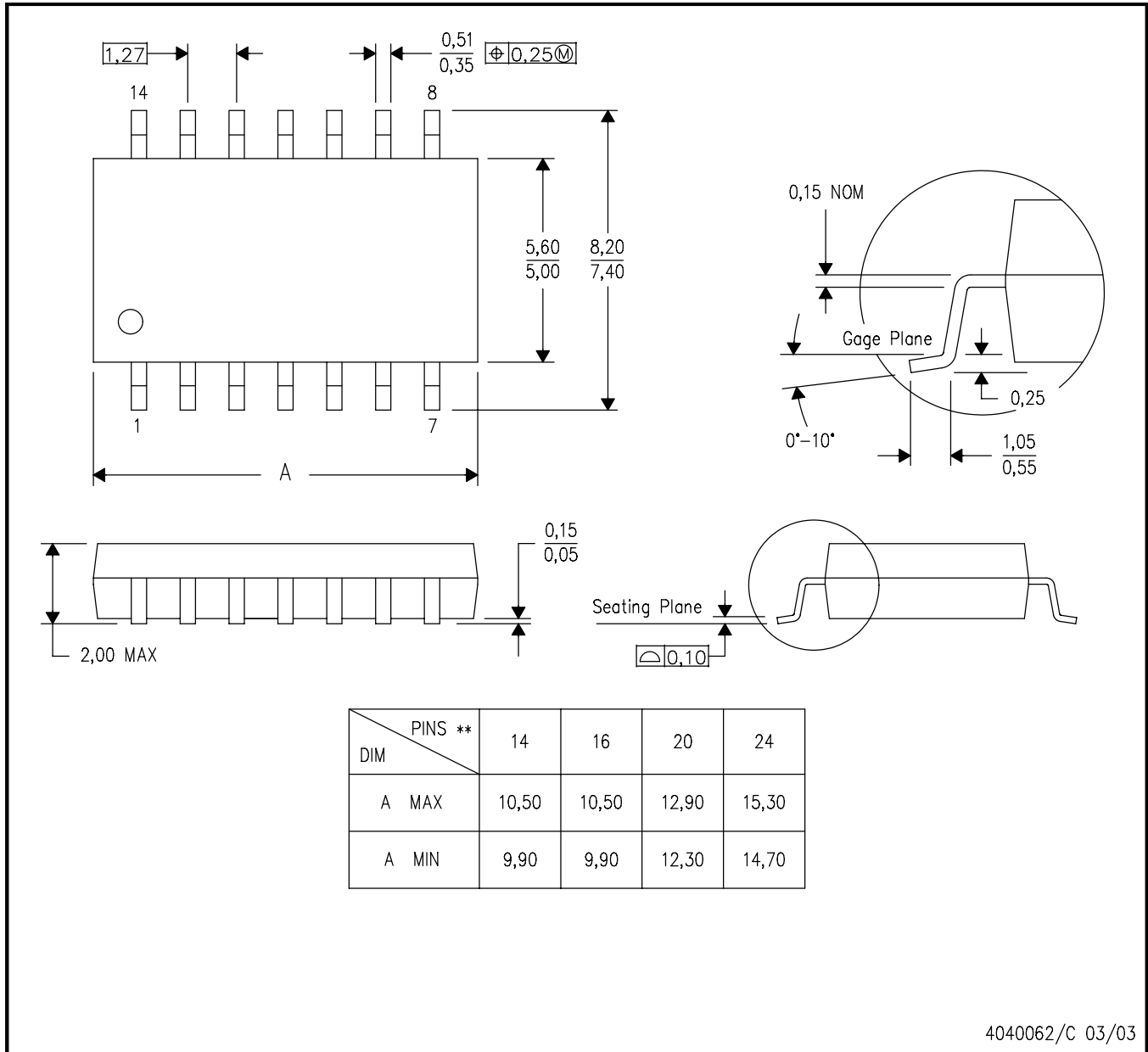
- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-150

MECHANICAL DATA

NS (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

PW (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

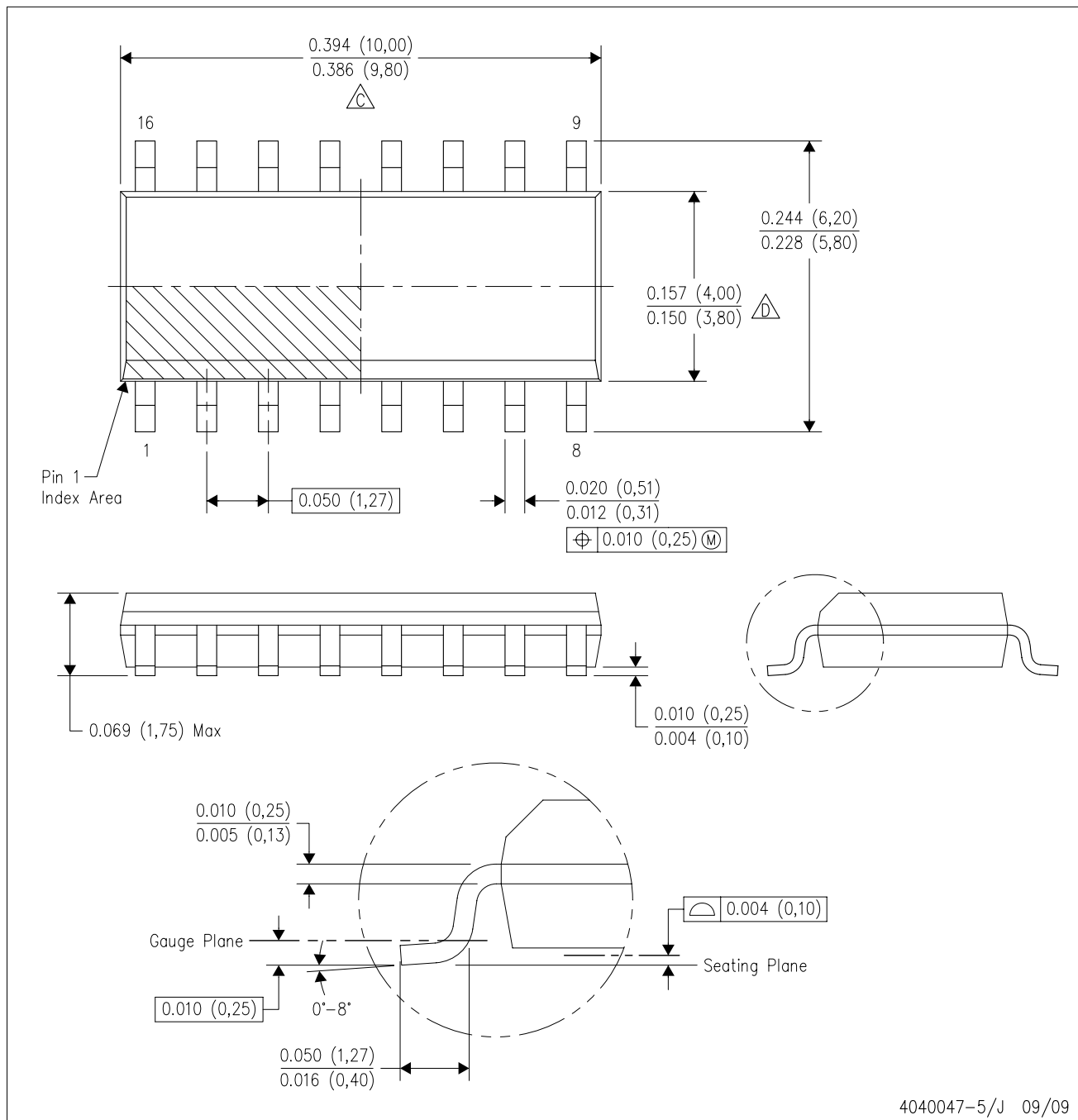
14 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

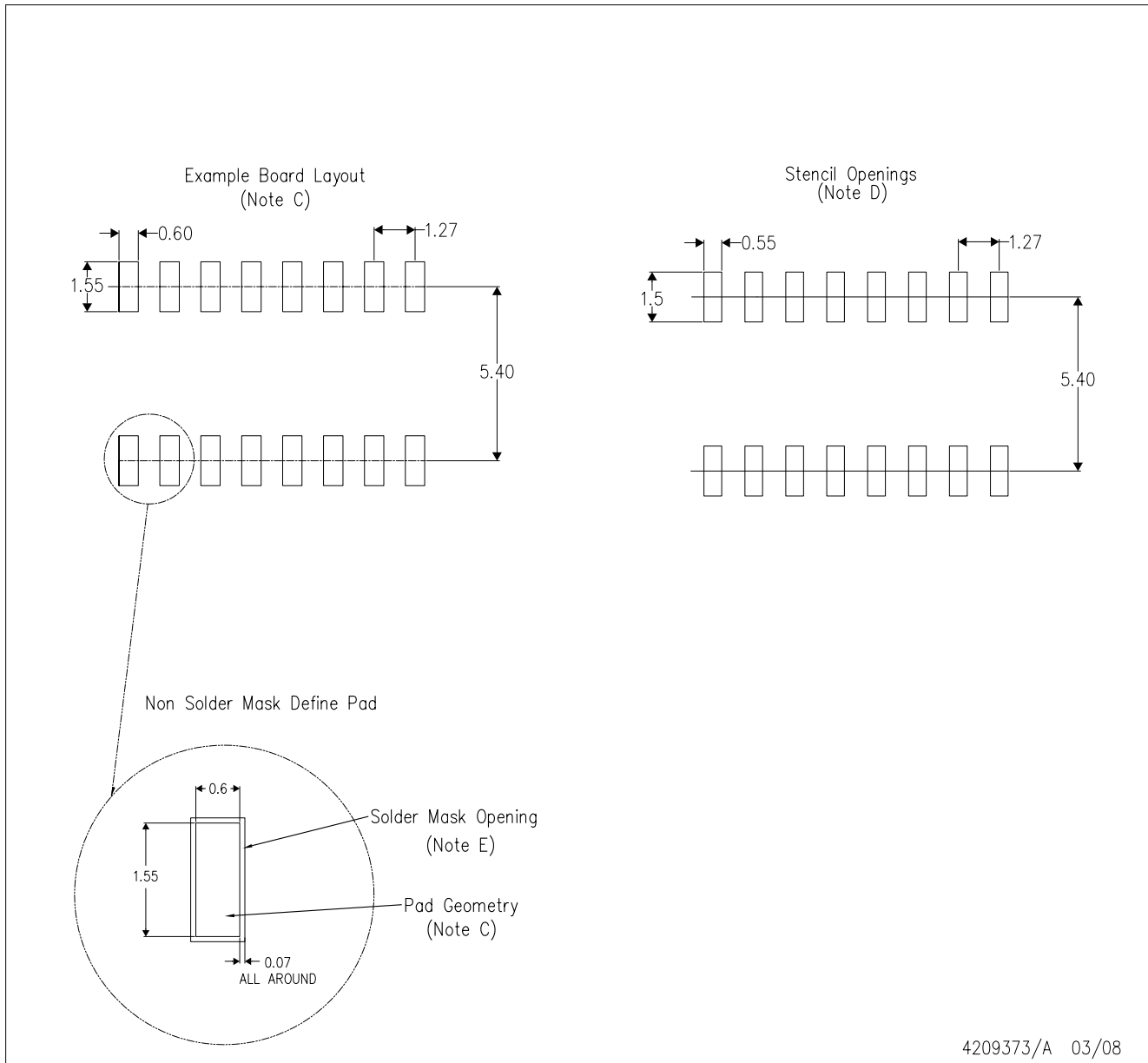
D (R-PDSO-G16)

PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - $\triangle C$ Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 (0,15) per end.
 - $\triangle D$ Body width does not include interlead flash. Interlead flash shall not exceed .017 (0,43) per side.
 - E. Reference JEDEC MS-012 variation AC.

D(R-PDSO-G16)



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Refer to IPC7351 for alternate board design.
 - D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525
 - E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

N (R-PDIP-T**)

16 PINS SHOWN

PLASTIC DUAL-IN-LINE PACKAGE



PINS **	14	16	18	20
DIM				
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS-001 VARIATION	AA	BB	AC	AD



14/18 Pin Only
20 Pin vendor option

4040049/E 12/2002

- NOTES:
- A. All linear dimensions are in inches (millimeters).
 - B. This drawing is subject to change without notice.
 - Falls within JEDEC MS-001, except 18 and 20 pin minimum body length (Dim A).
 - The 20 pin end lead shoulder width is a vendor option, either half or full width.

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