mb_hv_ctrl Firmware Properties

CPLD: XC2C128-7VQ100

Revision	Name	Short Description
5	mb_hv_ctrl_5.jed	The software has to set a 30bit shift register. Required are 31 clocks (MCU_CAL_SCLK). The 31st clock is used to update (latch) the output signals. MSB first (MCU_CAL_MOSI). MCU_CAL_SS must be '0', MCU_AFE_SEL must be '1' for the whole write cycle. The shift register data are clocked in at the upgoing MCU_CAL_SCLK edge. Bit30 dummy Bit29..25 UART_MUX_4..0 -- to select one of the PMT-bases BIT24..1 AFE_ENABLE_23..0 -- high active, '1' = power on, sequential enabling recommended BIT0 TX_BROADCAST_ENABLE -- high active, '1' = MCU_USART6_TX is fanout to HV-chan 23..0 MCU signal usage: MCU_AFE_RST, MCU port PA10, asynchronous reset, high active ➔ UART_MUX_4..0=00h, AFE_ENABLE_23..0 = 000000h MCU_AFE_SEL MCU port PA9, to distinguish between AFE and mDAB access, high active, AFE_SEL = '1' MCU_CAL_SS MCU port PE4, low active frame signal (like nCS) MCU_CAL_SCLK MCU port PE2, SPI clock, 0..50MHz MCU_CAL_MOSI MCU port PE6, SPI data MCU_USART6_RX MCU port PG9, connected to PMT base-TX via UART_MUX MCU_USART6_TX MCU port PG14, connected to PMT base-RX via UART_MUX HV_UART_RX0..23 inputs in standard mode, neither pullup, keeper or SCHMITT_TRIGGER anymore