# mb\_hv\_ctrl Firmware Properties

CPLD: XC2C128-7VQ100

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| **Revision** | **Name** | **Short Description** |
| 5 | mb\_hv\_ctrl\_5.jed | The software has to set a 30bit shift register. Required are 31 clocks (MCU\_CAL\_SCLK). The 31st clock is used to update (latch) the output signals. MSB first (MCU\_CAL\_MOSI). MCU\_CAL\_SS must be ‘0’, MCU\_AFE\_SEL must be ‘1’ for the whole write cycle. The shift register data are clocked in at the upgoing MCU\_CAL\_SCLK edge.Bit30 dummyBit29..25 UART\_MUX\_4..0 -- to select one of the PMT-basesBIT24..1 AFE\_ENABLE\_23..0 -- high active, ‘1’ = power on, sequential enabling recommendedBIT0 TX\_BROADCAST\_ENABLE -- high active, ‘1’ = MCU\_USART6\_TX is fanout to HV-chan 23..0MCU signal usage:MCU\_AFE\_RST, MCU port PA10, asynchronous reset, high active* UART\_MUX\_4..0=00h, AFE\_ENABLE\_23..0 = 000000h

MCU\_AFE\_SEL MCU port PA9, to distinguish between AFE and mDAB access, high active, AFE\_SEL = ’1’MCU\_CAL\_SS MCU port PE4, low active frame signal (like nCS)MCU\_CAL\_SCLK MCU port PE2, SPI clock, 0..50MHzMCU\_CAL\_MOSI MCU port PE6, SPI dataMCU\_USART6\_RX MCU port PG9, connected to PMT base-TX via UART\_MUXMCU\_USART6\_TX MCU port PG14, connected to PMT base-RX via UART\_MUX HV\_UART\_RX0..23 inputs in standard mode, neither pullup, keeper or SCHMITT\_TRIGGER anymore |
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