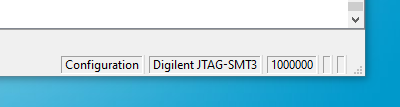
## Programming using ISE Impact

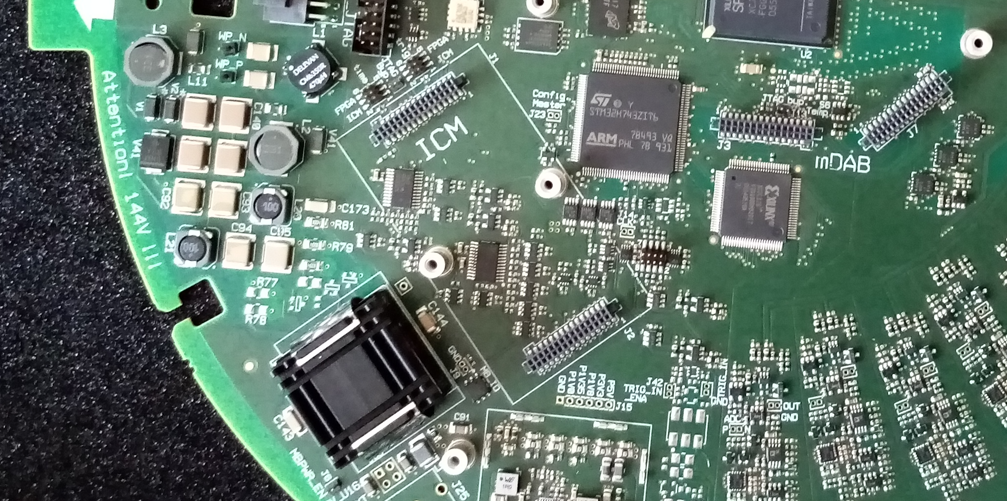
For some reason, at least this is my experience, ISE impact is not recognizing the standard Xilinx programmer ”Platform Cable USB II”, while the Digilent JTAG -SMT-3 worked always. Check the lower left of the ISE Impact window. There should be visible:



If not use the menu: Output/Cable Auto Connect

### Programming w/o ICM and mDAB

Note, for the mainboard Rev.2 it is possible to bypass the unplugged ICM and the unplugged mDAB. To establish the JTAG chain, the jumpers J5 and J13 must be set. To power the mainboard J6 (MBPWR\_EN) must be set as well.



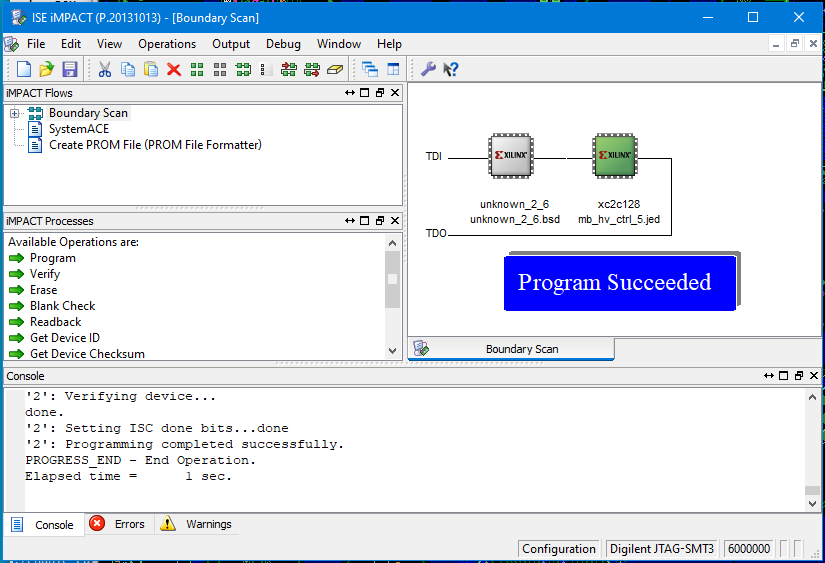
J5

J13

13

J6

Run ISE, start the Impact programmer from Menu / Tools. Do a boundary scan first. With right mouse click in the device field do “Initialize Chain”. You might be enforced to do Edit/Add Device. ISE does not know Spartan7 FPGAs ( while Vivado does not know, how to program CPLDs, unfortunately). Using impact to generated a .bsd file for the mainboard FPGA as a workaround. Use right mouse click on the device icon to assign / program /../ files.



mb\_FPGA

mb\_CPLD

With left / right mouse click assign the configuration files. With right mouse click on the CPLD-icon to initiate the programming.

### Programming with ICM and mDAB being plugged

See above, the jumpers J6, J5 and J13 must be unset. First, run the following command sequence:

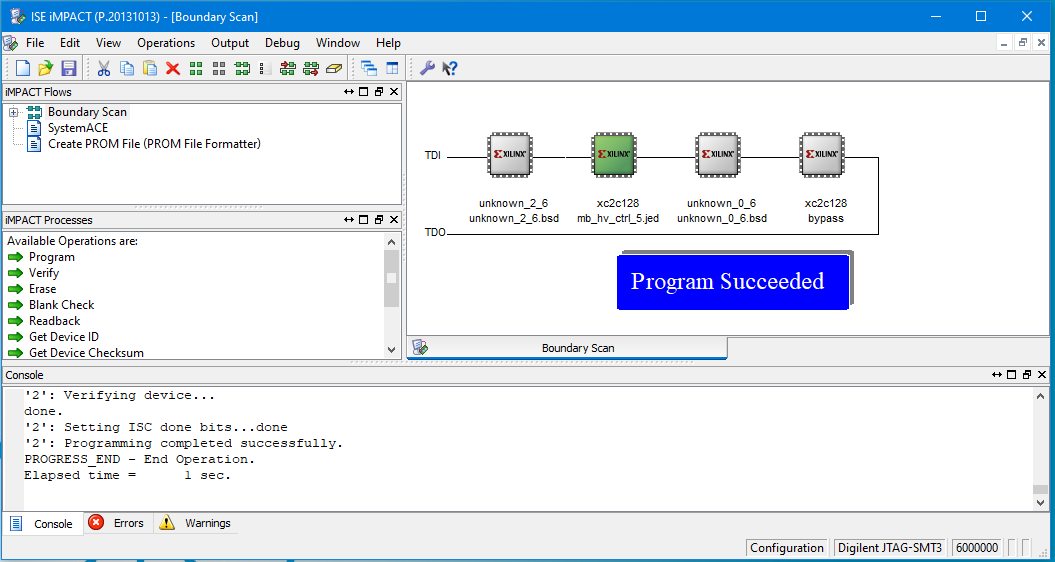
wp\_on.py

icm\_fpga\_reboot.py -w 7 -i 2

lid\_enable.py

./enable\_calibration\_power.py

Run ISE, start the Impact programmer from Menu / Tools. Do a boundary scan first. With right mouse click in the device field do “Initialize Chain”. You might be enforced to do Edit/Add Device. ISE does not know Spartan7 FPGAs ( while Vivado does not know, how to program CPLDs, unfortunately). Using impact to generated a .bsd file for the mainboard FPGA as a workaround. Use right mouse click on the device icon to assign / program /../ files.



mb\_FPGA

mb\_CPLD

ICM\_FPGA

mDAB\_CPLD