# mDAB\_2 Firmware Properties

CPLD: XC2C128-7VQ100

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| **Revision** | **Name** | **Short Description** |
| 1 | mDAB\_2\_ctrl\_1.jed | Implemented the discrete logic, shown in the DEggMBRev4.1- schematic,Added / differences:* FLASH2\_POWER\_ENA = Q2 of the Power Enable Shift Register
* FLASH1..2 brightness control by quad channel 16bit DAC AD5664, used channels: A=FLASH1, B=FLASH2, C=ILUM, DAC= ffffh -> FLASHx\_CHARGE\_BIAS = 15V, ILUM\_CTRL=2.5V
* FLASHx\_CHARGE\_BIAS read back, using 16bit ADC ADS8330 @ MCU\_CAL\_A3..0=8h, with ADC\_CONVSTn @ MCU\_CAL\_A3..0=7h,

All signals are synchronized to the MCU system clock (20MHz)All inputs with pullup + schmitt-trigger |
| 2 | mDAB\_2\_ctrl\_2.jed | * Like rev.1, but signals are NOT synchronized anymore to the MCU system clock (20MHz), CAL\_CLK is not being used

All inputs with pullup + schmitt-trigger |
| 3 | mDAB\_2\_ctrl\_3.jed | Like rev.1, incl. board / firmware rev. readback @ address CAL\_A = 1010, bits\_15..12=board-rev., bits\_11..0=fw-rev. |