# ICM Firmware Properties

FPGA: Xilinx XC7S25-2FTGB196I

FLASH (ISSI, SPIx1x4, 128 Mbit): IS25WP128-JKLE

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| **Revision** | **Name** | **Short Description** |
| 008 | icm\_008 | mDOT comm. @ 2MBd, Rx/Tx buffer: 32KB each, use the signals FPGA\_UART\_RX/TX, for comm. tests disable the mDOT-FPGA and shortcut on mDOT J21-3,4 (signal names there are wrong / mirrored !!!) |
| 009 | icm\_009 | dEgg comm. @ 2MBd, Rx/Tx buffer: 32KB each, use the signals MCU\_USART\_RX/TX, MCU\_BOOT = low, MCU\_nRST = low for ~ 6us after power on else high, INTLK\_0..3=low,  |
| 010 | icm\_010 | like icm\_009 + USB\_RESETn=low to disable the USB-LEDs V7, only relevant for ICM\_1 |
| 011 | icm\_011 | like icm\_011, INTLK\_0..3 set to high now |
| 012 | icm\_012 | improved comm. ADC waveform to ser. decoder |
| 013 | icm\_013 | FPGA\_CLOCK\_P/N, to be used by the mainboards MCU is 20MHz now (was 25MHz before) |
| 014 | icm\_014 | comm. threshold=0.8V, max. cable length=50m (!!!) |
| 015 | icm\_015 | comm. threshold=0.1V, max. cable length=3000m or gen1 3.5km-filterbox |
| 016 | icm\_016 | max. cable length=3000m or gen1 3.5km-filterbox, **AFE-friendly trapezoidal waveform** |
| 017 | icm\_017 | Like 016, but FPGA\_SYNC=50ns every second, synchronous to FPGA\_CLOCK=20MHz, MCU\_nRST = 15us |
| 019 | icm\_019 | Full flow control, when using together with mfh\_icm\_019, uart-mode=RTS/CTS must be configured on both ends !Data are sent in chunks of max. 1KB, the buffer size is 32KB, flow control is active when buffer is filled with 30KB |