ICM datasheet

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List of Abbreviations			
PCB	Printed Circuit Board		
ICM	IceCube Communication Module		
USART	Universal Synchronous/Asynchronous Receiver/Transmitter		
MCU	Micro Controller Unit		
FPGA	Field Programmable Gate Array		
MB	Main Board		
GPIO	General Purpose Input / Output		
INTLK	Interlock		
WP	Wire Pair		
PCA	Penetrator Cable Assembly		

History		
Version	Date	Observation
1.0	2019-01-24	Draft
1.1	2019-10-22	corrected PCA_ID voltage level
1.2	2020-01-17	P1, P2, Signal names harmonized with D-Egg / PDOM schematics
1.3	2020-05-06	Block Diagram corrected, signals CAL_trig, CAL_time connected to P1
1.4	2021-01-04	IceCube upgrade logo used now
1.5	2024-04-12	ICM_1 to ICM_4 differences and test point description added

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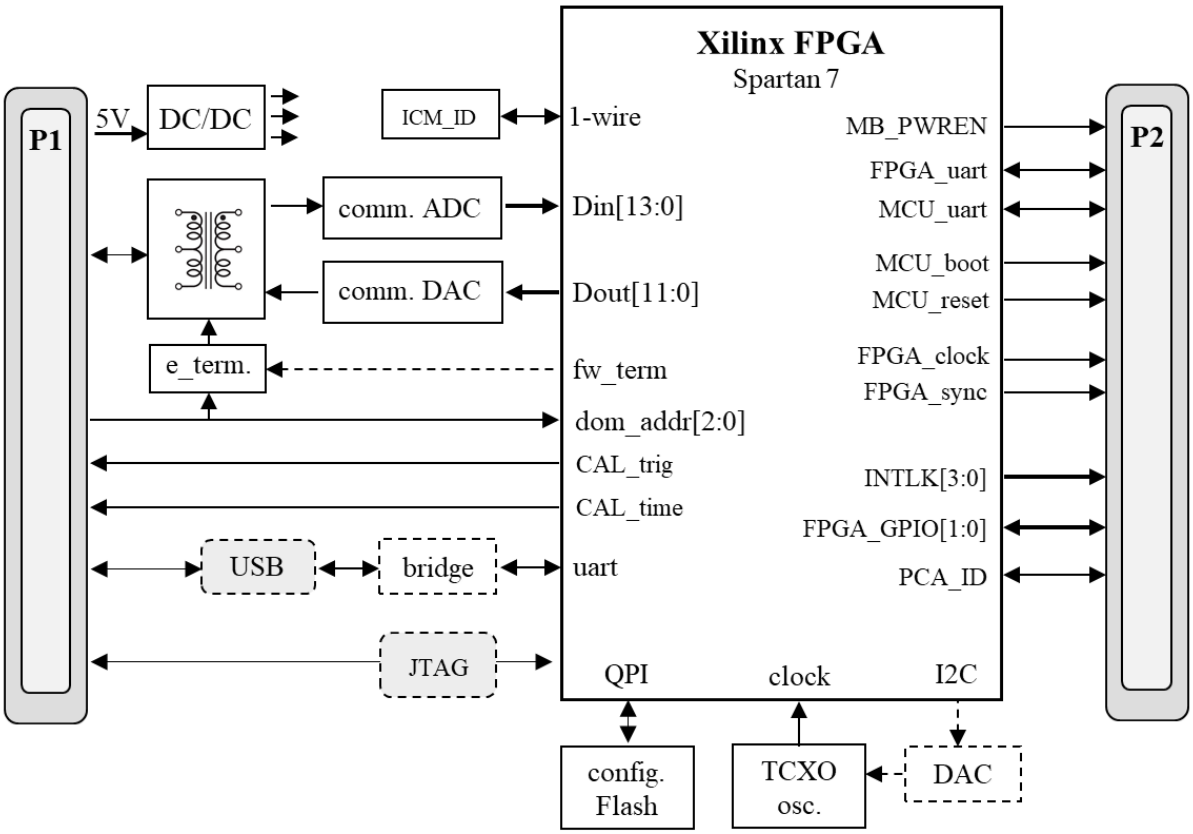
1 Introduction

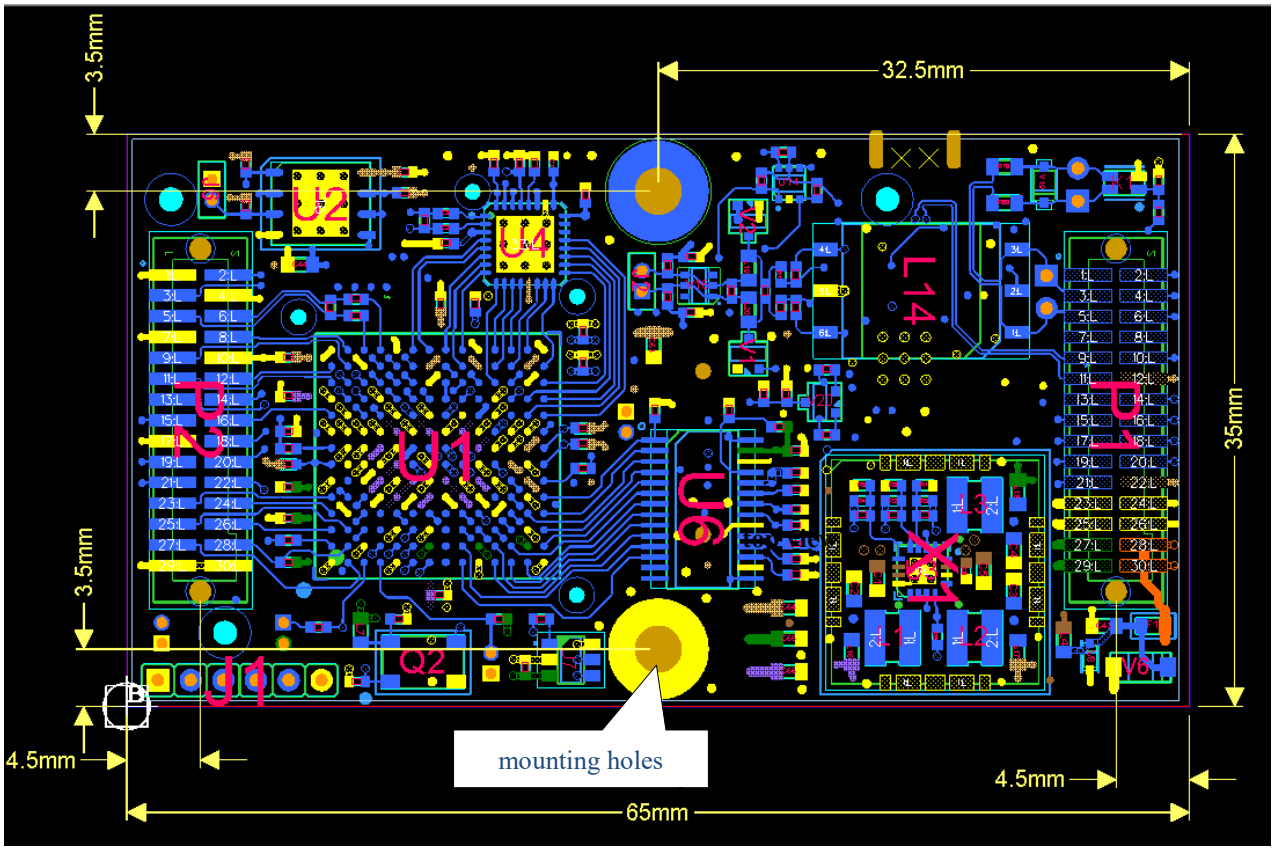
The document is based on a proposal by Perry Sandström. The idea is to use a unique piggy back module for all in ice devices. The main functionality is communication and time calibration.

2 Block Diagram



3 PCB

size	65 mm x 35 mm
thickness	1.6 mm
layers	8
mounting holes	x,y = (32.5, 3.5) + (32.5, 31.5) 2.9 mm drill diameter, metallized, 6 mm top / bottom ring, on GND
standoff	4-40 x 6.35 mm, soldered to mainboard, e.g. Keystone 4883 + screw Keystone 9400 or Wuerth 9774065151 + screw M2.5x5mm, e.g. ETTINGER 01.64.212



4 Connector Types

P1, P2	x,y = (61.5, 17.5) + (4.5, 17.5), Samtec TFM-115-02-S-D-A-K-TR, mates to Samtec SFM-115-02-S-D-A-K-TR (on mainboard)
J3 (optional)	on bottom side, micro USB, terminal and power connection (standalone mode), Hirose ZX62R-B-5P(30)
J4 (optional)	Xilinx Platform Cable USB II Molex 87832-1420

5 Signal Transformer

L14	Coilcraft SWB3010-SMLB

6 Connector Signals

P2					P1			
signal	**pin**	**pin**	**signal**		**signal**	**pin**	**pin**	**signal**
GND	1	2	FPGA_CLOCK_P			1	2	WP_ADR_0
FPGA_CLOCK_N	3	4	GND		WP_P	3	4	WP_ADR_1
FPGA_SYNC_N	5	6	FPGA_SYNC_P		WP_N	5	6	WP_ADR_2
GND	7	8	FPGA_GPIO_0			7	8	
FPGA_GPIO_1	9	10	GND		USB_D_P	9	10	USB_P5V
MCU_USART_CK	11	12	MCU_nRST		USB_D_N	11	12	P1V8
FPGA_UART_TX	13	14	FPGA_UART_RX			13	14	TDI
FPGA_UART_RTS	15	16	FPGA_UART_CTS		CAL_TRIG_P	15	16	TDO
GND	17	18	MCU_BOOT		CAL_TRIG_N	17	18	TCK
MCU_USART_TX	19	20	MCU_USART_RX		CAL_TIME_P	19	20	TMS
MCU_USART_RTS	21	22	MCU_USART_CTS		CAL_TIME_N	21	22	P1V8
MBPWR_EN	23	24	INTLK_0		GND	23	24	GND
INTLK_1	25	26	INTLK_2		GND	25	26	GND
INTLK_3	27	28	PCA_ID		P3V3	27	28	P5V_IN
GND	29	30	GND		P3V3	29	30	P5V_IN

7 Signal Description

7.1 Connector P1, Signals

Name	Direction	Voltage Level	Remark
WP_P	bidir.	analog	AC (comm.) part of the in ice quads wire pair signal
WP_N			
WP_ADR_0..2	in	3.3V	DOM address select bits, 10K pullups to 3.3V, B"111" activates the 150 ohm line termination, for address decoding connected to the FPGA as well
USB_D_P	bidir	digital	USB connector signals, can be used for a USB-B connector, placed on the mainboard
USB_D_N			
USB_P5V	in	5V	+5V by the USB master, used to power the USB to UART bridge chip (FT2322RQ)
TDI	in	1.8V LVCMOS	FPGA JTAG signals, connect (optional) to a 2x7 pin, 2mm pitch, vertical box header on the mainboard, according to the XILINX Platform Cable USB II definition
TDO	out		
TMS	in		
TCK	in		
P1V8	out		+1.8V by onboard DC/DC, 500 mA max. load, voltage reference for the XILINX Platform Cable
CAL_TRIG_P	out	1.8V LVDS signal	Trigger pulse
CAL_TRIG_N	out		
CAL_TIME_P	out	1.8V LVDS signal	Timer synchronization pulse
CAL_TIME_N	out		
P3V3	out	3.3V	+3.3V by onboard DC/DC, 500 mA max. load
P5V_IN	in	5V	+5V by mainbord DC/DC average current : TBD (< 200 mA expected) peak current : TBD
GND			mainboard ground, P5V_IN return

7.2 Connector P2, Signals

Name	Direction	Voltage Level	Remark
FPGA_CLOCK_P	Out	1.8V LVDS	20MHz, 0.4V diff., Vocm=0.9V, use 100 ohm termination, receiver can also use LVDS_25 inputs
FPGA_CLOCK_N			
FPGA_SYNC_N	Out	1.8V LVDS	0.46 diff., Vocm=0.9V, use 100 ohm termination, receiver can also use LVDS_25 inputs
FPGA_SYNC_P			
FPGA_GPIO_0	Bidir	1.8V	general purpose I/O, can also be used as diff., connect to mainboard FPGA
FPGA_GPIO_1			
MCU_USART_CK	Out	1.8V LVCMOS	MCU USART clock
MCU_nRST	Out	1.8V LVCMOS	MCU low active reset
FPGA_UART_TX	In	1.8V LVCMOS	connect to mainboard FPGA, signal direction by ICM FPGA view
FPGA_UART_RX	Out		
FPGA_UART_RTS	In		buffer status
FPGA_UART_CTS	Out		buffer status
MCU_BOOT	Out	1.8V LVCMOS	connect to STM32H743 boot pin
MCU_USART_TX	In		e.g., connect to STM32H743 USART3_TX, pin 46
MCU_USART_RX	Out		e.g., connect to STM32H743 USART3_RX, pin 47
MCU_USART_RTS	In		e.g., connect to STM32H743 USART3_TX, pin 53
MCU_USART_CTS	Out		e.g., connect to STM32H743 USART3_TX, pin 52
MBPWR_EN	Out	3.3V LVCMOS	mainboard power enable (on / off)
INTLK_0	Out	3.3V LVCMOS	Interlock 0...3
INTLK_1	Out		
INTLK_2	Out		
INTLK_3	Out		
PCA_ID	Bidir	3.3V open drain	connect to 1-wire mainboard ID EEPROM

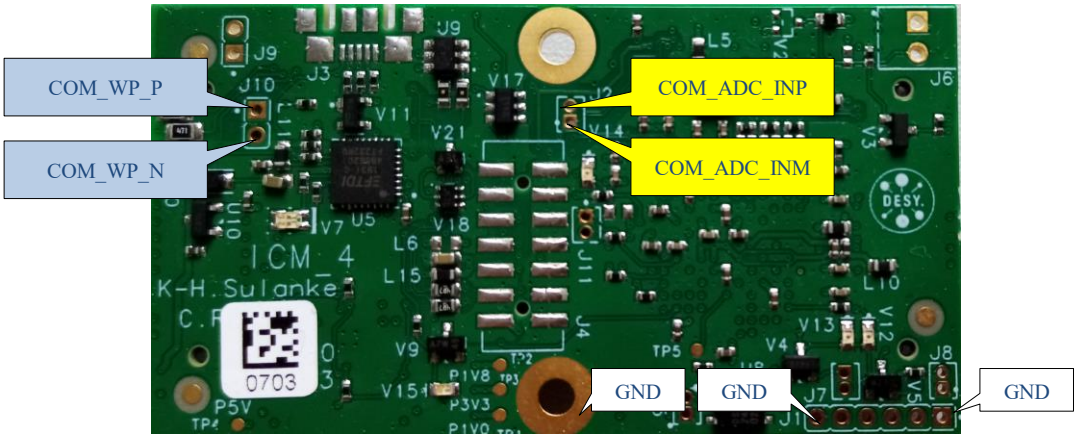
8 ICM_1 to ICM_4, Differences

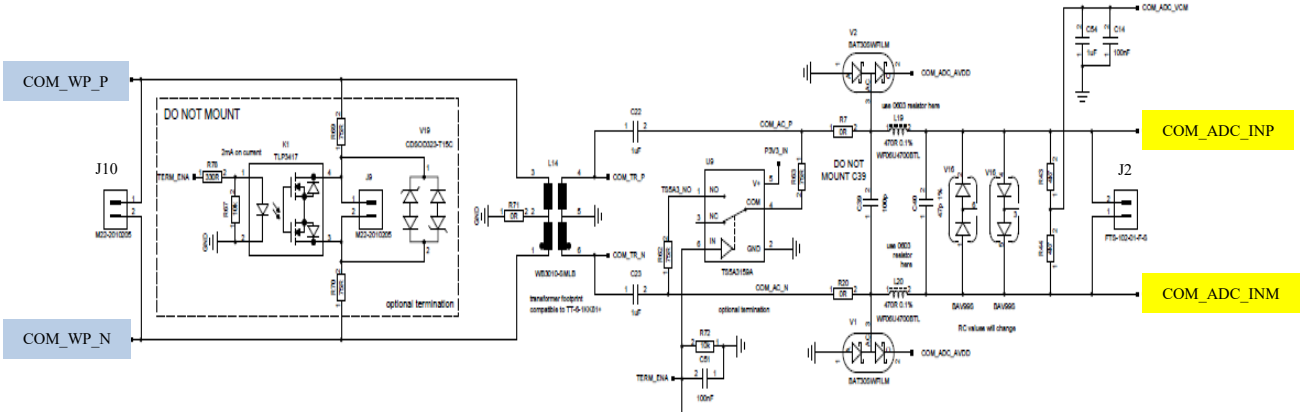
item	ICM_1	ICM_2	ICM_3	ICM_4	remark
JTAG interface, J4 TCK pull-up resistor	**330R**	**330R**	1k	1k	The low-cost programmer **JTAG-HS3** has very weak drivers. The config. partly failed, when additional parts (mainboard-FPGA) were in the JTAG chain, due to the too low 330R value at ICM_1, _2.
FPGA input **PUDC_B**	GND	**GND** Check if your MBPWR_EN has a pull-down of ~1K (330uA x 1k = 0.33V)	P1V8	P1V8	**GND**: all I/Os with weak pull-up while configuration See below min. / max. pull-up current vs. VCCO: V_{CCO} = 3.3V. 90 – 330 µA V_{CCO} = 2.5V. 68 – 250 µA V_{CCO} = 1.8V. 34 – 220 µA V_{CCO} = 1.5V. 23 – 150 µA V_{CCO} = 1.2V. 12 – 120 µA **P1V8**, (for ICM_3, _4 mounting option, R48=DNL) all I/Os are floating while configuration
Con. P1, pins 15,17,19,21 Signal names and termination scheme	MB_GPIO_0..3 MB_GPIO_0/_1 MB_GPIO_2/_3 by **3.3V** FPGA bank_ 34, Each signal with 47R serial termination	CAL_TRIG_P/N, CAL_TIME_P/N Driven by **1.8V** FPGA bank_14 Each pair with 100R parallel termination			For **ICM_1 other FPGA pins** are being used !!! When using ICM_2..4 in the **mini_Fieldhub, R81, R82** have to be removed before!
Flash write protection Signal D02_nWP	Permanently pull-up to P1V8 by R16 (4k7), pull down to GND per Jumper J6		Permanently pulled down by R16 (4k7), C85 (100nF) to P1V8 for debouncing. ICM_4 allows to readback the D02_nWP signal via FPGA pin D10		Use J6 to connect an infrared photo-transistor, e.g. 1540601NEA200. (1540601NEA200 is hand-soldered on J6 pads) Disable the write protection using an infrared lamp (~900nm).
Signal **PCA_ID** (MB_ID)	MB_ID w/o pull-up	PCA_ID with 1k pull-up (R83)			Not sure why the name got changed to PCA_ID
Comm. ADC, diff. anlog input filter	2x(2x47R+100pF)	1x (2x470R + 47pF)			Check individual ICM_1 for possible changes

9 ICM_x Test Points

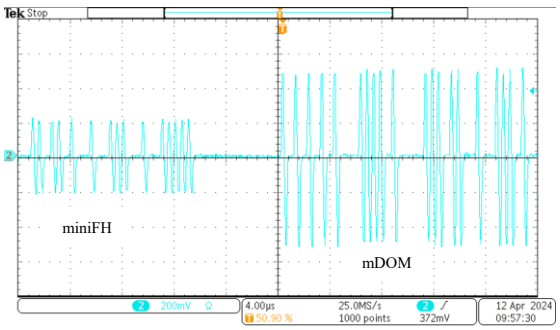
9.1 Communcation, unfiltered Wire Pair and filtered ADC Input signal

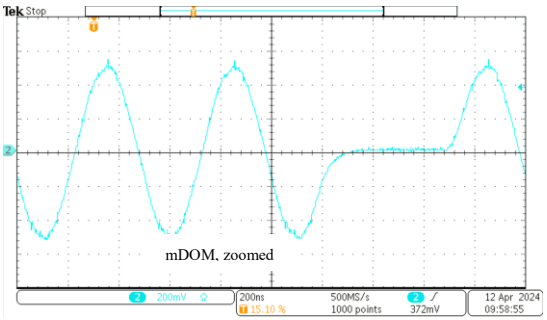
Best, use a differential probe. Or two single ended probes + GND connection in differential math-mode.





E.g., the half duplex comms. signal, measured at J2 at an mDOM-ICM, using a 1.5m 100ohm twisted pair cable and a diff. probe (Tektronix P6247).





9.2 Power Supply

See the test points below. Use a multimeter or the scope.