|  |
| --- |
| **ICM datasheet** |

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Author** | *Laboratory* |  | **Approved by** | *Laboratory* |
| Karl-Heinz Sulanke DESY | |  |  | |
|  | |  |  | |
|  | |  |  | |

|  |  |  |  |
| --- | --- | --- | --- |
| **List of Abbreviations** | | | |
| PCB | Printed Circuit Board |  |  |
| ICM | IceCube Communication Module |  |  |
| USART | Universal Synchronous/Asynchronous Receiver/Transmitter |  |  |
| MCU | Micro Controller Unit |  |  |
| FPGA | Field Programmable Gate Array |  |  |
| MB | Main Board |  |  |
| GPIO | General Purpose Input / Output |  |  |
| INTLK | Interlock |  |  |
| WP | Wire Pair |  |  |
| PCA | Penetrator Cable Assembly |  |  |

|  |  |  |
| --- | --- | --- |
| **History** | | |
| Version | Date | Observation |
| 1.0 | 2019-01-24 | Draft |
| 1.1 | 2019-10-22 | corrected PCA\_ID voltage level |
| 1.2 | 2020-01-17 | P1, P2, Signal names harmonized with D-Egg / PDOM schematics |
| 1.3 | 2020-05-06 | Block Diagram corrected, signals CAL\_trig, CAL\_time connected to P1 |
| 1.4 | 2021-01-04 | IceCube upgrade logo used now |
| 1.5 | 2024-04-12 | ICM\_1 to ICM\_4 differences and test point description added |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |
|  |  |  |

**Table of Contents**

[1 Introduction 4](#_Toc163813529)

[2 Block Diagram 4](#_Toc163813530)

[3 PCB 5](#_Toc163813531)

[4 Connector Types 6](#_Toc163813532)

[5 Signal Transformer 6](#_Toc163813533)

[6 Connector Signals 6](#_Toc163813534)

[7 Signal Description 7](#_Toc163813535)

[7.1 Connector P1, Signals 7](#_Toc163813536)

[7.2 Connector P2, Signals 8](#_Toc163813537)

[8 ICM\_1 to ICM\_4, Differences 9](#_Toc163813538)

[9 ICM\_x Test Points 10](#_Toc163813539)

[9.1 Communcation, unfiltered Wire Pair and filtered ADC Input signal 10](#_Toc163813540)

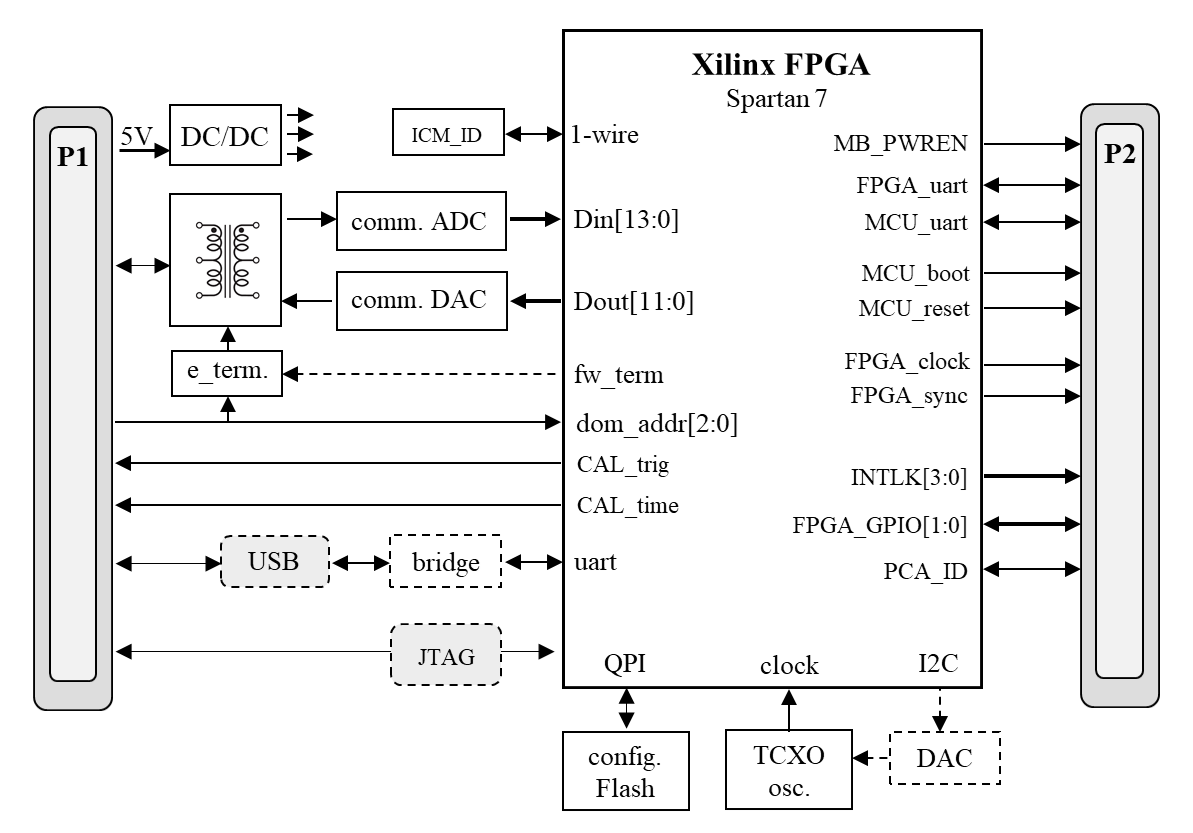
[9.2 Power Supply 11](#_Toc163813541)

**List of Figures**

# Introduction

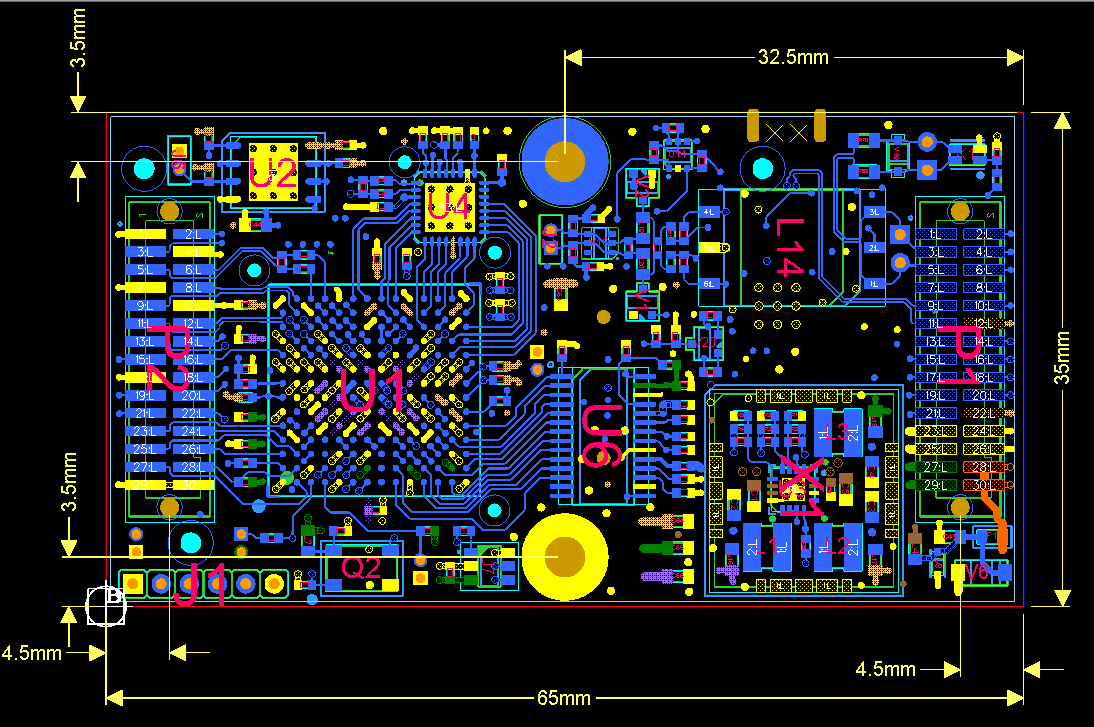
The document is based on a proposal by Perry Sandström. The idea is to use a unique piggy back module for all in ice devices. The main functionality is communication and time calibration.

# Block Diagram



# PCB

|  |  |
| --- | --- |
| size | 65 mm x 35 mm |
| thickness | 1.6 mm |
| layers | 8 |
| mounting holes | x,y = (32.5, 3.5) + (32.5, 31.5) 2.9 mm drill diameter, metallized, 6 mm top / bottom ring, on GND |
| standoff | 4-40 x 6.35 mm, soldered to mainboard,  e.g. Keystone 4883 + screw Keystone 9400  or Wuerth 9774065151 + screw M2.5x5mm, e.g. ETTINGER 01.64.212 |



mounting holes

**top view**

**bottom side, viewing into P1, P2**

# Connector Types

|  |  |
| --- | --- |
| P1, P2 | x,y = (61.5, 17.5) + (4.5, 17.5), Samtec TFM-115-02-S-D-A-K-TR,  mates to Samtec SFM-115-02-S-D-A-K-TR (on mainboard) |
| J3 (optional) | on bottom side, micro USB, terminal and power connection (standalone mode), Hirose ZX62R-B-5P(30) |
| J4 (optional) | Xilinx Platform Cable USB II Molex 87832-1420 |

# Signal Transformer

|  |  |
| --- | --- |
| L14 | Coilcraft SWB3010-SMLB |

# Connector Signals

|  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- |
| **P2** | | | |  | **P1** | | | |
| **signal** | **pin** | **pin** | **signal** |  | **signal** | **pin** | **pin** | **signal** |
| GND | 1 | 2 | FPGA\_CLOCK\_P |  |  | 1 | 2 | WP\_ADR\_0 |
| FPGA\_CLOCK\_N | 3 | 4 | GND |  | WP\_P | 3 | 4 | WP\_ADR\_1 |
| FPGA\_SYNC\_N | 5 | 6 | FPGA\_SYNC\_P |  | WP\_N | 5 | 6 | WP\_ADR\_2 |
| GND | 7 | 8 | FPGA\_GPIO\_0 |  |  | 7 | 8 |  |
| FPGA\_GPIO\_1 | 9 | 10 | GND |  | USB\_D\_P | 9 | 10 | USB\_P5V |
| MCU\_USART\_CK | 11 | 12 | MCU\_nRST |  | USB\_D\_N | 11 | 12 | P1V8 |
| FPGA\_UART\_TX | 13 | 14 | FPGA\_UART\_RX |  |  | 13 | 14 | TDI |
| FPGA\_UART\_RTS | 15 | 16 | FPGA\_UART\_CTS |  | CAL\_TRIG\_P | 15 | 16 | TDO |
| GND | 17 | 18 | MCU\_BOOT |  | CAL\_TRIG\_N | 17 | 18 | TCK |
| MCU\_USART\_TX | 19 | 20 | MCU\_USART\_RX |  | CAL\_TIME\_P | 19 | 20 | TMS |
| MCU\_USART\_RTS | 21 | 22 | MCU\_USART\_CTS |  | CAL\_TIME\_N | 21 | 22 | P1V8 |
| MBPWR\_EN | 23 | 24 | INTLK\_0 |  | GND | 23 | 24 | GND |
| INTLK\_1 | 25 | 26 | INTLK\_2 |  | GND | 25 | 26 | GND |
| INTLK\_3 | 27 | 28 | PCA\_ID |  | P3V3 | 27 | 28 | P5V\_IN |
| GND | 29 | 30 | GND |  | P3V3 | 29 | 30 | P5V\_IN |

# Signal Description

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Connector P1, Signals  |  |  |  |  | | --- | --- | --- | --- | | **Name** | **Direction** | **Voltage Level** | **Remark** | | WP\_P | bidir. | analog | AC (comm.) part of the in ice quads wire pair signal | | WP\_N | |  |  |  |  | | WP\_ADR\_0..2 | in | 3.3V | DOM address select bits, 10K pullups to 3.3V, B”111” activates the 150 ohm line termination, for address decoding connected to the FPGA as well | |  |  |  |  | | USB\_D\_P | bidir | digital | USB connector signals, can be used for a USB-B connector, placed on the mainboard | | USB\_D\_N | | USB\_P5V | in | 5V | +5V by the USB master, used to power the USB to UART bridge chip (FT2322RQ) | |  |  |  |  | | TDI | in | 1.8V LVCMOS | FPGA JTAG signals, connect (optional) to a 2x7 pin, 2mm pitch, vertical box header on the mainboard, according to the XILINX Platform Cable USB II definition | | TDO | out | | TMS | in | | TCK | in | | P1V8 | out |  | +1.8V by onboard DC/DC, 500 mA max. load, voltage reference for the XILINX Platform Cable | | CAL\_TRIG\_P | out | 1.8V  LVDS signal | Trigger pulse | | CAL\_TRIG\_N | out | | CAL\_TIME\_P | out | 1.8V  LVDS signal | Timer synchronization pulse | | CAL\_TIME\_N | out | |  |  |  |  | | P3V3 | out | 3.3V | +3.3V by onboard DC/DC, 500 mA max. load | | P5V\_IN | in | 5V | +5V by mainbord DC/DC  average current : TBD (< 200 mA expected) peak current : TBD | | GND |  |  | mainboard ground, P5V\_IN return | |

|  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- | --- |
| Connector P2, Signals  |  |  |  |  | | --- | --- | --- | --- | | **Name** | **Direction** | **Voltage Level** | **Remark** | | FPGA\_CLOCK\_P | Out | 1.8V LVDS | 20MHz, 0.4V diff., Vocm=0.9V, use 100 ohm termination, receiver can also use LVDS\_25 inputs | | FPGA\_CLOCK\_N | |  |  |  |  | | FPGA\_SYNC\_N | Out | 1.8V LVDS | 0.46 diff., Vocm=0.9V, use 100 ohm termination, receiver can also use LVDS\_25 inputs | | FPGA\_SYNC\_P | |  |  |  |  | | FPGA\_GPIO\_0 | Bidir | 1.8V | general purpose I/O, can also be used as diff., connect to mainboard FPGA | | FPGA\_GPIO\_1 | | MCU\_USART\_CK | Out | 1.8V LVCMOS | MCU USART clock | | MCU\_nRST | Out | 1.8V LVCMOS | MCU low active reset | |  |  |  |  | | FPGA\_UART\_TX | In | 1.8V LVCMOS | connect to mainboard FPGA, signal direction by ICM FPGA view | | FPGA\_UART\_RX | Out | | FPGA\_UART\_RTS | In | buffer status | | FPGA\_UART\_CTS | Out | buffer status | |  |  |  |  | | MCU\_BOOT | Out | 1.8V LVCMOS | connect to STM32H743 boot pin | | MCU\_USART\_TX | In | e.g., connect to STM32H743 USART3\_TX, pin 46 | | MCU\_USART\_RX | Out | e.g., connect to STM32H743 USART3\_RX, pin 47 | | MCU\_USART\_RTS | In | e.g., connect to STM32H743 USART3\_TX, pin 53 | | MCU\_USART\_CTS | Out | e.g., connect to STM32H743 USART3\_TX, pin 52 | |  |  |  |  | | MBPWR\_EN | Out | 3.3V LVCMOS | mainboard power enable (on / off) | |  |  |  |  | | INTLK\_0 | Out | 3.3V LVCMOS | Interlock 0...3 | | INTLK\_1 | Out | | INTLK\_2 | Out | | INTLK\_3 | Out | | PCA\_ID | Bidir | 3.3V open drain | connect to 1-wire mainboard ID EEPROM | |
|  |

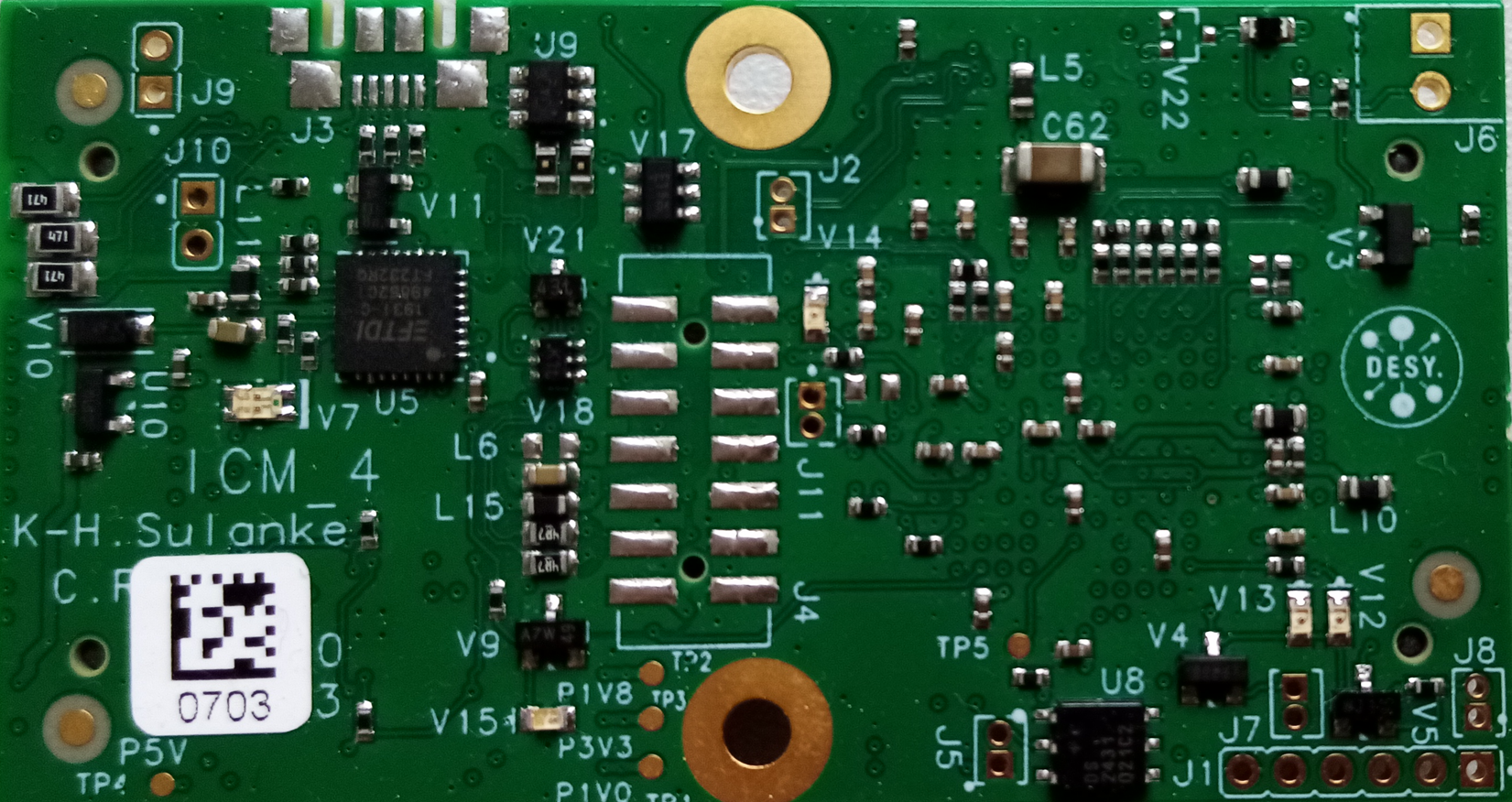
# ICM\_1 to ICM\_4, Differences

|  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- |
| **item** | **ICM\_1** | **ICM\_2** | **ICM\_3** | | **ICM\_4** | **remark** |
| **JTAG interface, J4**  TCK pull-up resistor | **330R** | **330R** | 1k | | 1k | The low-cost programmer **JTAG-HS3** has very weak drivers. The config. partly failed, when additional parts (mainboard-FPGA) were in the JTAG chain, due to the too low 330R value at ICM\_1, \_2. |
| FPGA input **PUDC\_B** | GND | **GND**  Check if your MBPWR\_EN has a pull-down of ~1K  (330uA x 1k = 0.33V) | P1V8 | | P1V8 | **GND**: all I/Os with weak pull-up while configuration  See below min. / max. pull-up current vs. VCCO:    **P1V8**, (for ICM\_3, \_4 mounting option, R48=DNL)  all I/Os are floating while configuration |
| **Con. P1, pins 15,17,19,21**  Signal names and termination scheme | MB\_GPIO\_0..3  MB\_GPIO\_0/\_1 MB\_GPIO\_2/\_3 by **3.3V** FPGA  bank\_ 34,  Each signal with 47R serial termination | CAL\_TRIG\_P/N, CAL\_TIME\_P/N  Driven by **1.8V** FPGA bank\_14  Each pair with 100R parallel termination | | | | For **ICM\_1 other FPGA pins** are being used !!!  When using ICM\_2..4 in the **mini\_Fieldhub, R81, R82** have to be removed before! |
| **Flash write protection**  Signal D02\_nWP | Permanently pull-up to P1V8 by R16 (4k7), pull down to GND per Jumper J6 | | | Permanently pulled down by R16 (4k7), C85 (100nF) to P1V8 for debouncing. ICM\_4 allows to readback the D02\_nWP signal via FPGA pin D10 | | Use J6 to connect an infrared photo-transistor, e.g.  1540601NEA200. (1540601NEA200 is hand-soldered on J6 pads)  Disable the write protection using an infrared lamp (~900nm). |
| Signal **PCA\_ID**  (MB\_ID) | MB\_ID w/o pull-up | PCA\_ID with 1k pull-up (R83) | | | | Not sure why the name got changed to PCA\_ID |
| Comm. ADC, diff. anlog input filter | 2x(2x47R+100pF) | 1x (2x470R + 47pF) | | | | Check individual ICM\_1 for possible changes |

# ICM\_x Test Points

## Communcation, unfiltered Wire Pair and filtered ADC Input signal

Best, use a differential probe. Or two single ended probes + GND connection in differential math-mode.



COM\_ADC\_INM

COM\_ADC\_INP

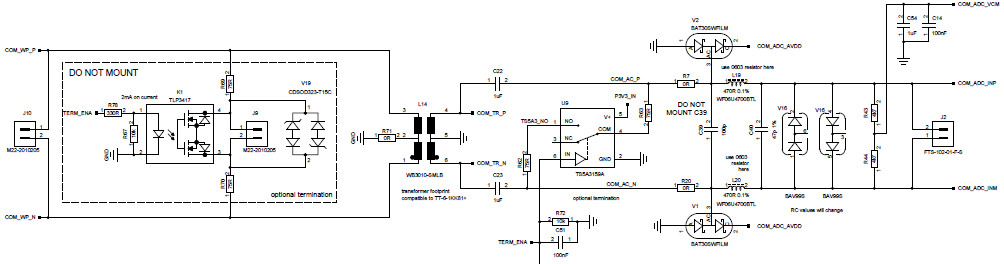
COM\_WP\_P

COM\_WP\_N

GND

GND

GND



COM\_WP\_P

COM\_WP\_N

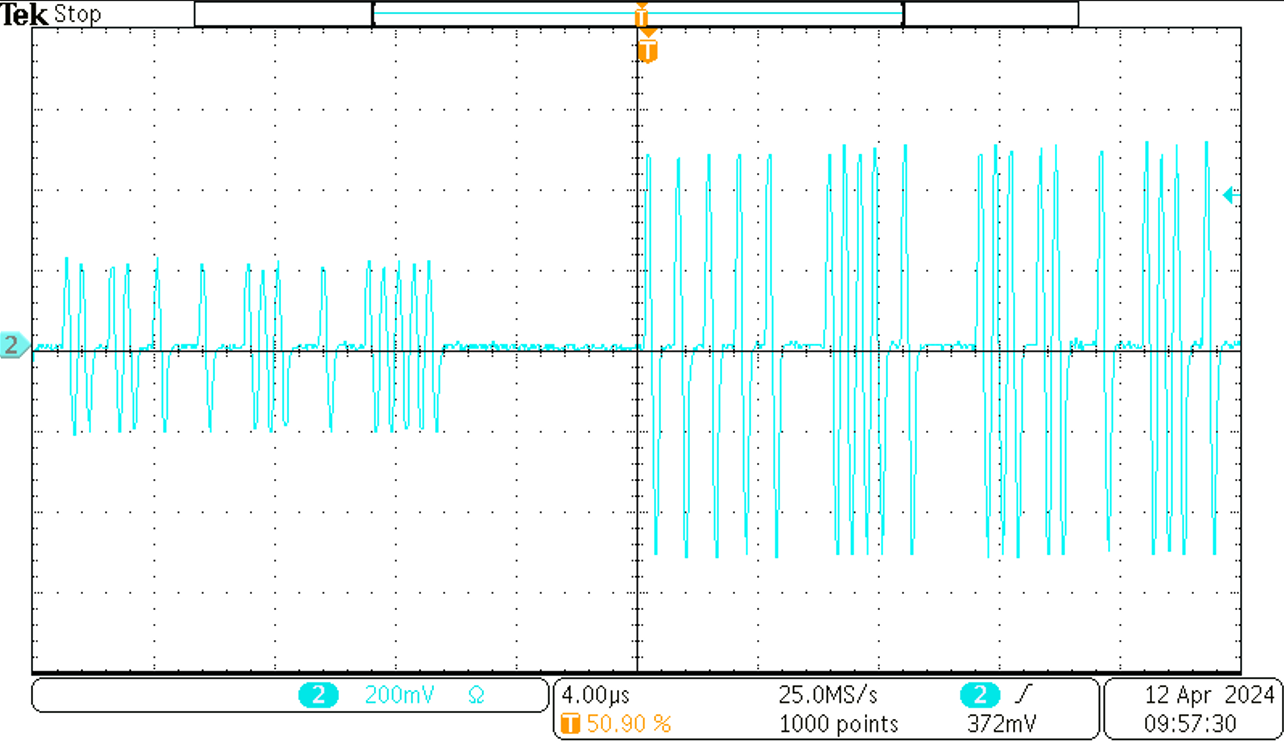
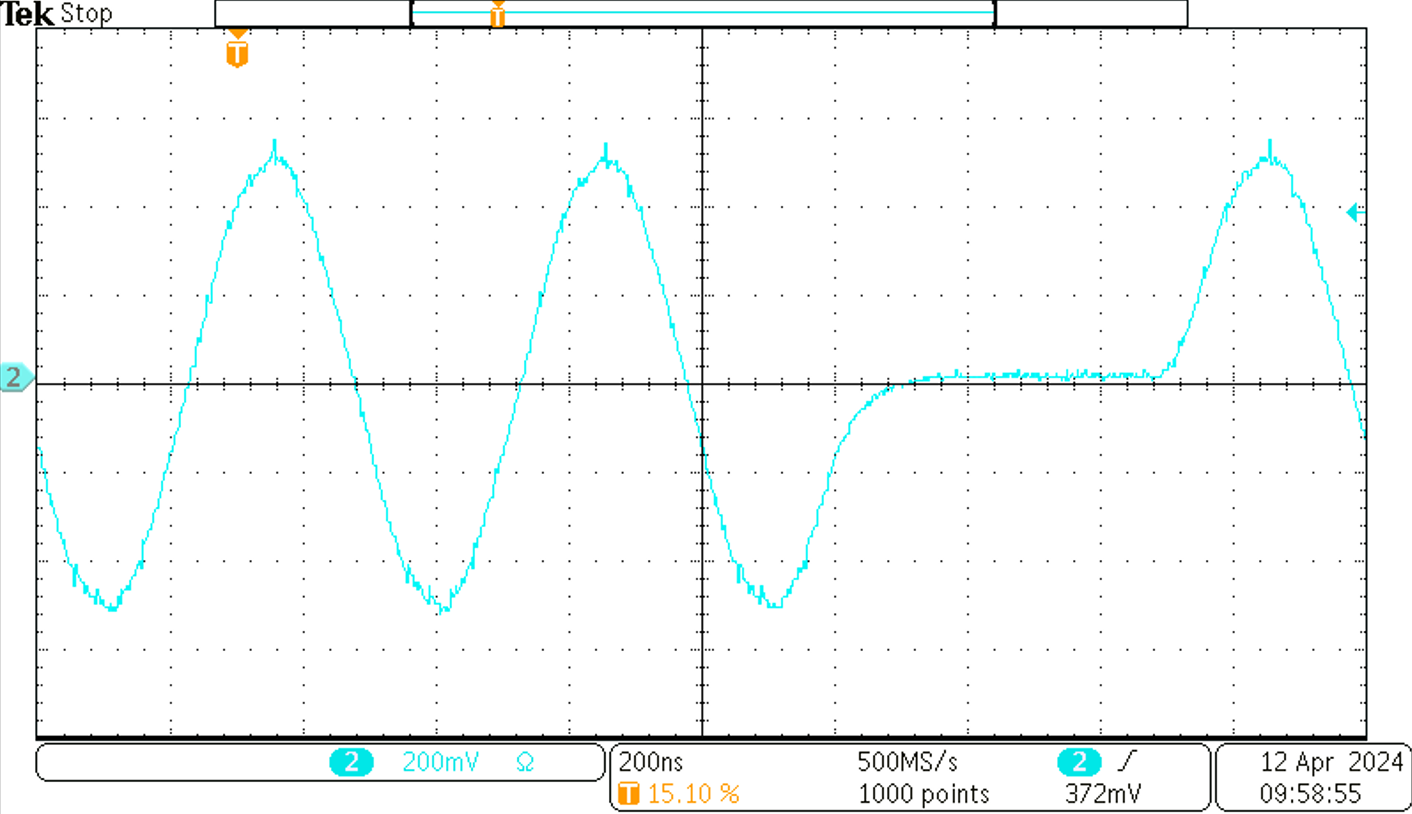
COM\_ADC\_INP

COM\_ADC\_INM

J10

J2

E.g., the half duplex comms. signal, measured at J2 at an mDOM-ICM, using a 1.5m 100ohm twisted pair cable and a diff. probe (Tektronix P6247).



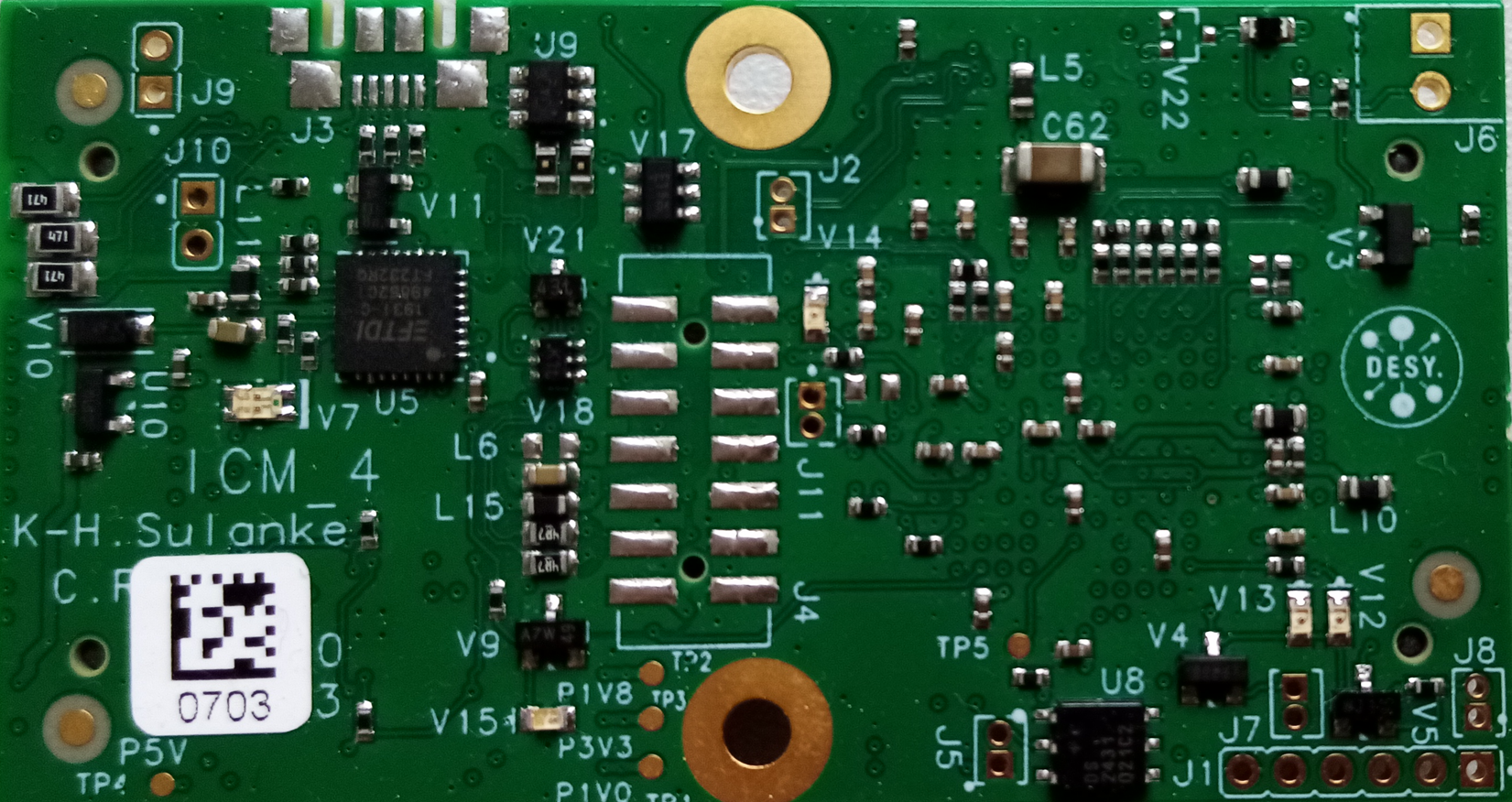
miniFH

mDOM

mDOM, zoomed

## Power Supply

See the test points below. Use a multimeter or the scope.



GND

GND

GND

1.8V

3.3V

1.0V

5V

