# FCON\_3, Boot-Issue Fix

Issue: about 20..30% not boot after power-on, the message “A2” on the screen instead, meaning no mass storage device detected.

The following seemed to be the issue:

The P3V3 / FPGA up delay, while the SBC is already under power.

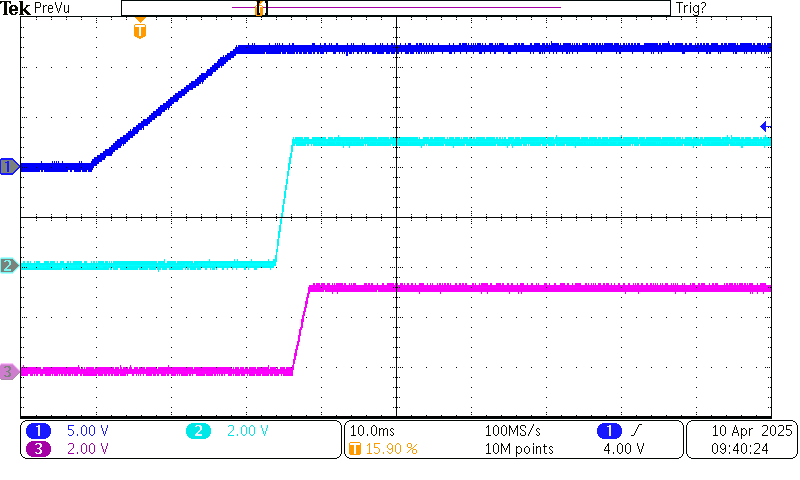
At this point the signal PWR\_OK had an undefined level, not low like required.

1. I fixed this by changing R181 to 300R, 90° rotated, pin-1 on GND, using it as a PWR\_OK-pull-down now.
2. to get an early P3V3-up I changed R15 to a 2.4V zener-diode
3. to further accelerate the P3V3 ramp up I changed both,  C3 (1uF) and C15 (100nF) to 10nF

## Schematic changes to resolve the boot from PCIe-SSD issue

|  |  |  |  |
| --- | --- | --- | --- |
| Vref | Old value | New value | Remark |
|  |  |  |  |
| R181 | 330R 0603 | 300R 0603, pin1 to GND | To GND (!!!) bei 90° rotation, clean signal after P12V-on now, activated by FPGA after 1.4s |
| C3 | 1u 0603 | 10n 0603 | P5V, U1 / TRACK\_SS, to accelerate P5V-up |
| R15 | 620R 0603 | MM3Z2V4T1G | 2.4V Zener diode, MPQ-PG accelerated |
| C15 | 100n 0603 | 10n 0603 | P3V3, U4 / TRACK\_SS, to accelerate P3V3-up |

The 12V / 5V /3.3V  power-up sequence now:

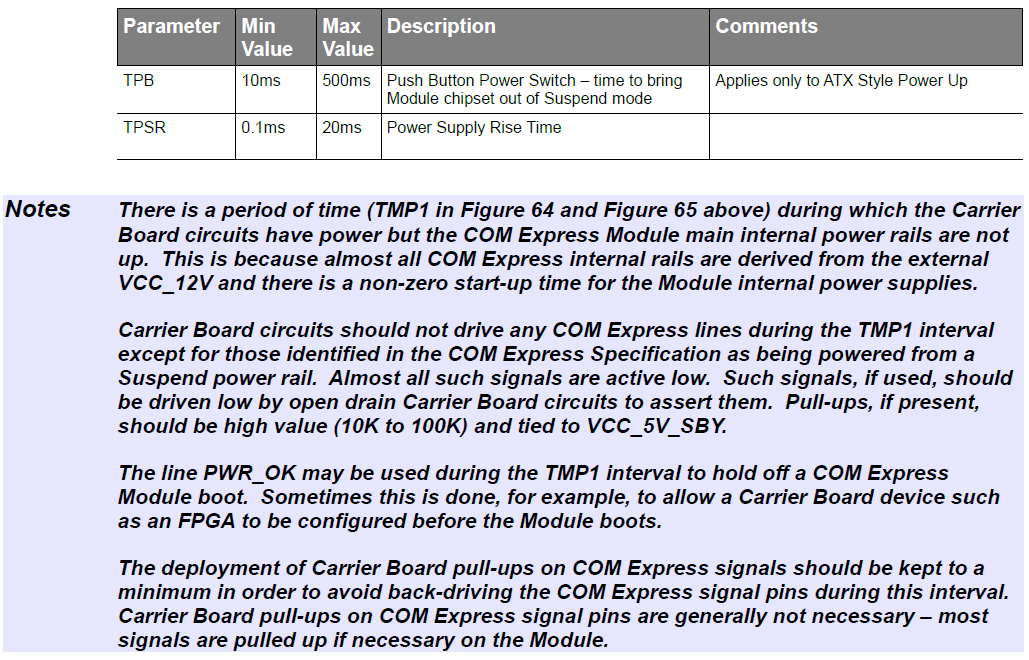
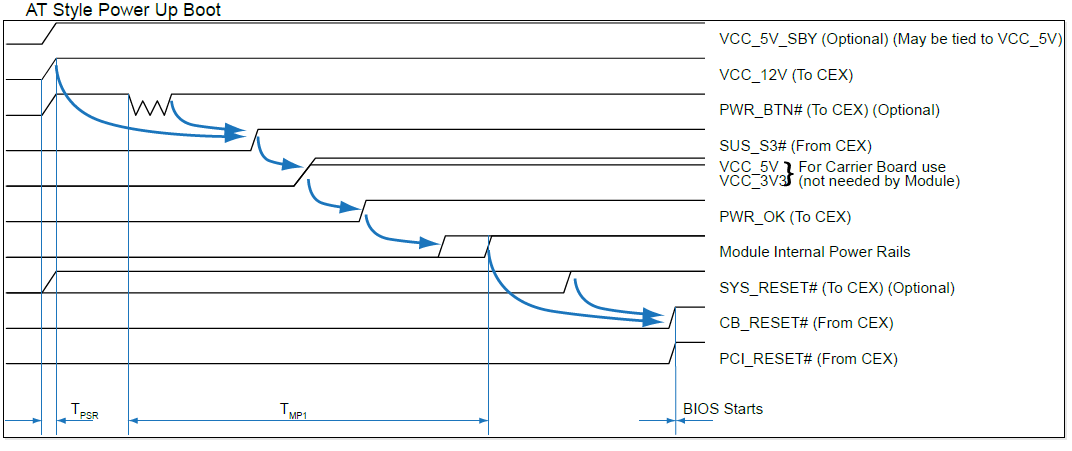


P12V

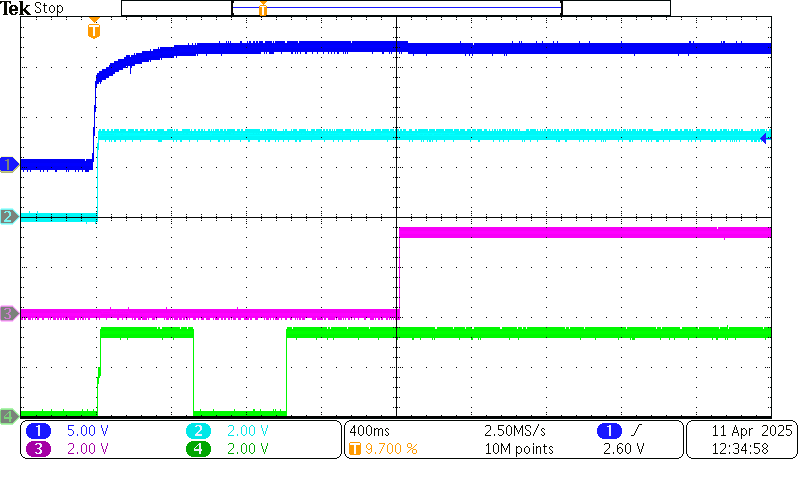
P5V

P3V3

According to the PICMG documentation:



The PWR\_OK / PWRBTn signal sequence, driven by the FPGA, firmware rev. 07:



P12V

P3V3

PWR\_OK

PWRBTn

SYS\_RESETn = high