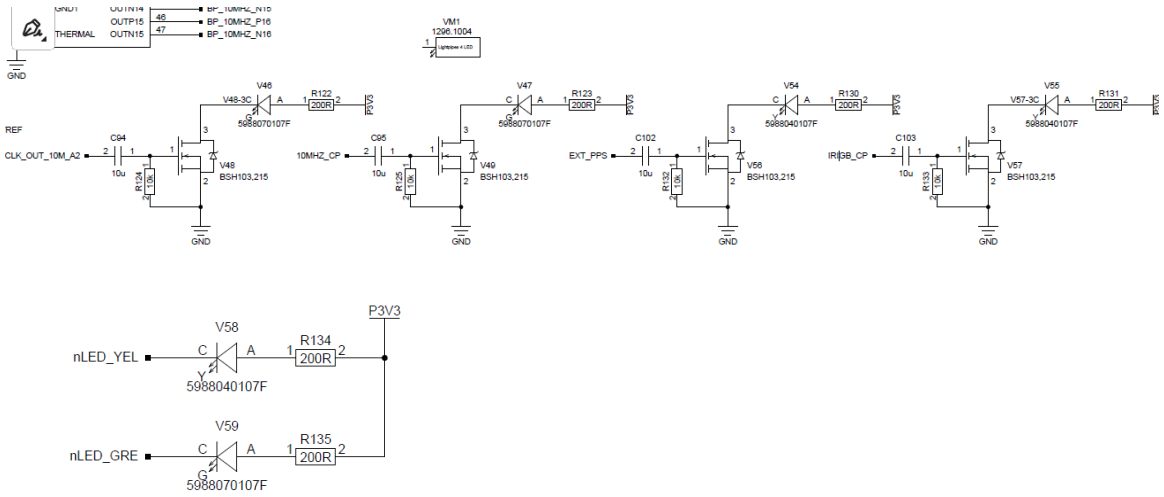
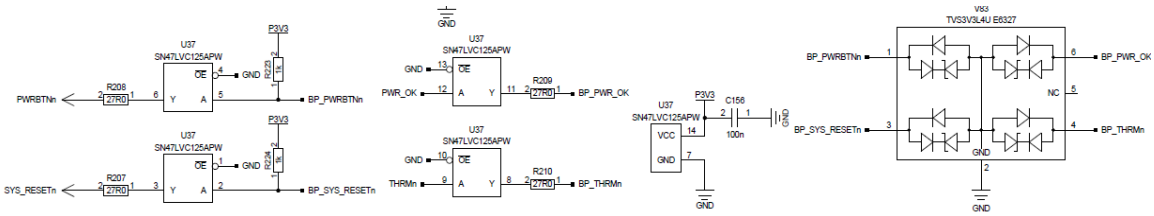
FCON rev.2 to rev.2 changes

Schematic

1. CPLD replaced by FPGA XC7S25-2FTGB196I
2. Added FPGA-flash MT25QL128ABA1EW9-0SIT + circuitry
3. Added DC/DC 3.3V to 1V, SC189ZSKTRT (FPGA core voltage)
4. CLKREQn circuitry, J25, R154 removed
5. Tricolor frontplate LED ASMB-MTB1-0B3A2 + ligh-pipe 515-1255-0590-F added
6. Backplane connector J20, pins B77..88 reassigned to BP_FANx_SENSE, 4x SBC signal removed
7. The following LEDs + control removed



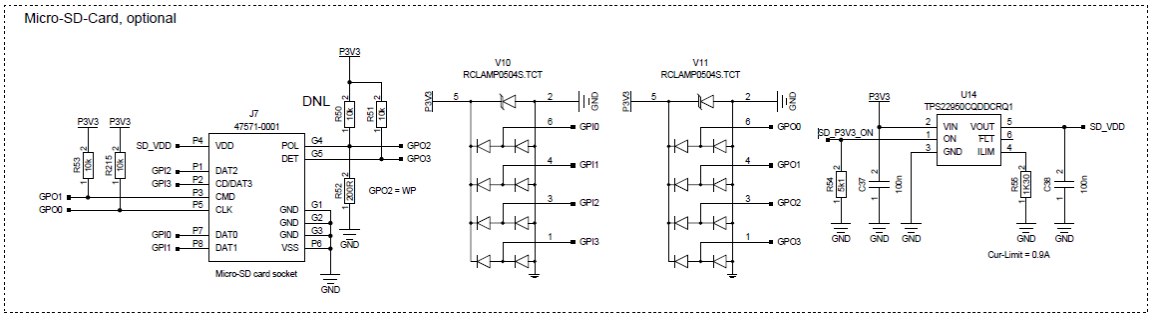
8. U37 + R207…210 + V83 removed



9. C158 … C165 (100n 0603) replaced by 100nF 0402

10. C171, C172 replaced by R310…R311 (0R 0402) **??? change to 100n 0402 ???**

11. Micro-SD card control removed



12. Pullup for GBE0_ACTn added
13. PCIE_SATA0 , SATA1 activity-LEDs moved to fontplate
14. Tricolor LED, controlled by FPGA, arranged at frontplate top end
15. 6 fans (FCON, FSEB, backplane conn.) with sense signals to FPGA now
16. WR-LEN fan connector added
17. WR_P2V6 related circuitry (U42+) removed
18. 10MHZ and IRIGB generation / termination / routing improved
19. Monitoring ADC U6, RTC_VBAT_P3V resistor divider load active at the SPI CSn low phase only
20. External BIOS flash type changed, to be conform with Kontron recommendations
21. Power test conn. J2 with 6 pins now, includes P1V0 (FPGA core voltage)

CPLD signals, removed

signal	meaning	remark
SMB_ALERT		
SMB_DAT		
SMB_CK		
CLKREQn		

Mechanics

1. Frontplate SFP instead of SEP
2. Frontplate with .m2 SSD activity LEDS and universal (programmable) tricolor LED now