Digital Trigger, Status and Next Steps

April 2016

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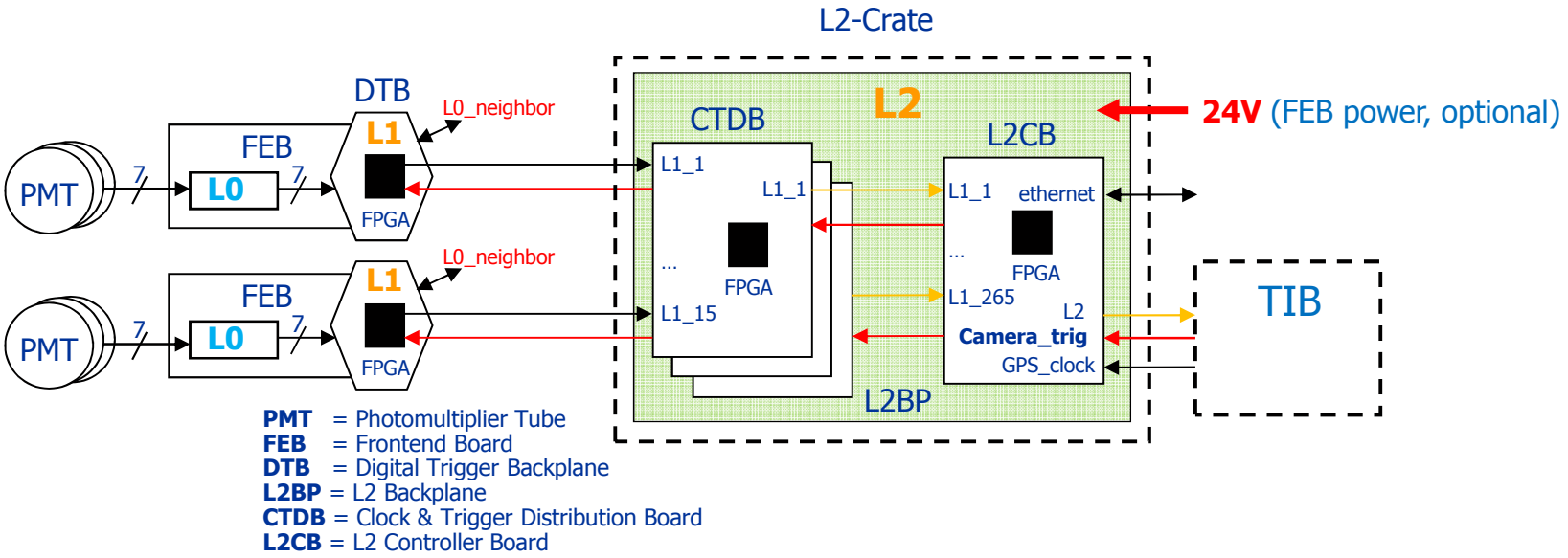
DESY

Topics

- L2 hardware, highlights
- Saclay DT integration, test results
- trigger FPGA configuration / reloading
- next steps

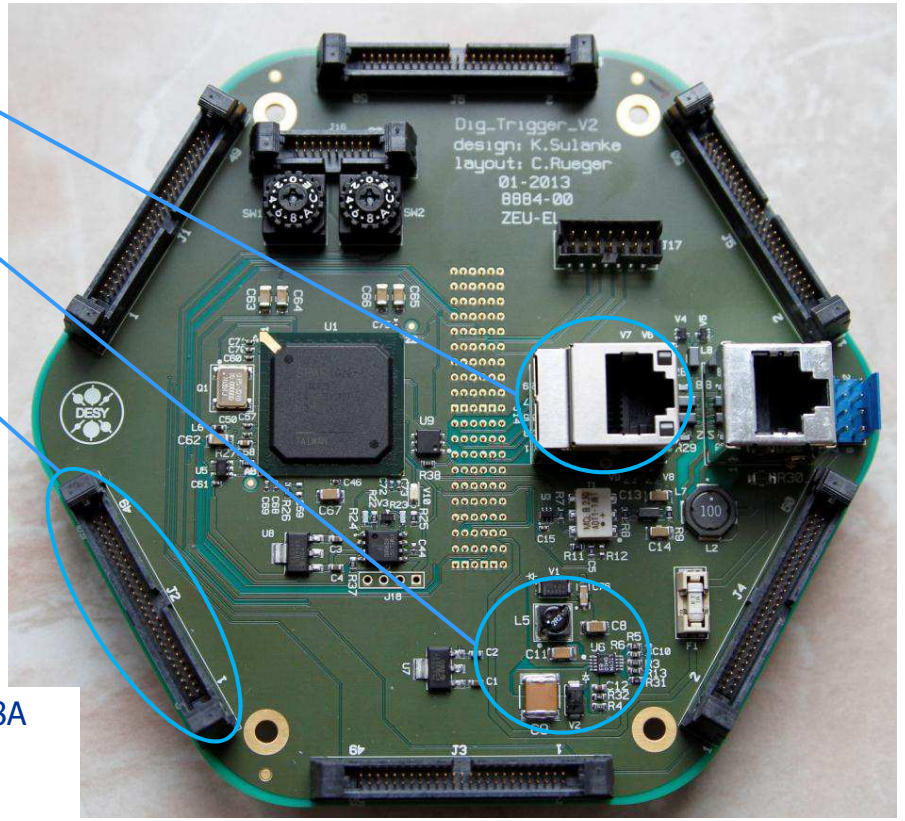
The Centralized Trigger Schema

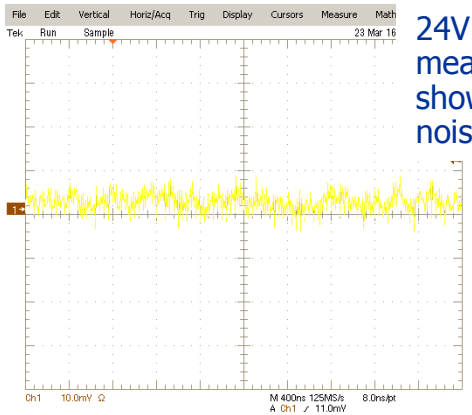


- L0 by AT-L0-Asic discriminator outputs now, (digital L0 mezzanine replaced)
- L1 by 265 DTBs
- L2 by L2-Crate including
  - Backplane (L2BP)
  - 18 Clock & Trigger Distribution Boards (CTDB)
  - 1 L2 Controller Board (L2CB)

DTB2 -> DTB2a

- obsolete gigabit ethernet conn. replaced by ERNI 203342
- DC/DC, additional filter added
  - avoiding ripple on the 24V
- pin compatible, cheaper conns. used, Samtec => Harwin
  - 53 € cost reduction for mass production
- 20 boards assembles by the DESY workshop

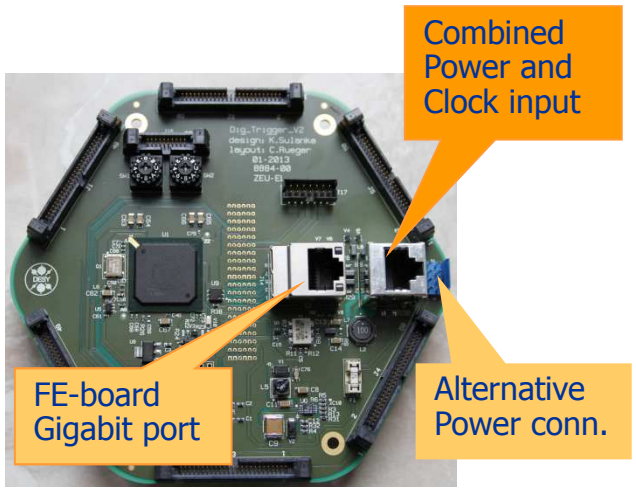




24V ripple @ 0.8A measurement showed probe noise only

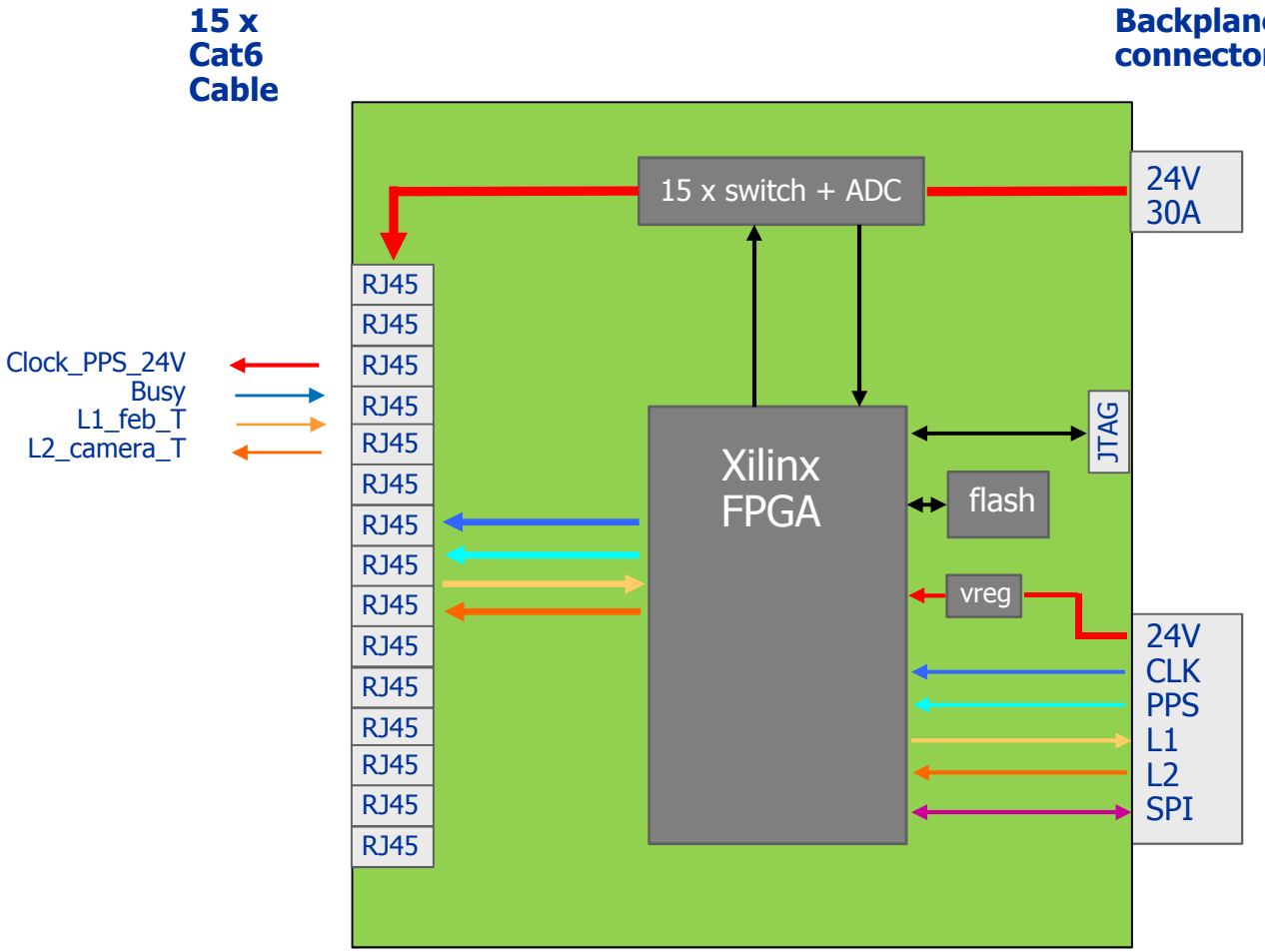
DTB2a, Combined Power and Clock Input

- requires a single Cat.6 cable per cluster only (+ gigabit ethernet cable)
- 24V, clock and PPS over a single wire pair
- overall voltage drop is 0.7V … 1V, depending on the cable being used



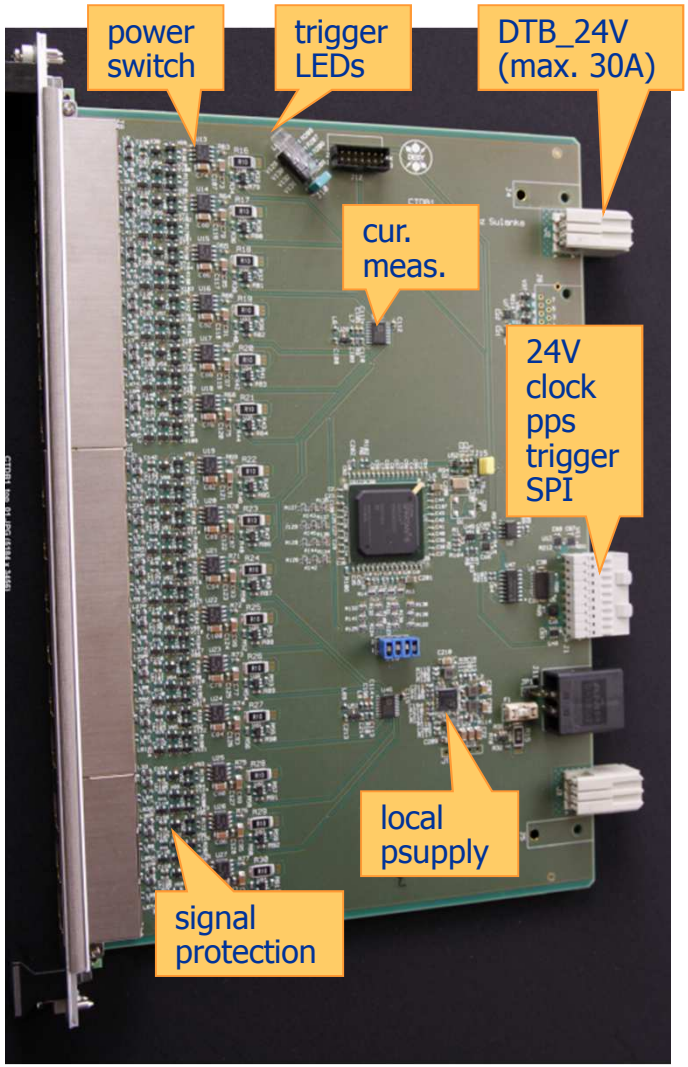
Cat6 - Wire Pair	signal
1	1PPS_CLK_24V
2	BUSY_out
3	Trig_L1_out
4	Trig_L2_in

The Clock & Trigger Distribution Board (CTDB)



CTDB1

- main features
  - DTB signals √
    - P24V_clock_pps distribution
    - L1_trigger reception, passing to L2CB
    - L2_trigger fanout, passing to DTBs
    - FEB_BUSY reception, passing to L2CB
  - DTB + FEB power switches √
    - allows individual FEBs power on / off
  - monitoring of FPGA config. and trigger √
  - current measurement --
  - control via SPI bus interface --



CTDB1, Power Switch (FPF2702)

- on / off by FPGA CMOS signal
- power on ramping
- programmable (R63) max. cur.
- short circuit and overheat protection

Typical Performance Characteristics FPF270X

V_{IN} = 12V and T_A = 25°C.

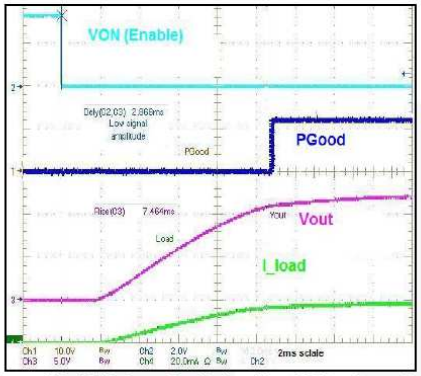


Figure 30. 12V Turn-On Delay (R_L=500Ω, C_{OUT}=2µF)

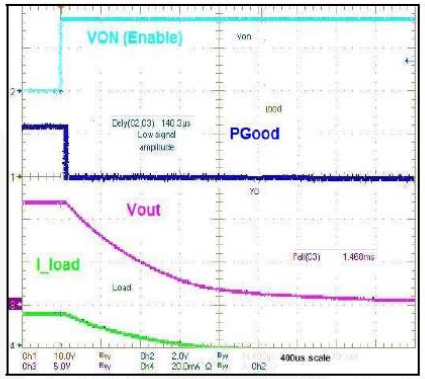
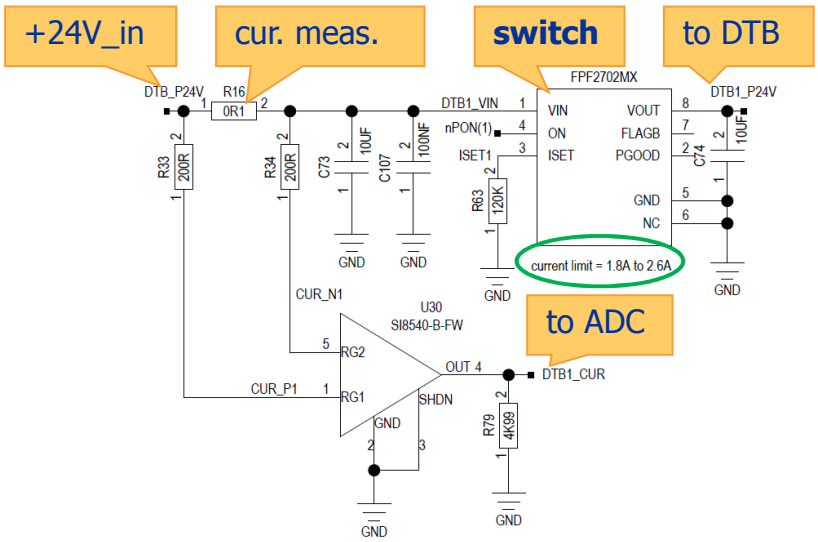


Figure 31. 12V Turn-Off Delay (R_L=500Ω, C_{OUT}=2µF)

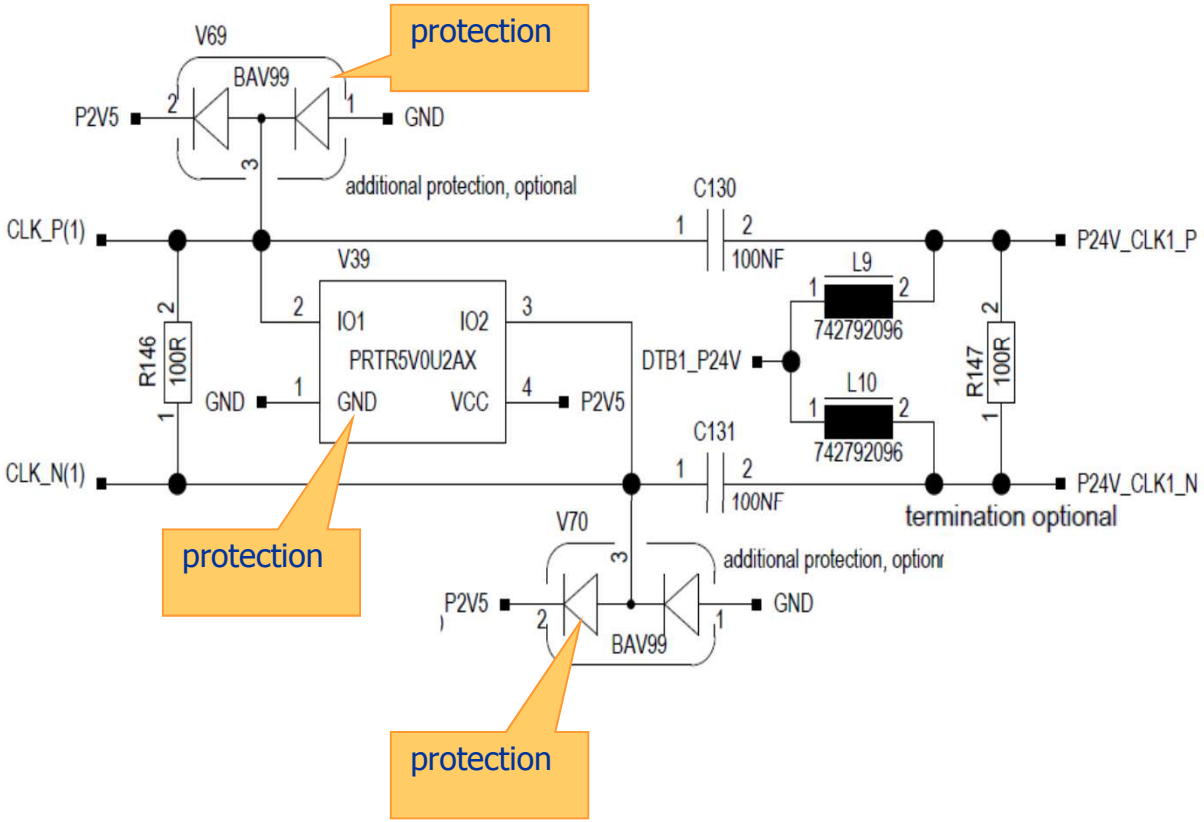


FPF7202 datasheet

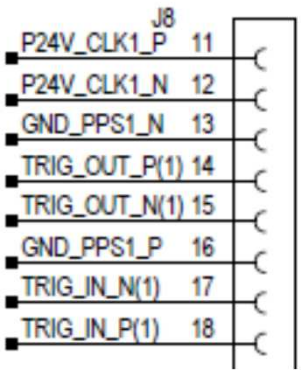
Protections						
I_{LIM}	Current Limit	T_A=25°C	0.8 x I_{NOM}	1.0 x I_{NOM}	1.2 x I_{NOM}	A
I_{SC}	Short Circuit Current Limit	V_{OUT} < 2V, Switch in Over-Current Condition		0.75 x I_{NOM}		A
TSD	Thermal Shutdown	Shutdown Threshold		140		°C
		Return from Shutdown		110		
		Hysteresis		30		
UVLO	Under-Voltage Shutdown	V_{IN} Increasing	2.3	2.5	2.7	V
$UVLO_{HYST}$	Under-Voltage Shutdown Hysteresis			100		mV
Dynamic						
t_{don}	Turn On Delay	R_L=500Ω, C_L=2uF		2.7		ms
t_{doff}	Turn Off Delay			0.1		
t_R	V_{OUT} Rise Time			7.5		
t_F	V_{OUT} Fall Time			1.5		
t_{BLANK}	Over-Current Blanking Time	FPF2700/1, T_A=25°C	0.25	0.50	0.75	ms
$t_{RESTART}$	Auto-Restart Time	FPF2700, T_A=25°C	63.8	127.5	191.2	ms
t_{CLR}	Current-Limit Response Time	V_{IN}=12V, V_{ON}=0V		50		µs

CTDB1, Signal Protection

- all in coming and outgoing signals are protected
- hot swapping of the Cat.6 patch cables is possible

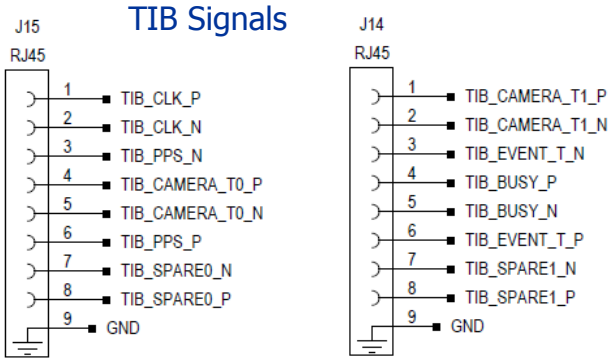


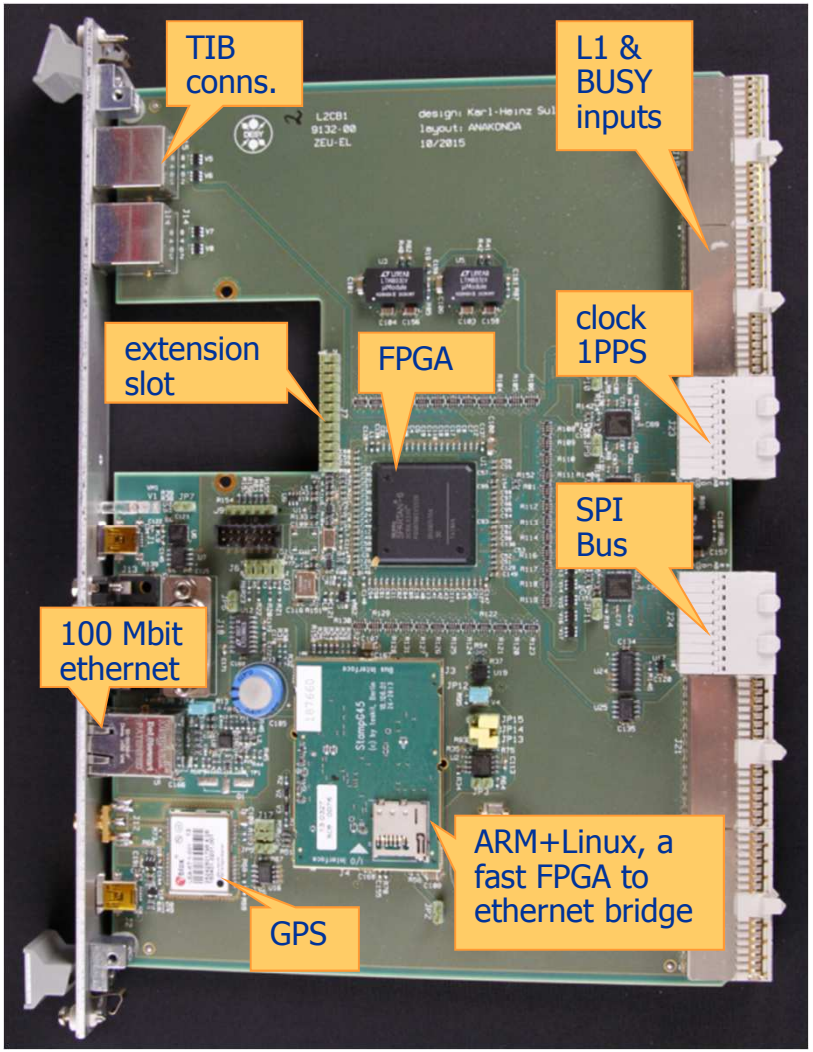
RJ45 conn.



L2CB1, L2 Controller Board

- 270 L1 trigger inputs connected to a single FPGA (676 pins)
- Connection to the TIB
- Clock and PPS distribution on the L2 backplane
- SPI bus control (talking to the CTDBs)
- Linux based onboard microcontroller unit as a fast ethernet to FPGA bridge





L2BP1 (L2 Backplane), Main Features

- PCB design by Carola Rueger, DESY Zeuthen
- **10 layer** PCB, 426 x 262 x 3 mm
- fits (mounting hole positions) into a **standard 6u crate** by Schroff / Pentair
- **18 CTDB** (Clock & Trigger Distribution Board) slots
- **1 central slot** for the L2CB (L2 controller Board)
- all connectors are of the **pressfit** type
- Polysilicon fuses (local power supply) , the only to be soldered
- **length matched** 50 ohm (single ended) and 100 (diff.) signal lines
- all signals lines routed **without (!) using vias**
- **hard wired slot encoding**, 1 to 21 (SPI address)
- high speed diff. SPI Bus
- Two isolated power entries, global (FEB) and local (L2 logic) 24V

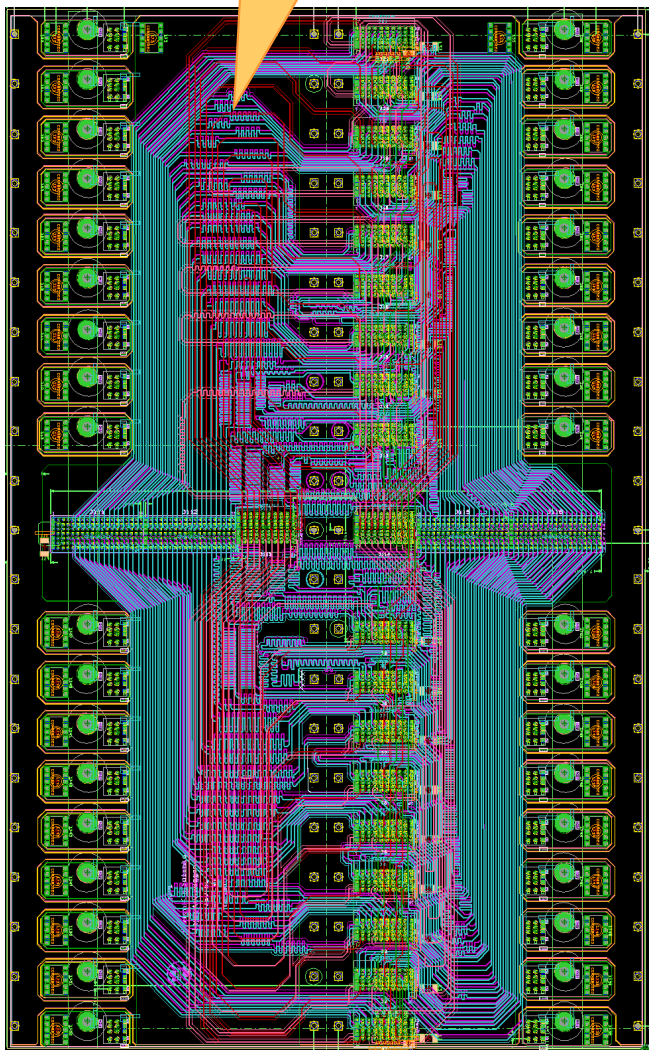
L2BP1, Impedances

Kunde	DESY
Leiterplattentype	L2023304
Teilenummer	L2BP1
Revisionsnummer	G3170a
Datum der Testdatei	Wednesday, December 09, 2015 16:09:17
Druckdatum	Wednesday, December 09, 2015 16:09:48
Stations-ID	_TEST STATION 1_
Testdatei-Pfad	W:\G\G3170a\Impedanz\L2023304.cif
Datenaufzeichnungspfad	W:\G\G3170a\Impedanz\L2023304.clf

all within the 10 % limit

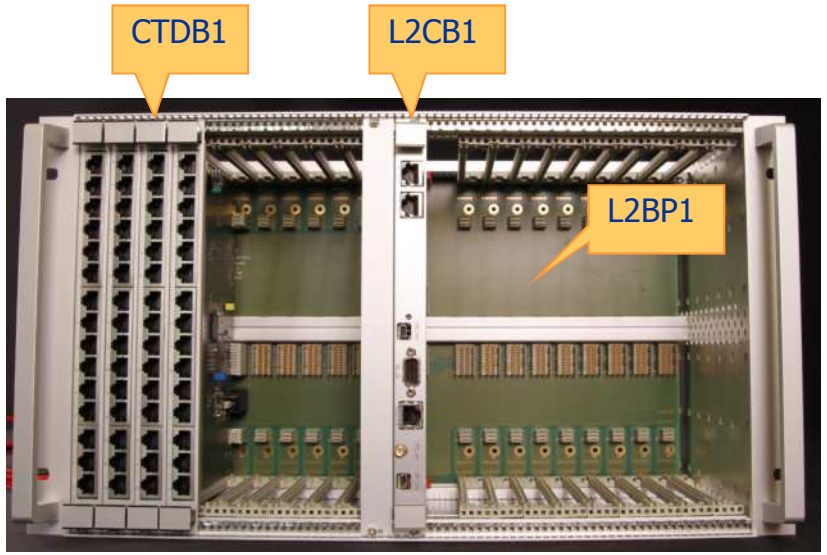
Beschreibung	Lage	Mittelwert
Diff. 100R P1A	L3	93.30
Diff. 100R P2A	L4	93.19
Single P7A	L7	46.39
Single P8A	L8	46.02
Diff. 100R P1B	L1	104.95
Diff. 100R P4B	L10	102.73
Single P5B	L1	47.81
Single P6B	L10	46.78
Diff. 100R P1A	L3	94.91
Diff. 100R P2A	L4	94.54
Single P7A	L7	47.34
Single P8A	L8	46.40
Diff. 100R P1B	L1	101.91
Diff. 100R P4B	L10	102.78
Single P5B	L1	47.55
Single P6B	L10	48.61
Diff. 100R P1A	L3	94.64
Diff. 100R P2A	L4	94.20
Single P7A	L7	46.67
Single P8A	L8	46.62
Diff. 100R P1B	L1	101.69
Diff. 100R P4B	L10	101.68
Single P5B	L1	46.61
Single P6B	L10	46.58
Diff. 100R P1A	L3	93.77
Diff. 100R P2A	L4	94.16
Single P7A	L7	46.91
Single P8A	L8	45.99
Diff. 100R P1B	L1	106.34
Diff. 100R P4B	L10	104.46
Single P5B	L1	46.91
Single P6B	L10	46.63
Diff. 100R P1A	L3	93.60
Diff. 100R P2A	L4	94.51
Single P7A	L7	46.99
Single P8A	L8	46.03
Diff. 100R P1B	L1	103.06
Diff. 100R P4B	L10	100.91
Single P5B	L1	47.65
Single P6B	L10	47.60

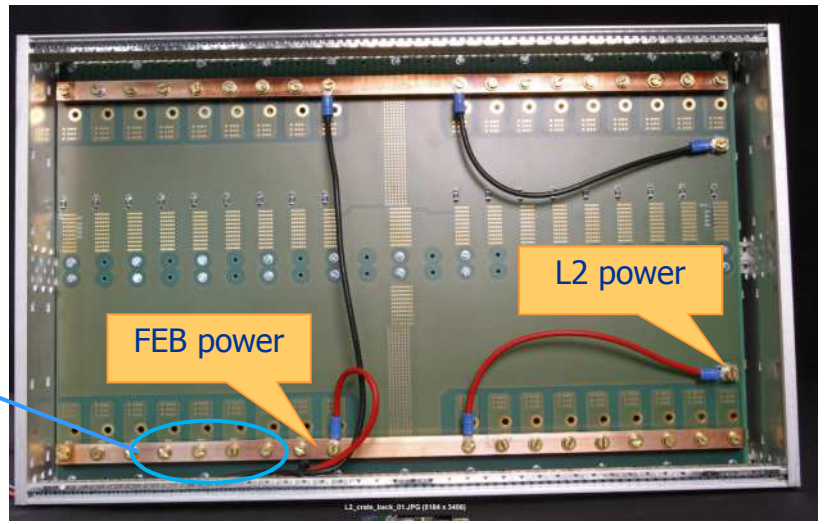
length matched signal traces



L2-Crate

- CDTB1 boards slide in easily
  - guide pins not needed
- L2CB1 needs some force (pin count = 560)
- backplane power & signal connectivity checked
  - except SPI bus
- seperate power supply for the L2 would be better (here, both are connected)
  - Should come up before the main psupply
- power rails for direct connection of 8 parallel psupplies PULS-QT40.24x
  - or via connector

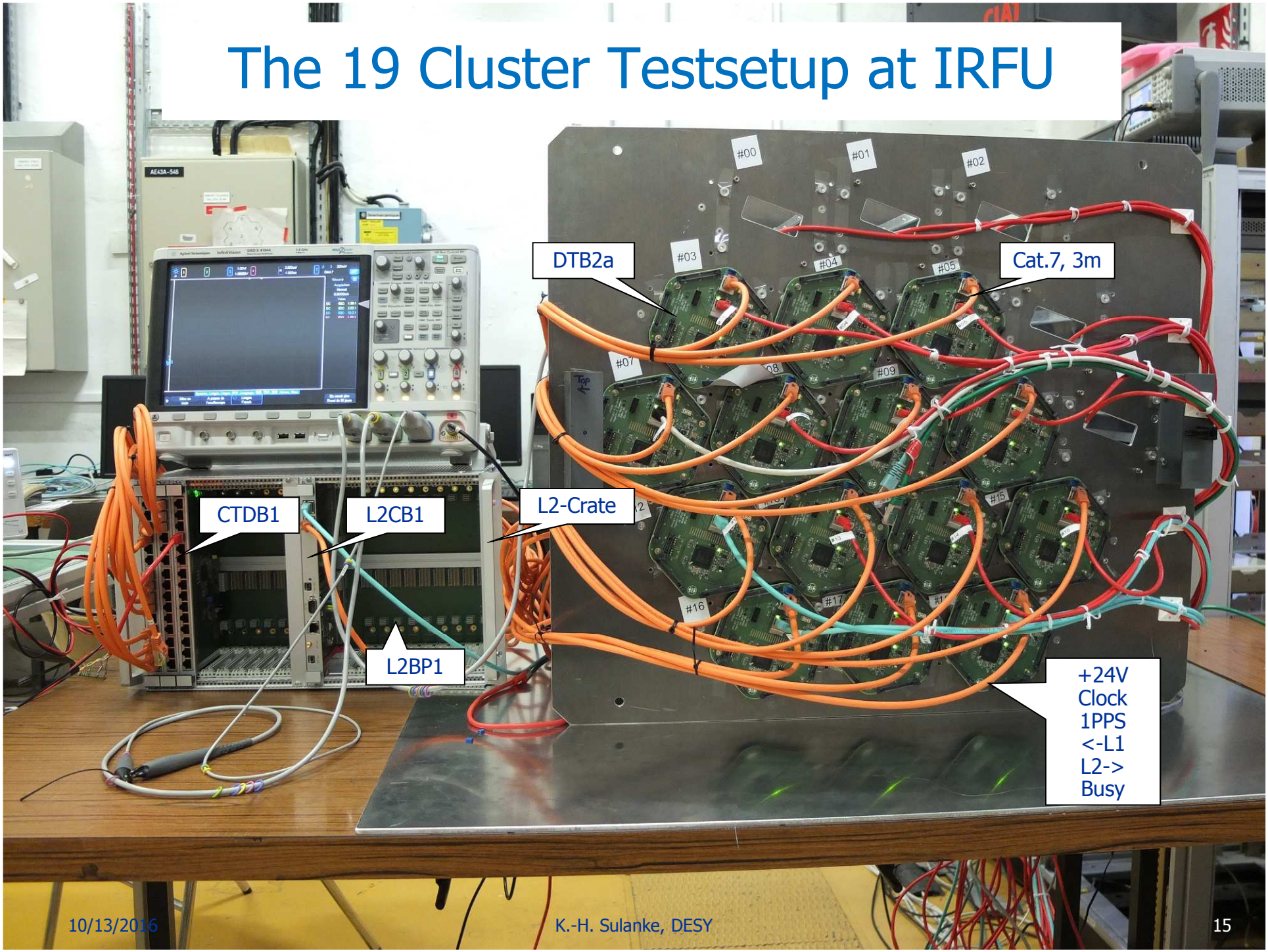




DT Hardware, delivered to IRFU

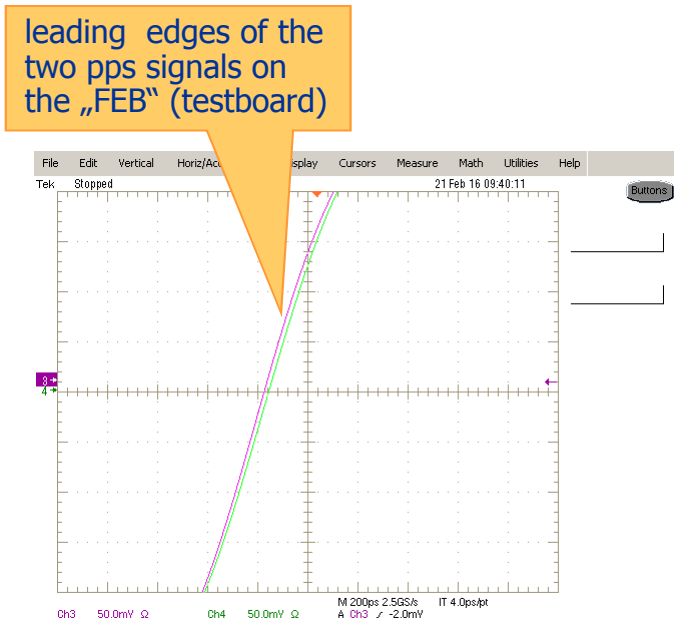
item	amount	remark
DTB2a	20	1 spare
CTDB1	3	1 spare
L2CB1	2	1 spare
L2-Crate	1	
L2BP1	1	
flat cable, 120 mm, 50 way	45	DTB2a interconnect
Cat.7 patch cable, 3m	22	L2-crate to DTB2a
L2-crate power cabling	2	

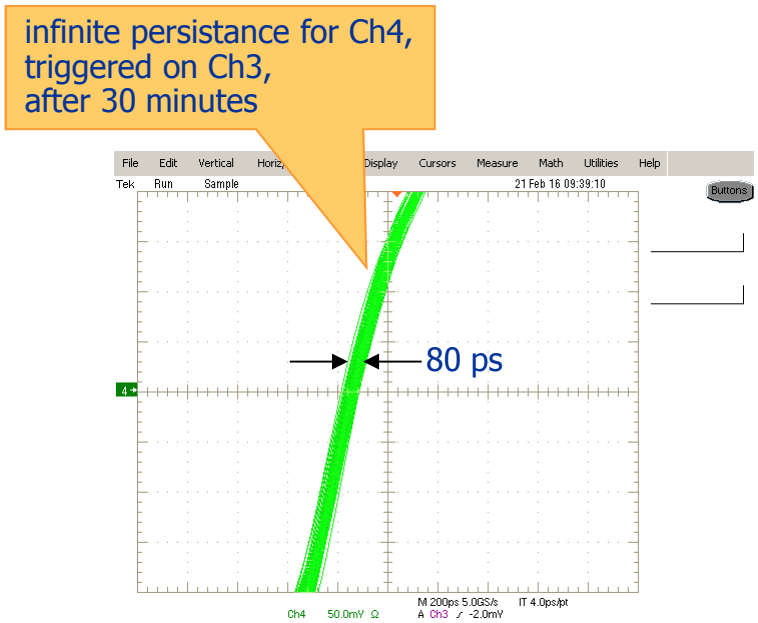
The 19 Cluster Testsetup at IRFU



Skew and Jitter Measurements

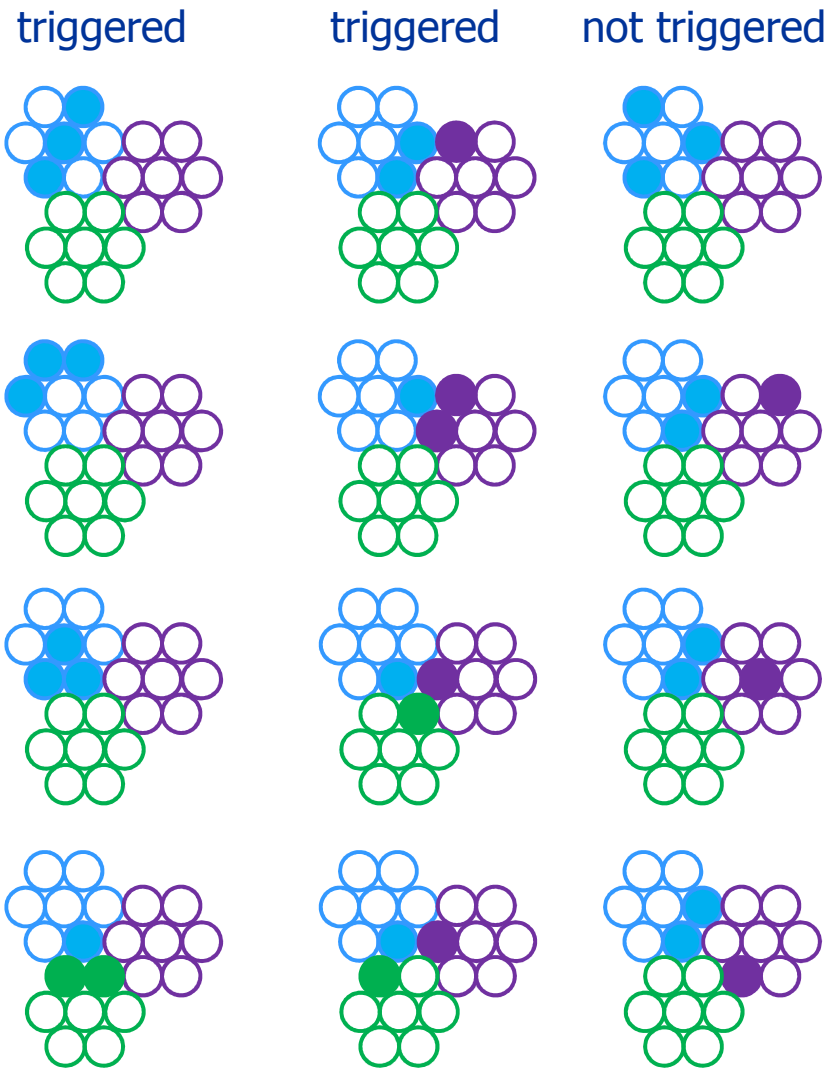
- 1PPS FEB to FEB skew without tuning is in the range of +/- 400 ps (worst case)
- the same for the L2 (camera trigger) fanout
- presently delay adjusted within the DTBs firmware, in 36 ps steps, resulting in
  - 1PPS => -80 ps …+160 ps, L2 => -120 ps …+200 ps
- later delay will get tuned even better by software, using the SPI bus between FEB and DTB
- very little 1PPS jitter (measured at the Zeuthen test setup)





3nn, Trigger Pattern (e.g.), tested

- used 1, 2 and 3 cluster
- various 3nn pattern have been tried
- no failing trigger observed

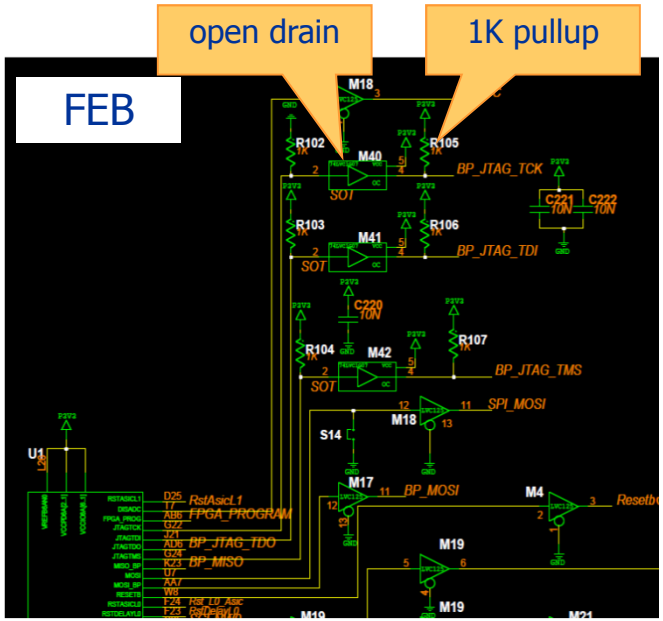


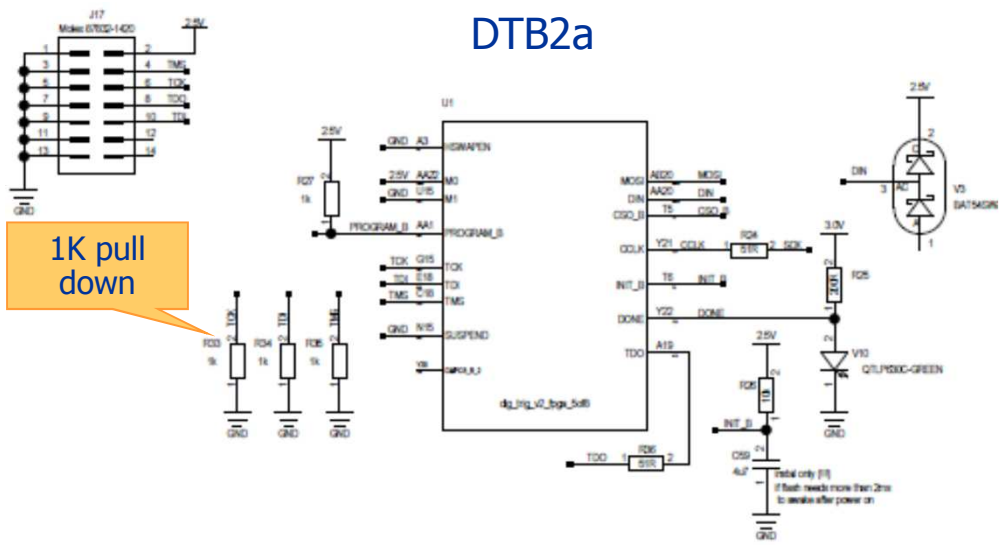
Overall trigger delay

- „TIB" delay is zero here (back looped cable at L2CB1 to TIB connection)
- trigger delay is 210 ns

JTAG Issue

- DTB2a FPGA configuration / Flash programming via JTAG
- JTAG is shared with FEB FPGA-I/O pins via open drain driver 74LVC1G07
- quiet level of these I/O pins (firmware 5.2 (?)) seems to be low
  => blocks the JTAG usage, signals are pulled down
- for DTB2a reflashing the FEB needs to get unpowered and unplugged ☹
- very little FEB firmware change needed only, like „JTAG_TCK <= '1';"



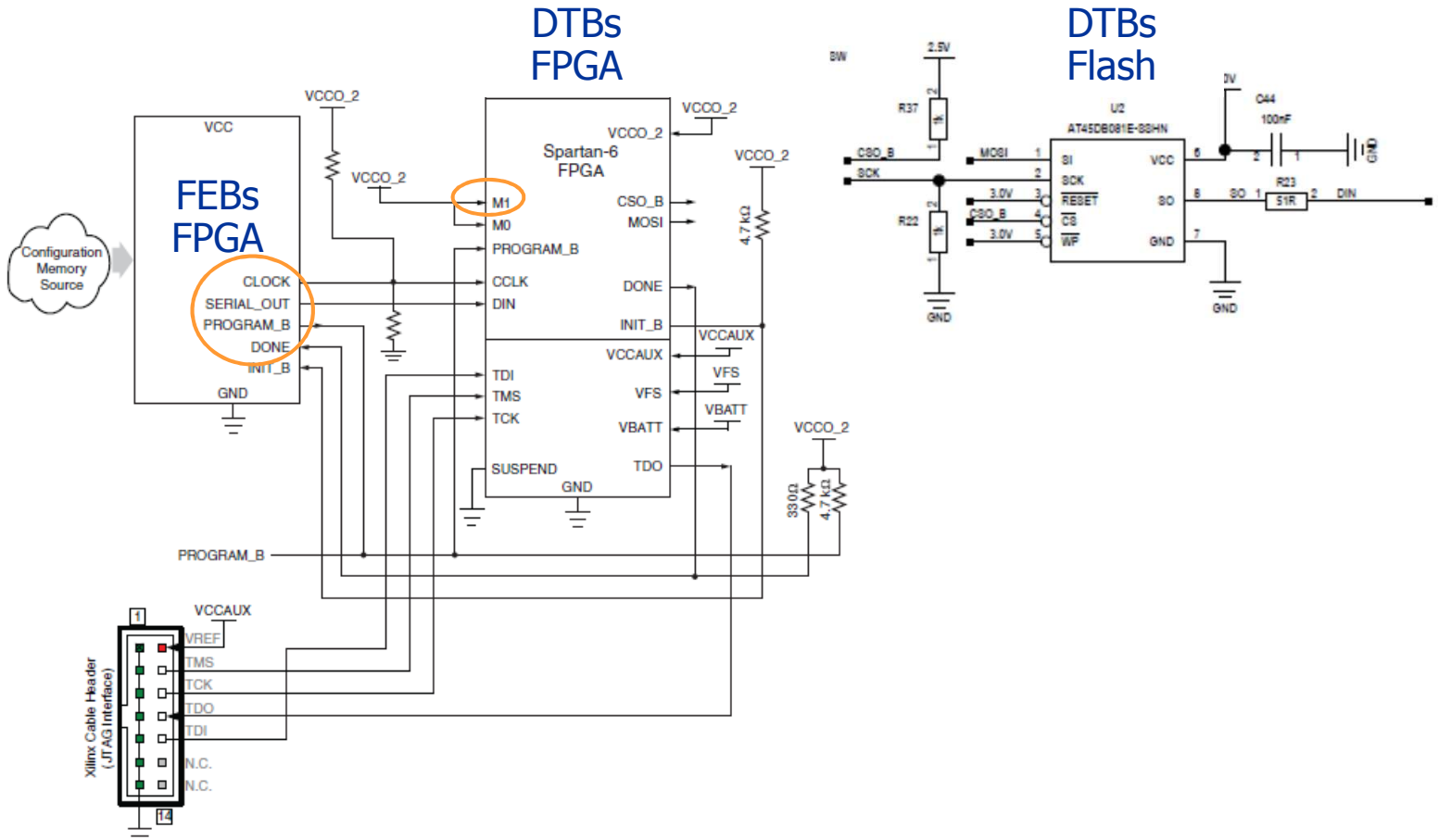


JTAG Issue, possible solution

- when staying with JTAG, better used tristate drivers or a multiplexer or a direct connection to the FPGA (using internal tristate drivers)
- easier to use, is the „slave serial configuration" scheme for the DTB (or ATB)
  - FEB is the master
  - software just has to load the Trigger-FPGA image (binary file) to be serialized and shifted by the FEBs FPGA
  - recommended way, fast and simple
  - essential for remote trigger firmware update

JTAG Issue, possible solution, cont.

- slave serial configuration, 4 signals needed
- switching M1 would allow the DTB to load from a Flash first (power on)



Summary

- DT hardware, needed for a 19 cluster test setup, delivered to IRFU (including spares)
- worked „out of the box"
- presently 1PPS and L2 delay fine tuning per firmware only
- L2 Crate will allow individual FEB powering and health monitoring (current measurement)
- JTAG issue needs to get solved
- Trigger-FPGA remote configuration should be discussed

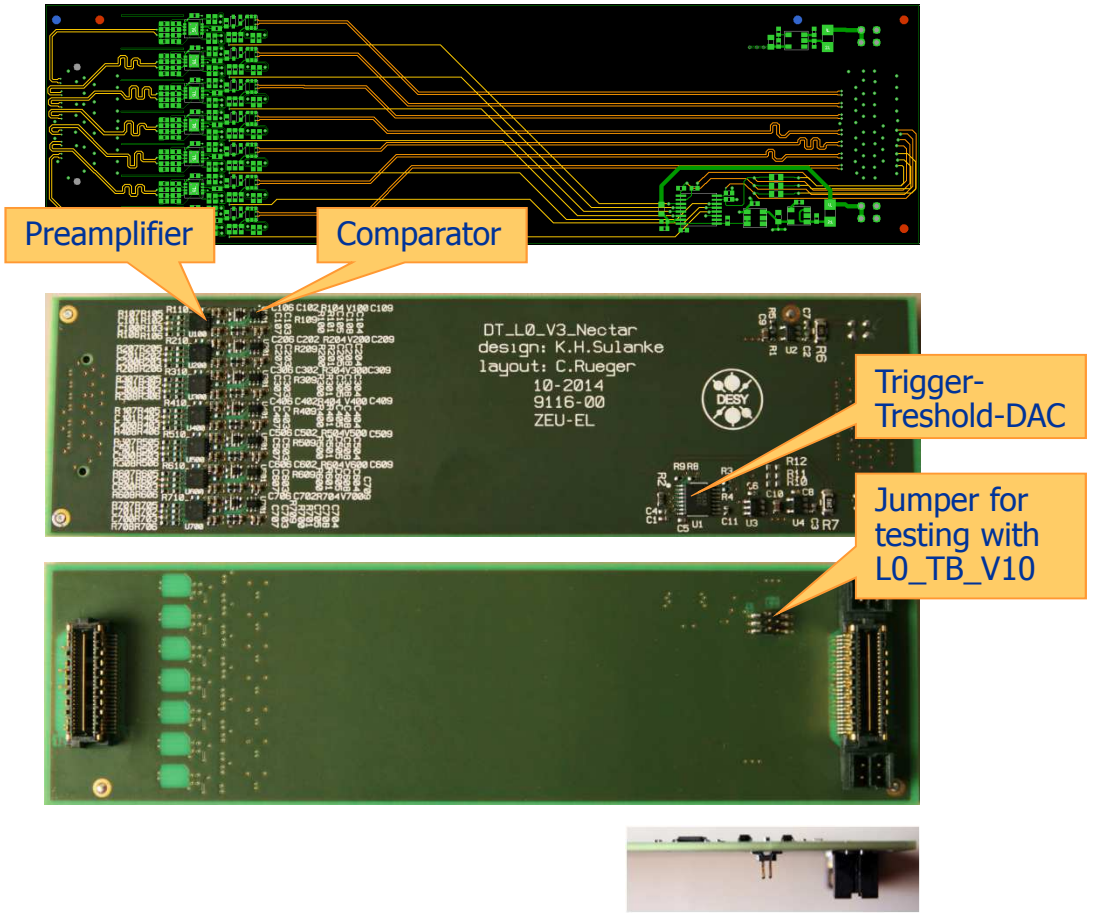
Next Steps, with downgoing priority

- DTB2a, implementing the SPI bus interface to the FEB + software API
  - for delay fine tuning
  - switching the trigger mode
    - e.g. to single pixel (for calibration purposes)
  - other control and status exchange
- L2CB1, implementing the SPI bus control
  - software controlled FEB power on / off
  - FEB current read back
- DTB2a, trying other trigger algorithms
- DTB2a => DTB3 migration
  - new FEB connector angle
  - new remote configuration schema (?)

Backup Slides

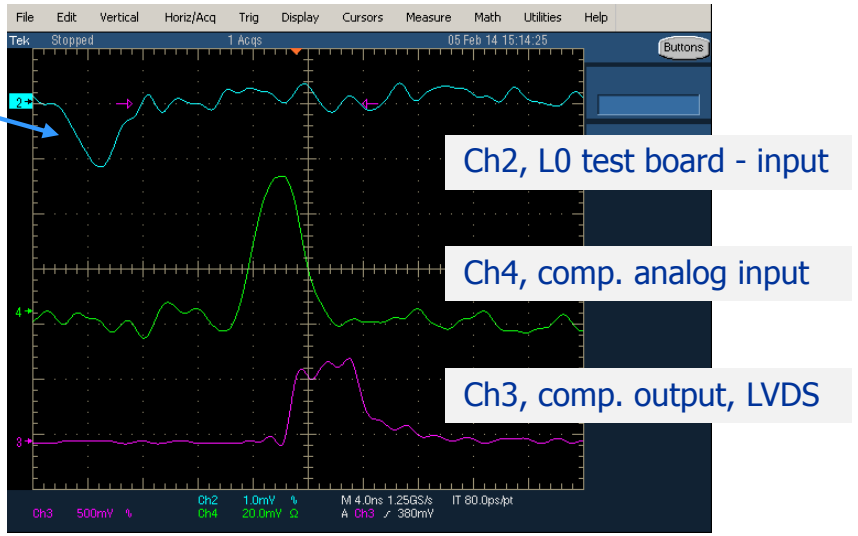
Nectar_L0_V3, Mezzanine Board

- 6 layer PCB with length-tuned signal lines
- tested at DESY, using the L0-Testboard (L0_TB_V10)



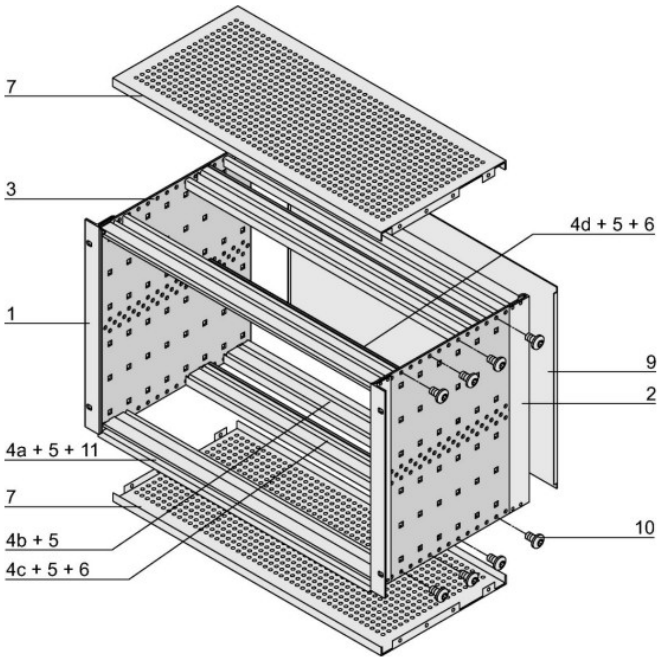
DT-L0 vs. AT-L0_Asic

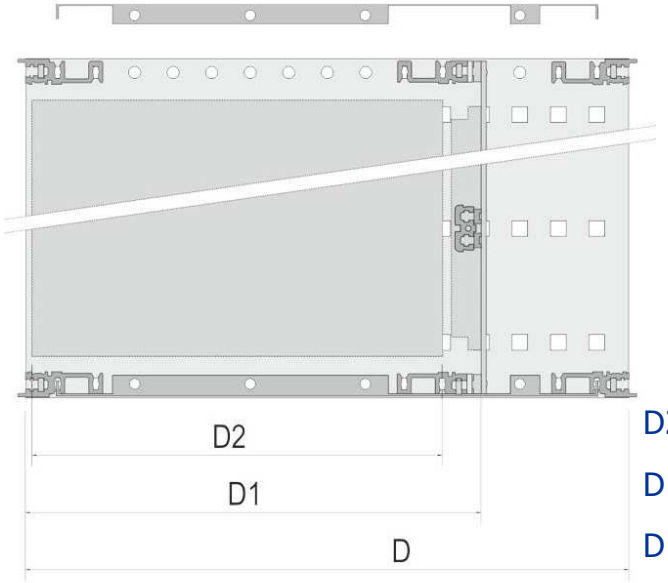
- Performance of the Digital Trigger depends strongly on the quality if its first stage
- … and on the quality of the FE design
- to be compared
  - noise floor (most important)
  - crosstalk
  - channel to channel deviation (comp. offset, delay)
  - temperature dependency
- e.g., discrimination of a -1.2 mV pk, PMT like signal
  - L0-TB gain = 4.4
  - L0-mezz. gain = 6.1



The L2-Crate

- Schroff 24563-442
- 6 U, 84 HP (21 slots)
- Card size : 233 x 160 mm
- Slot usage, see below

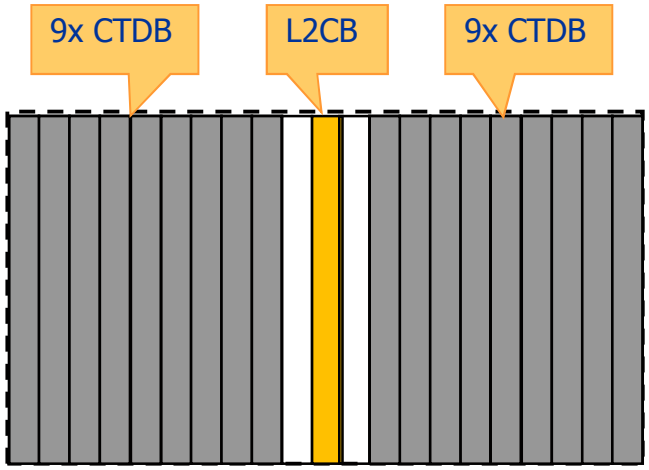




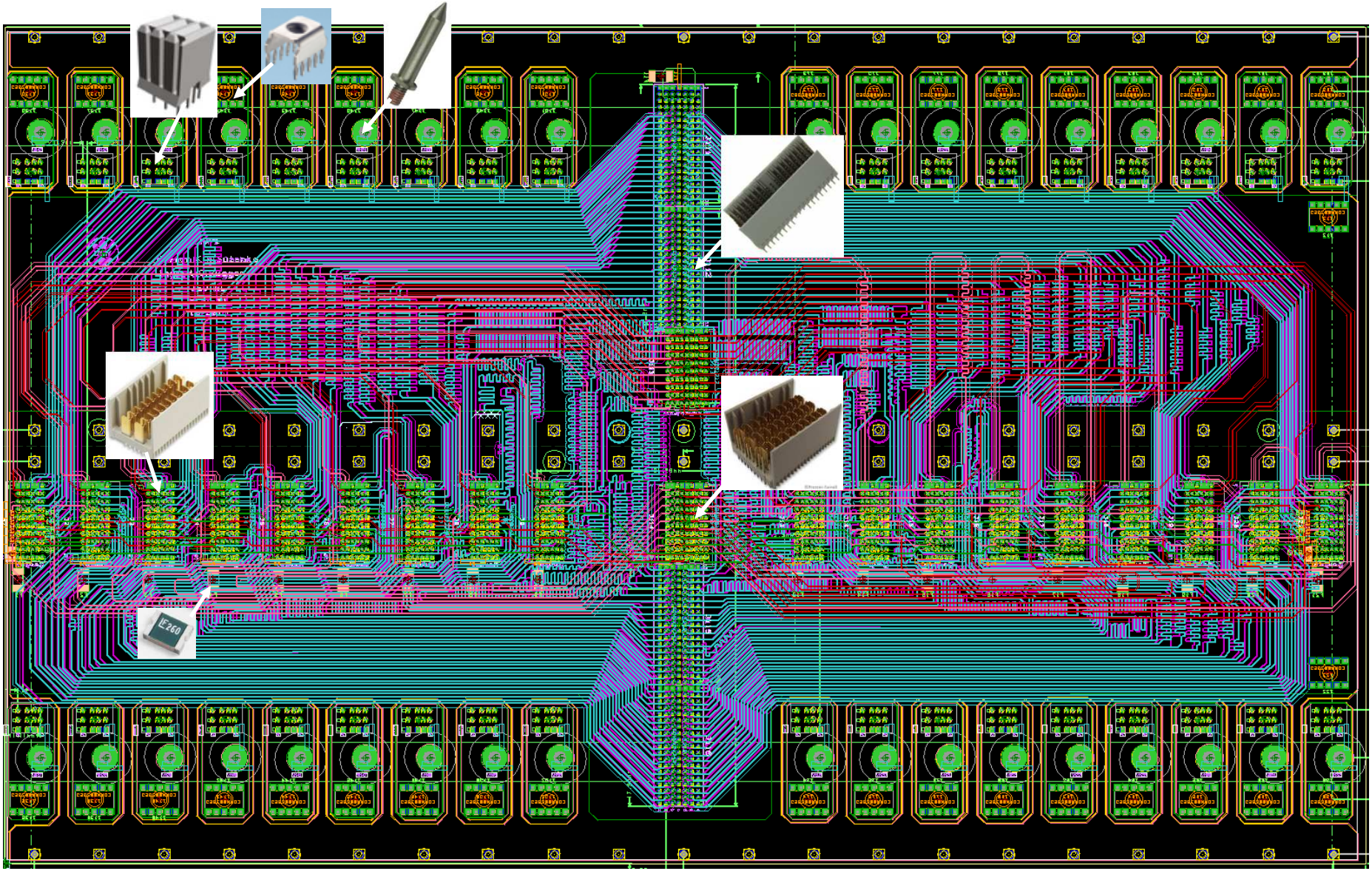
D2 = 160 mm

D1 = 175 mm

D = 235 mm

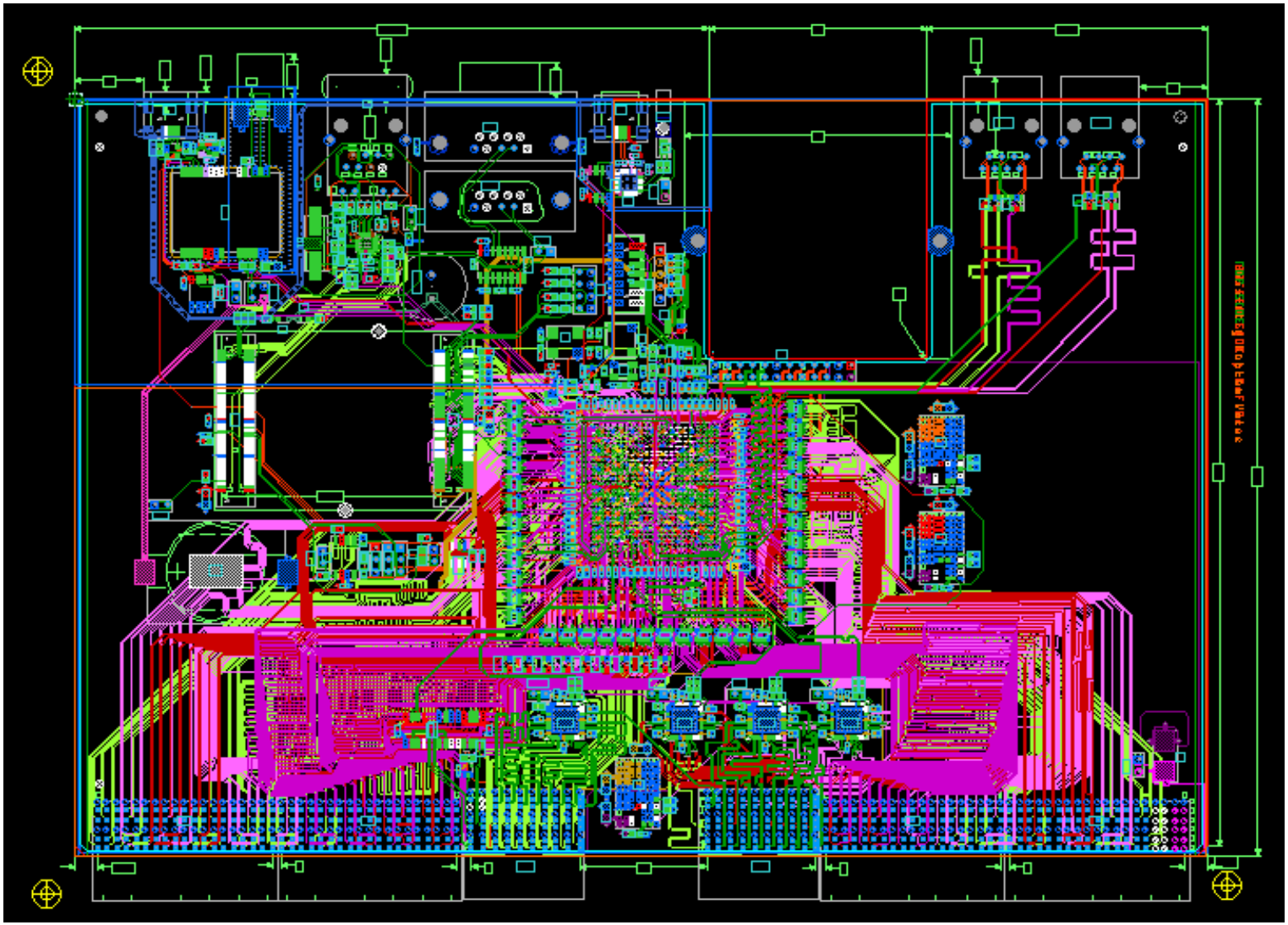


L2BP (L2 Backplane), PCB with used parts



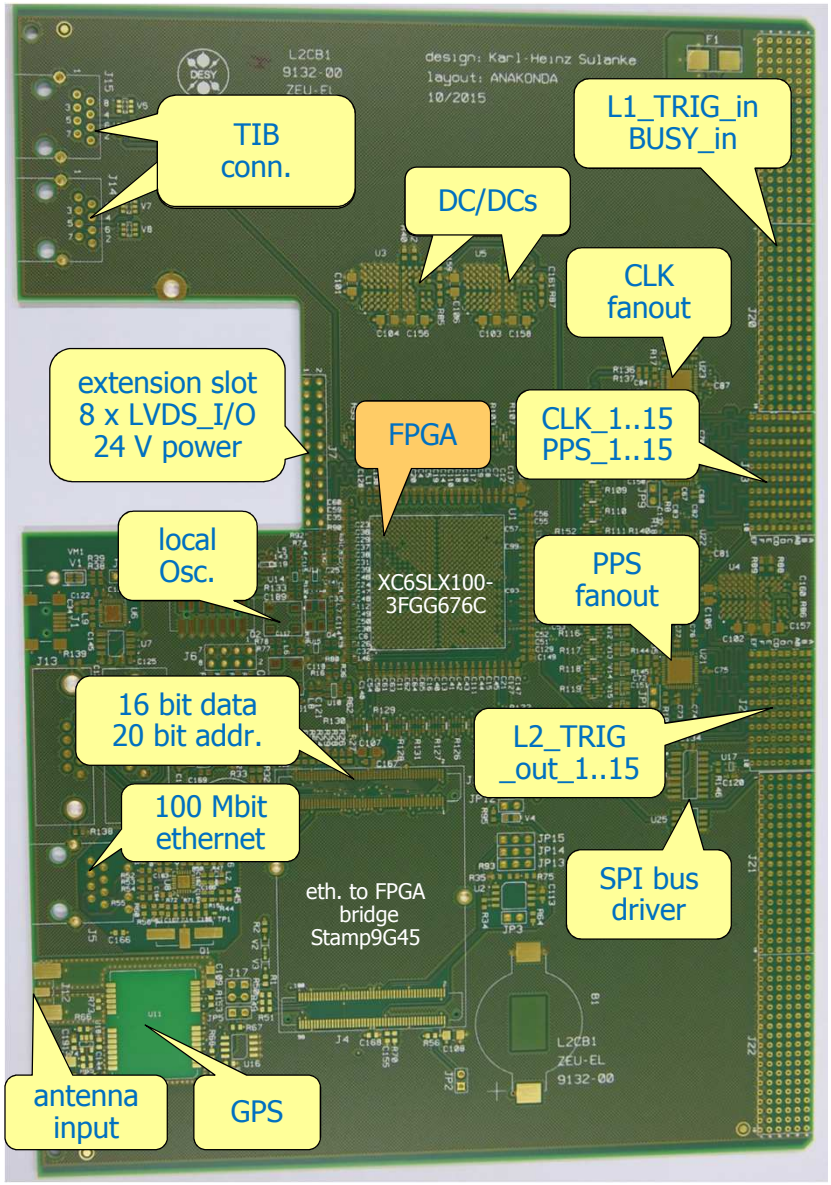
L2CB (L2 Controller Board), PCB

PCB design by Brigitte Kielgas, Anakonda Electronic Design, Berlin



L2CB (L2 Controller Board), Features

- 10 layer PCB, 6u, 233 x 160 x 1.6 mm
- central part is the 676 pin Xilinx FPGA
- handles up to 270 single ended L1 trigger signals (50 ohm terminated)
- Backplane SPI bus control
  - individual FEB power on/off + current monitoring
  - CTDB firmware update
- ARM based MCU, ethernet to FPGA bridge
  - Stamp9G45 by taskit
  - Linux, 512 MB Flash, 256 MB RAM
  - 16 bit memory bus, max. 50 MB/s
    - slow control
    - L2CB firmware update
- optional usage of :
  - extension slot, +24V, 8 x LVDS_I/O
  - precise local oscillator
  - GPS system
  - USB / RS232 interface



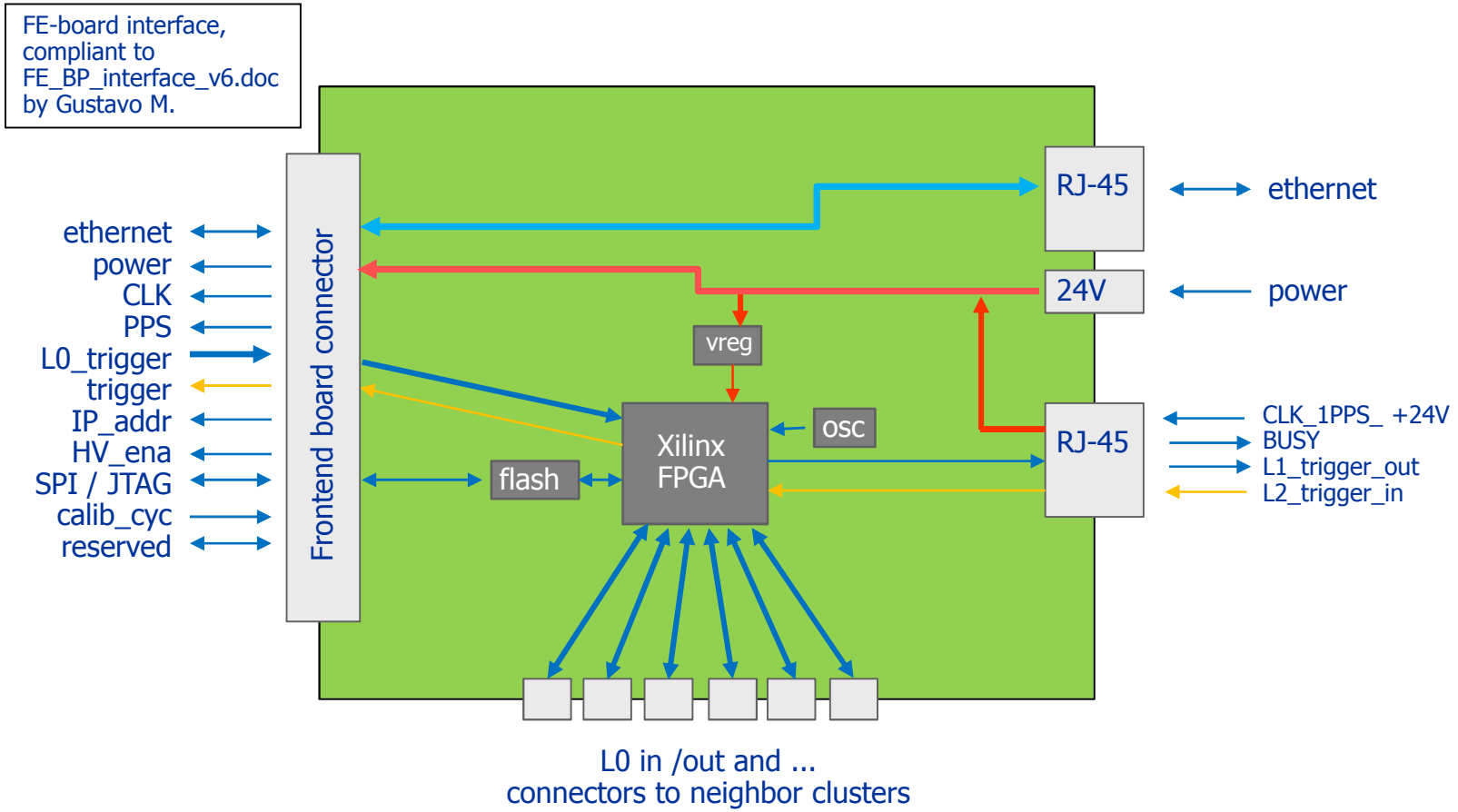
CTDB, Features

- 8 layer PCB, 233 x 160 x 1.6 mm
- central part is the 484 pin Xilinx Spartan 6 FPGA
- reception / fanout of clock, pps, busy, L1, L2 (camera trigger)
- a lot of protection circuitry
- slow control via (backplane) SPI Bus
- FPGA power-on load from write protected Flash, reprogramming via SPI Bus possible
  - only all CTDBs at once (broadcast mode)
- optional :
  - individual FEB power on / off + current monitoring via L2CB
    - max. FEB current limit by resistor and / or firmware, up to 2.5 A
    - accuracy of the current measurement ~ 1 %
    - hardware based overload protection
    - Interrupt bus line, connected to the L2CB
  - for small test setups (CTDB-only mode)
    - local oscillator
    - TIB connection on the backplane side

DT-L0, TOT with 12 mV Threshold

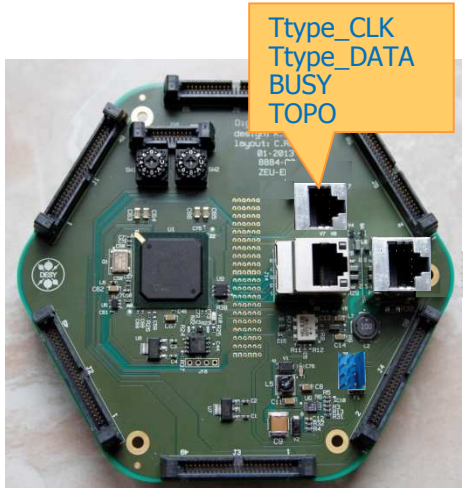
- Measurements done, using the L0 Testboard (TB_gain = 8.3, L0_gain = 6.1)

The Digital Trigger Backplane Rev. 2

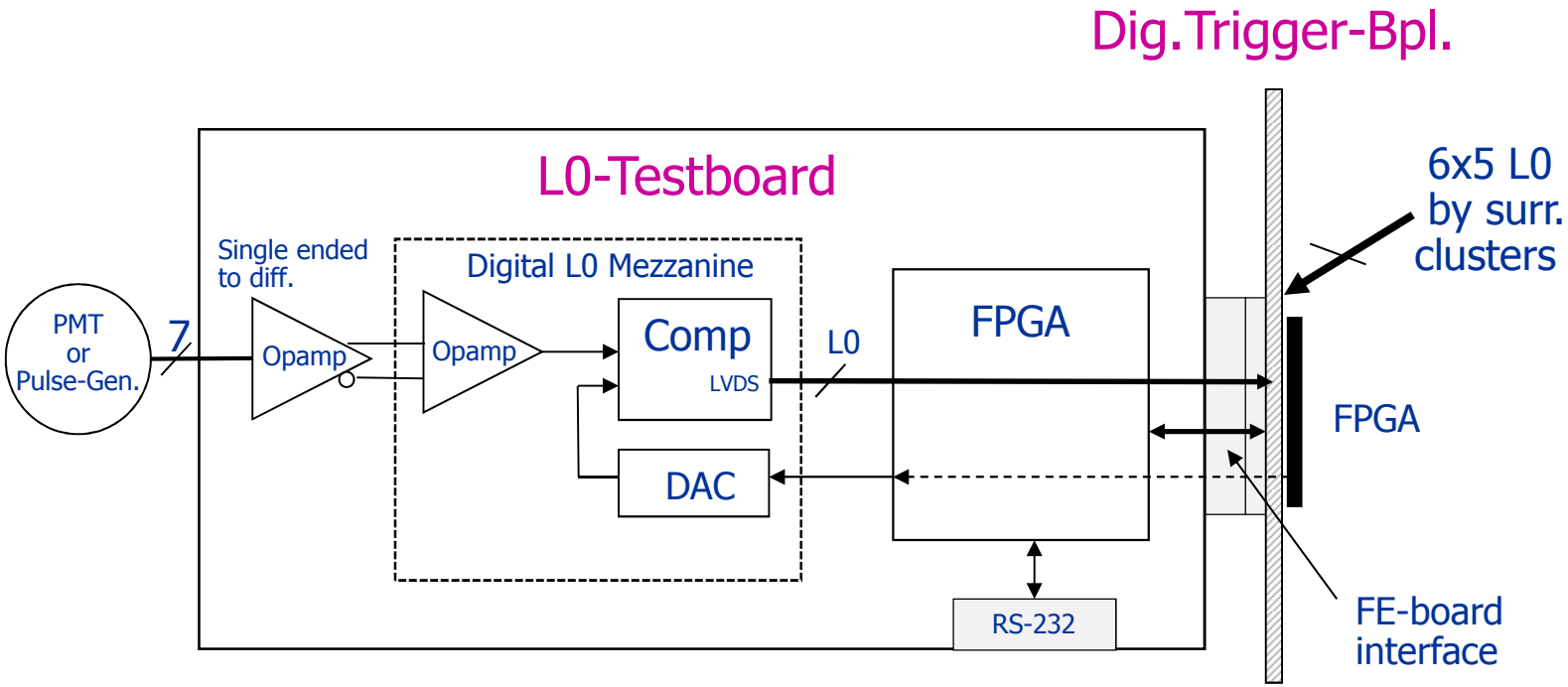


DTB2a -> DTB3

- Rev. 2a performing well
- Rev. 3 design, depending on the acceptance of the digital trigger approach
- if Rev. 3 design takes place, some minor changes only:
  - Mechanical (FEB-conn. angle, mounting holes)
  - additional RJ45 connector
  - Removal of ID switches
    - use 1-wire EEPROM instead, to encode the cluster position
  - new FPGA configuration schema (?)
    - power on load from a write protected flash always
    - FEB - FPGA can reload the FPGA using the passive serial schema
      - compared to the JTAG based schema much easier to implement in software / firmware

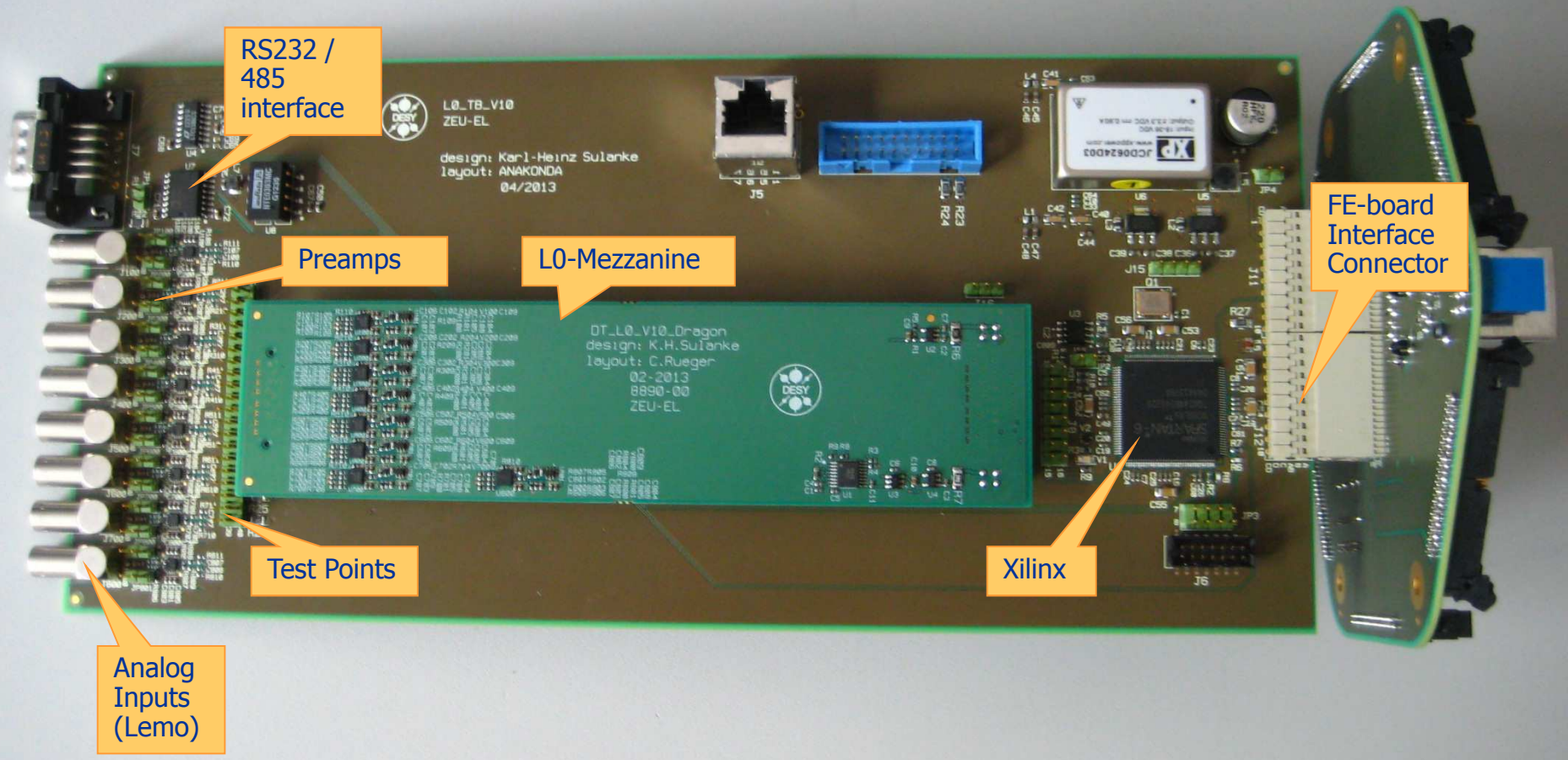


Digital Trigger L0 Test Board

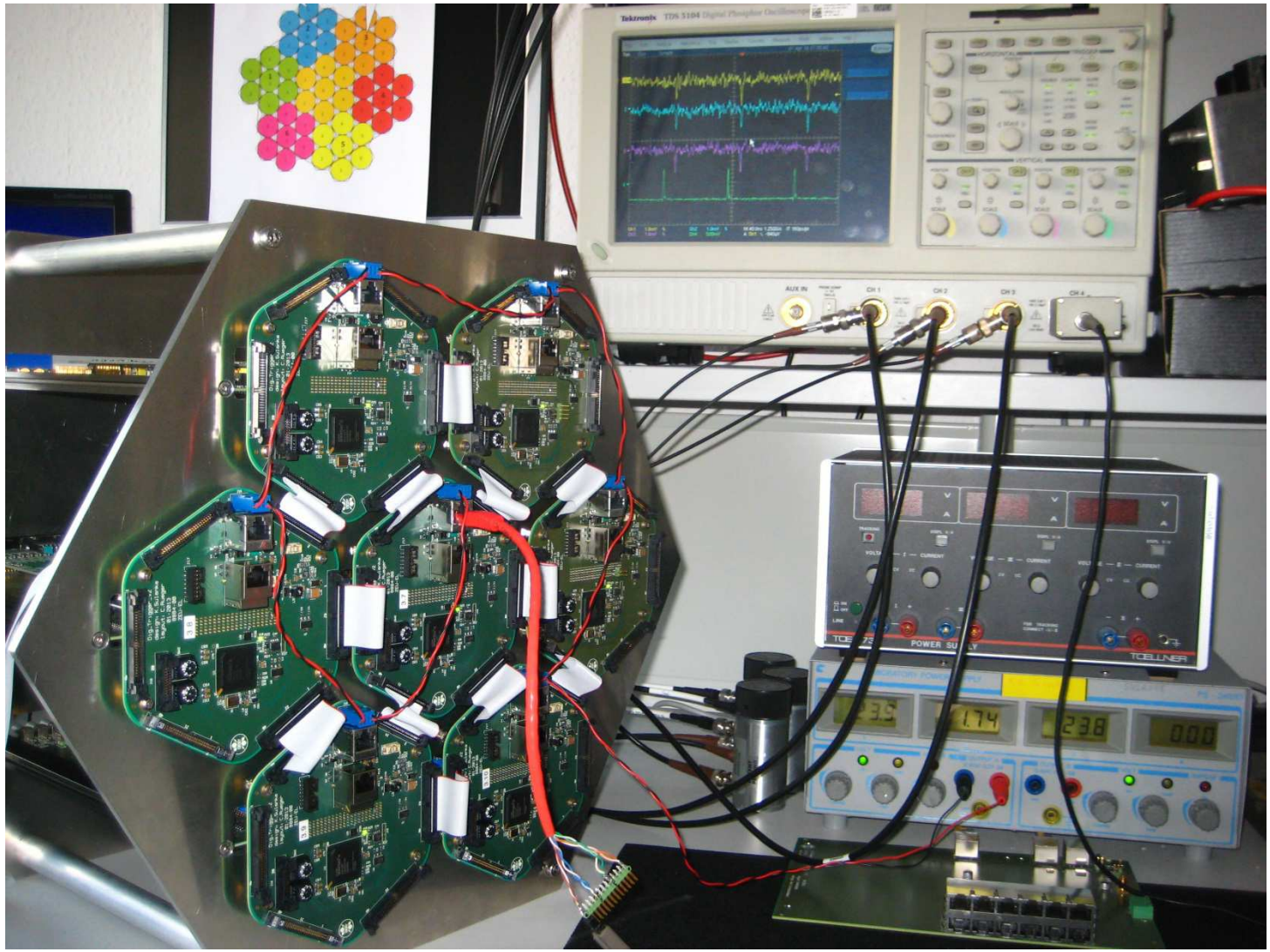


DT-L0 Test Board

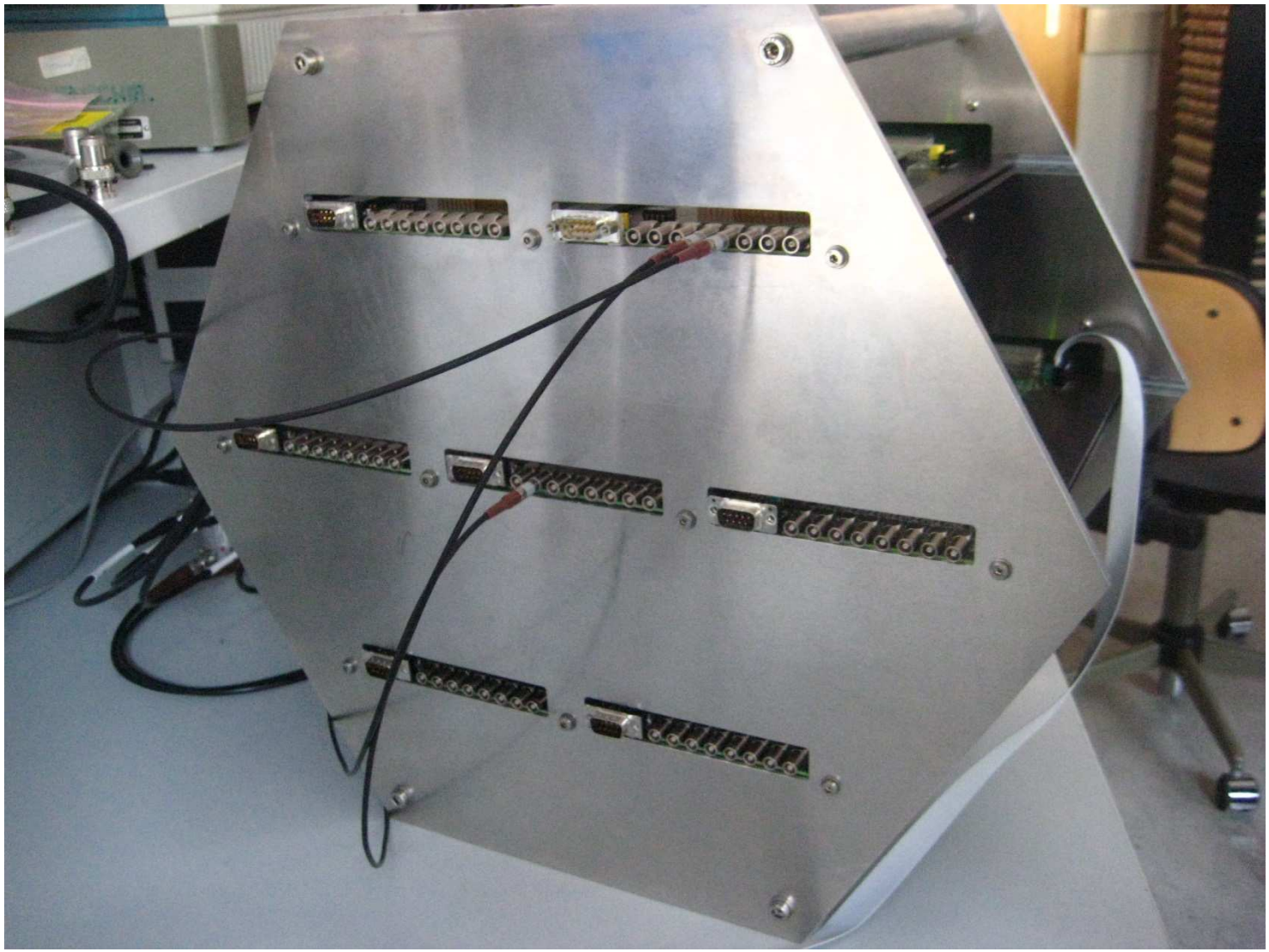
- 120 mm x 260 mm, 6 Layer PCB, various analog and digital test points



Digital Trigger Test Setup at DESY

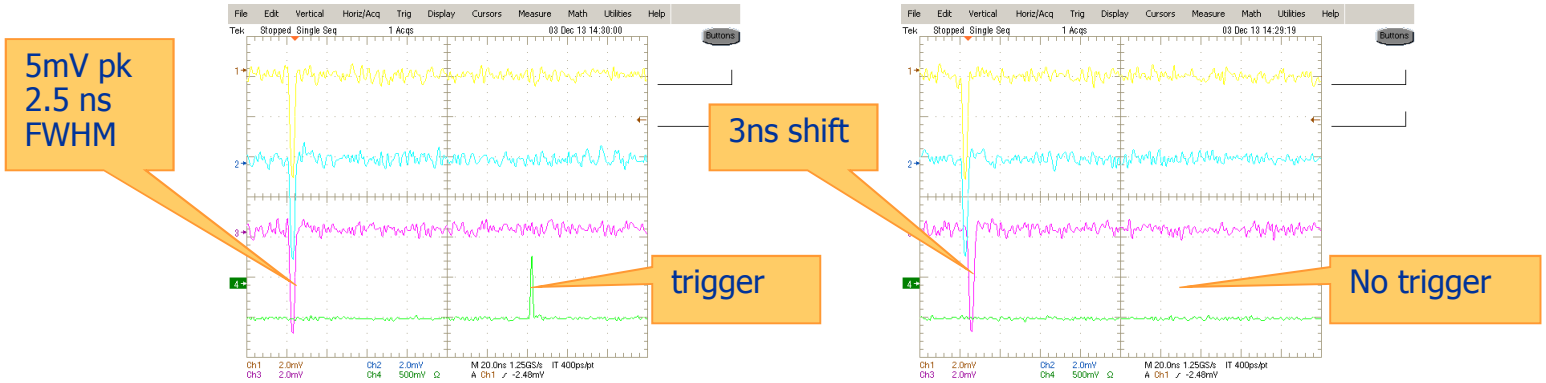


Digital Trigger Test Setup, Back Side

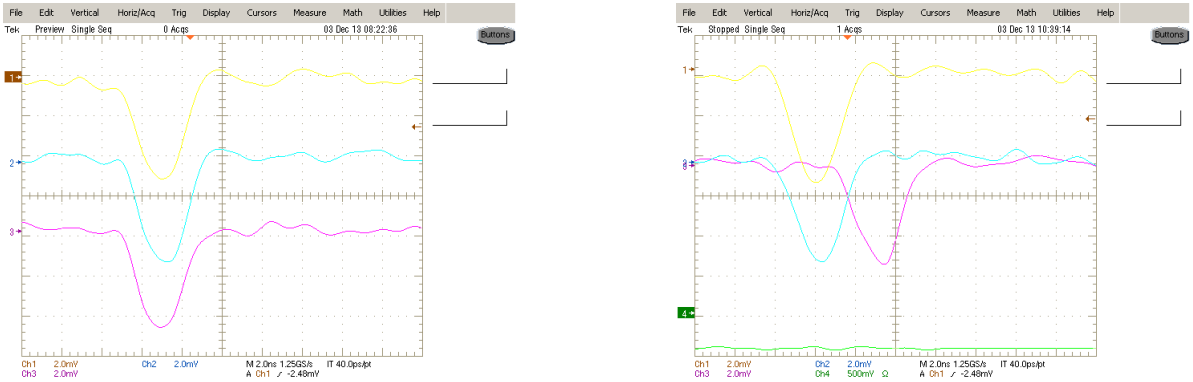


3NN Trigger Test Results

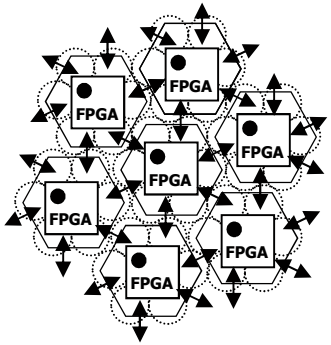
- 100% trigger and 0% trigger situation

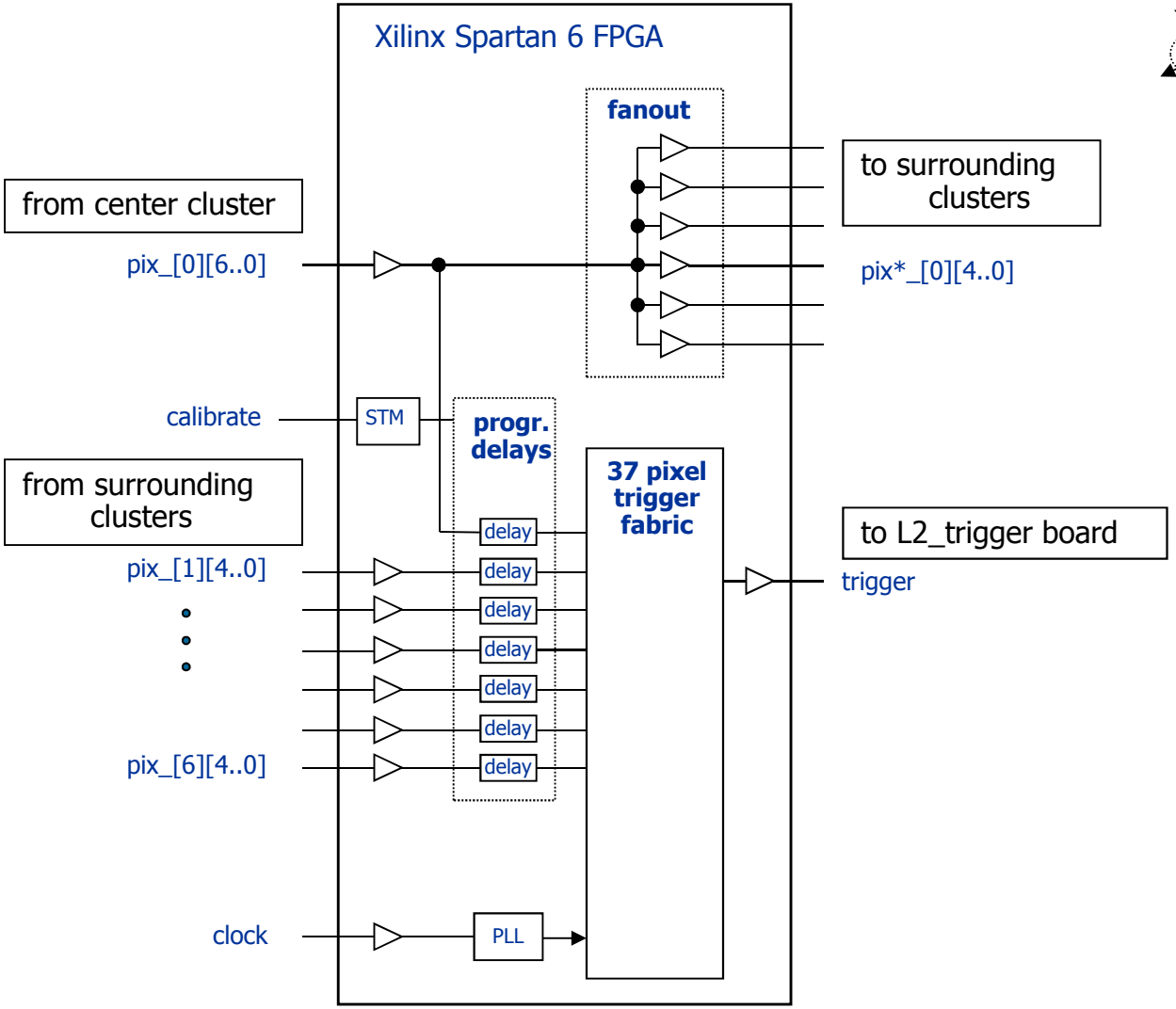


- Analog input signals, zoomed time scale



L1, DTB-FPGA's Functionality





Cabling, Power Consumption and Cooling

- Cat6 Cabling
  - DTBs <-> CTDB (L2-crate), standard round (d=6mm) 265 x shielded CAT6
    - Same Length up to 5 m, but as short as possible preferred. 3 m is o.k. ?
  - L2CB (L2-crate) <-> TIB, standard round (d=6mm) 2 x shielded CAT6, .. 5m
  - L2CB (L2-crate) <-> central cluster, standard round (d=6mm) 1 x shielded CAT6, .. 5m
  - L2CB (L2-crate) <-> ethernet hub, standard round (d=6mm) 1 x shielded CAT6, .. 5m
- 24V Power cabling
  - DTBs, same like for the ATBs, or the CAT6 cable, used for clock, pps, trigger,...
  - L2-crate, 2 x copper, 0.5 … 1 mm2, like used for other peripherals
- Max. L2-crate Power consumption
  - 50 W estimated
  - Cooling, L2-Crate
  - Additional cooling not required
  - Convection must be possible