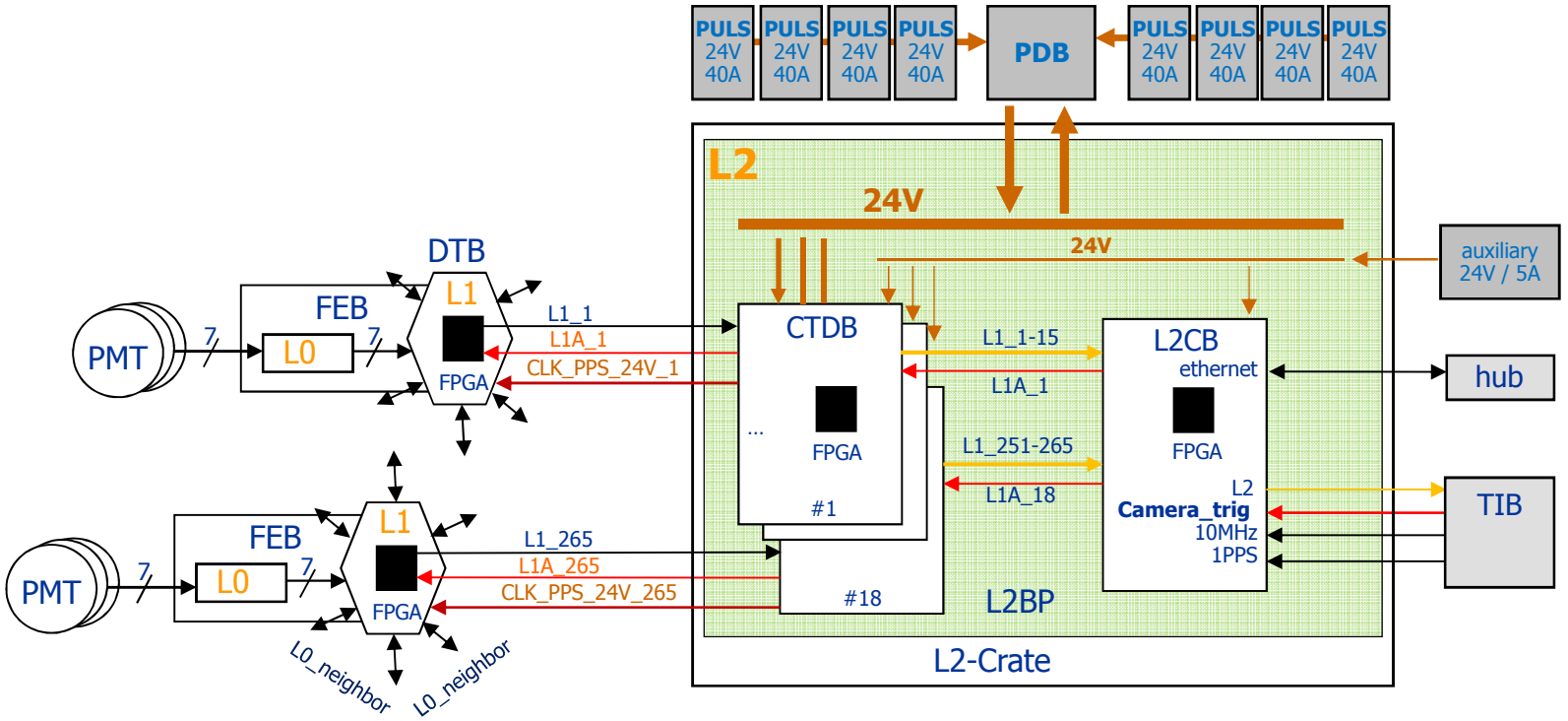
Digital Trigger, Status, December 2017

- firmware status
- FEB powering, firmware fuse
- calibration
- L2, OPCUA implementation
- available hardware and production planned
- next steps
- answering on Julies questions
  - remaining issues of prototypes
  - test benches, test procedures, status
  - administrative procedures
  - SCHEDULE
  - money ... money
  - documentation, status

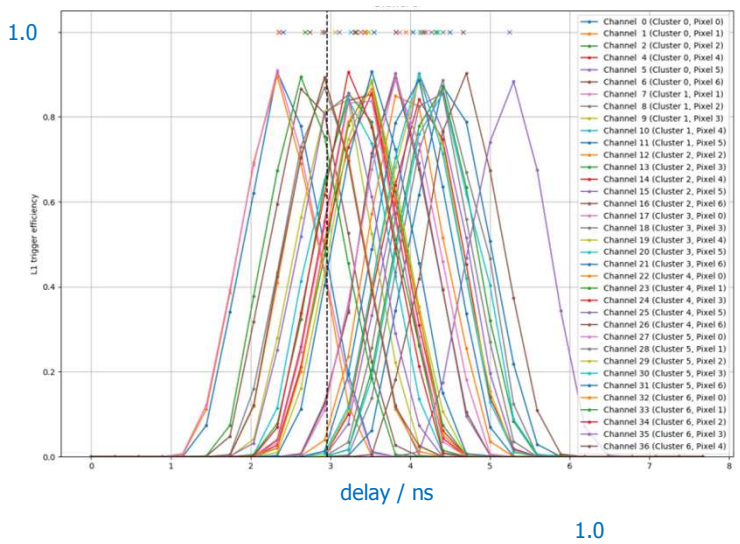
Trigger & Power Topology



DTB4 Firmware Rev.007, Status

- improved L0 delay adjustment
  - improved behavoir, see diagram by Patrick S.
  - no 5ns max. delay limit anymore
  - presently implemented is a max. range of 8ns for each of the 37 L0 signals
  - can be easily extended, e.g. to 16ns, if required
  - no need to tune the analog L0 delays (L0 ASIC)

trigger efficiency vs. L0 delay, 1ns trigger window



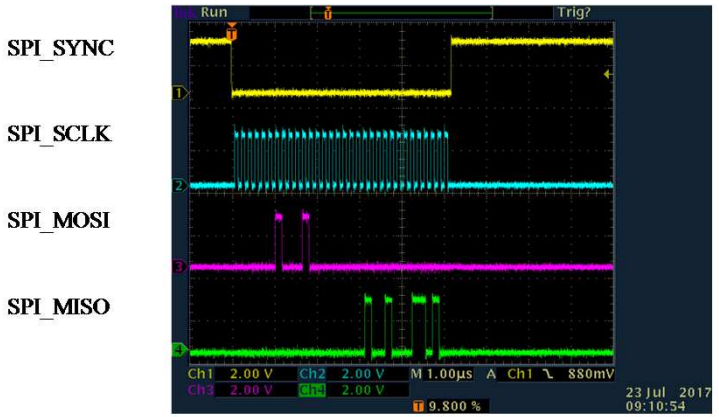
1.0

- PPS_ERR_CT register implemented
  - 50 MHz system clock cycles between consecutive 1PPS pulse are being counted
  - if not equal to exactly 50 Mio., the PPS_ERR_CT increments

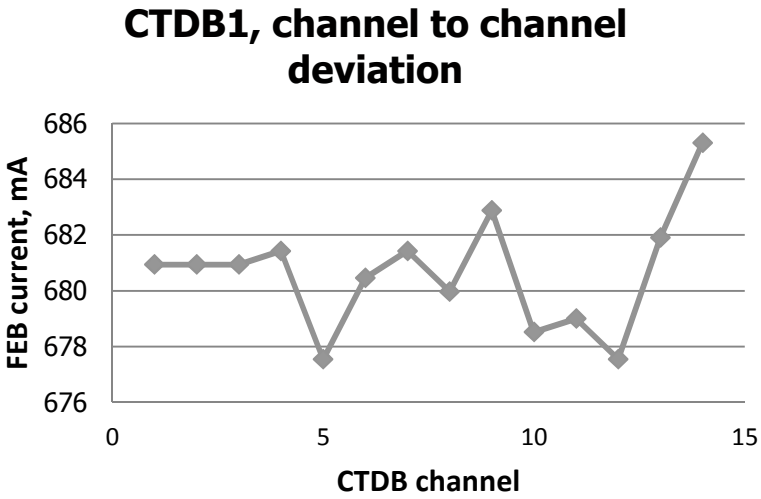
CTDB1 Firmware Rev. 004, Status

- 28 x 16bit register block implemented
  - access via SPI bus (L2-backplane)
  - L2CB is master, controlling 18 CTDBs
  - SPI read / write cycle time is 5.4us
  - e.g., reading 1234h @ addr 20h, slot 2

SPI read of 1234h from reg. @20h, CTDB in slot 2

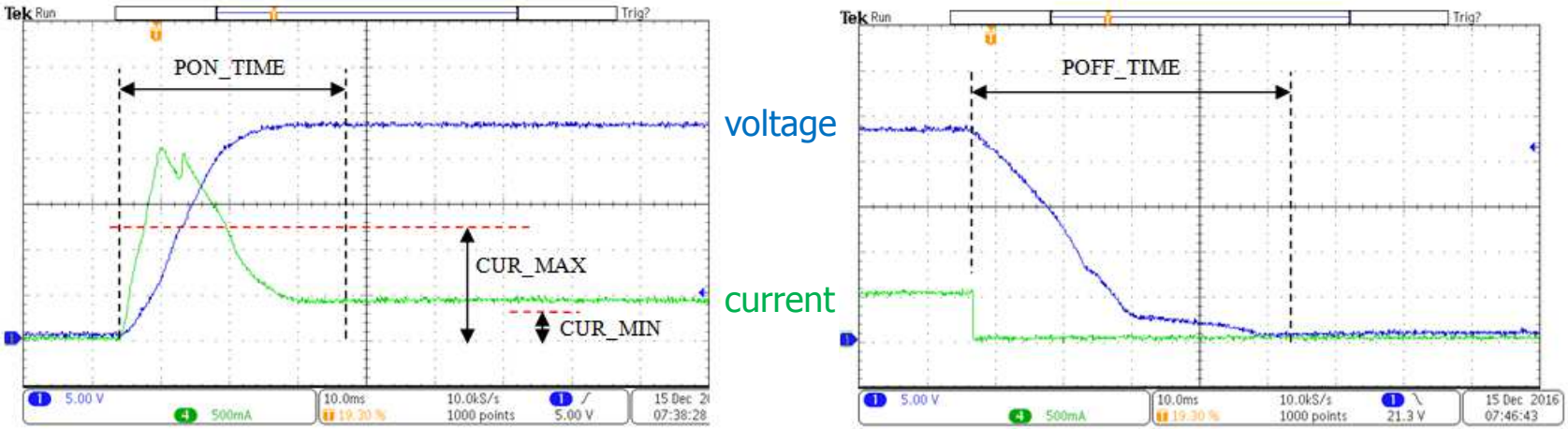


- FEB current measurement implemented
  - range : 0 to 2A
  - 12 bit resolution, 0.485mA / bit
  - accuracy : +/-1 % (prelim.)



CTDB1 Firmware Status, cont.

- Firmware fuse
  - FEB emergency power off in case of over or under (!) current
  - max. fuse delay is 44.8us (by ADC refresh cycle)
  - error status („fuse of chan_x blown") kept, until software toggles the power on bit
  - FEB power cycling, measured, see below
  - programmable max. (1.6A is default) and min. current (100mA is default)
  - programmable disable period (50ms is default) at power on while inrush current flows
  - programmable wait period after power off (60ms is default)



Camera, Power On Sequence

- powering on, all FEBs at the same (almost) time
  - would require 18 SPI write cycles a´5.4us => ~ 100us
  - 24V, overall inrush current load ~265 * 2 A = 530A for about 10 ms
  - Pulse power supplies have dynamic overcurrent capabilty, max. 720A for < 25ms,

  => would work, but is fairly brutal
- powering on, one by one, with 30 ms delays
  - would require 265 * 30ms => ~ 8s

  => fairly long duration
- powering on, 15 FEBs at the same time, with 30 ms delays
  - would require 18 * 30ms => ~ 0.54s

  ⇒ might be the **best compromise**
- other possible ways to reduce the overall inrush current
  - change max. inrush current peak from 2A to 1.2A, by resistor, power on all at the same time => max. 320A
  - force 30ms - sequencing by firmware

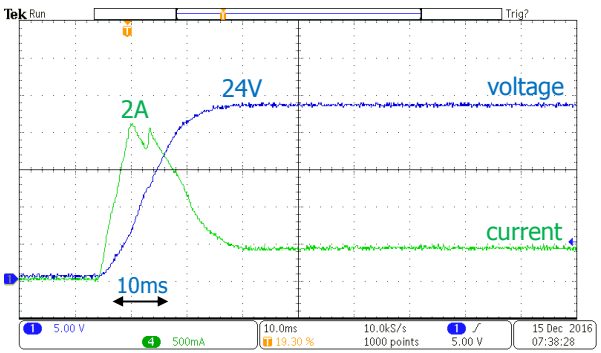
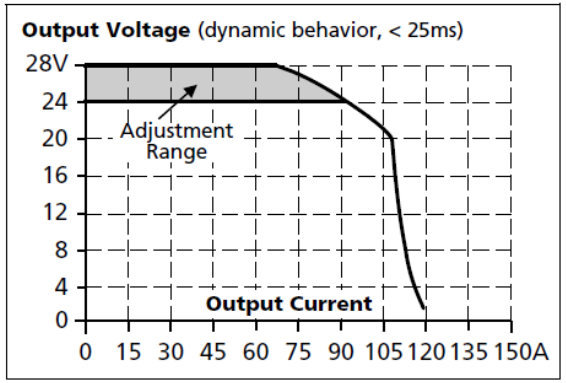
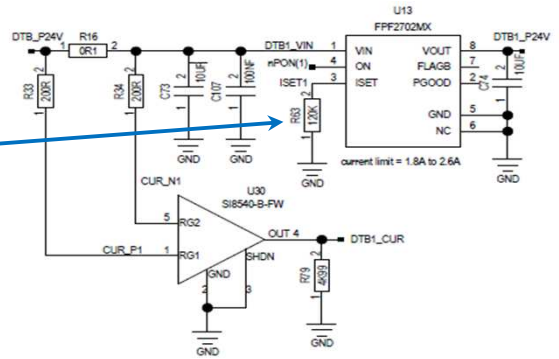


Fig. 6-4 **Dynamic overcurrent capability, typ.**

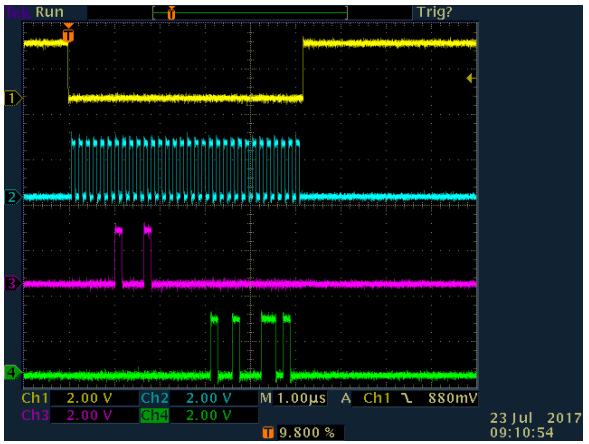




CTDB1 Firmware cont., Debug Register

- the DEBUG register allows to program the usage of the test pin field

DEBUG reg.	test pin field functionality
00h (default)	power on groups of FEBs by setting jumpers
01h	serial ADC1 (U45), monitoring SPI bus signals
02h	serial ADC2 (U46), monitoring SPI bus signals
03h	L2-crate backplane, monitoring SPI bus signals



Calibration

- digital trigger works w/o any calibration already
- for improved performance, four items to calibrate
  1. 1PPS / clock delay
     - method still to be agreed on, see next slides
  2. L0 delays
     - implemented, by using „trig_2_of_37"
  3. L1 up delay (L2CB)
     - possible, based on delay table by Xilinx compiler
  4. L1A down delay (camera trigger)
     - according to latest measurements not required
     - programmable at DTB4
     - possible by analyzing the FEB trigger timestamp
- upper shown calibration sequence should be used
  - digital trigger is a synchronous system
  - best performance, when all clocks are in phase

1PPS & Clock Calibration

- should be the first step of the calibration procedure, several methods possible
- Method 1, using the LED / laser source, could even be triggered by 1PPS
  - using firmware TDCs, take L0 time stamps (central pixel ?)
  - adjust the 1PPS delay accordingly by software
  - pros: fully automated procedure
  - contra: uncertainty of the L0 delay (PMT, L0-ASIC, FEB-FPGA, …)

- Method 2, step by step, 1PPS phase comparison and delay adjustment by DTB4 firmware
  - one time calibration after Digital Trigger installation
  - central FEB as reference
  - needs 264 x plugging of a test cable and pressing a button on the DTB4
  - implemented in firmware, successfully simulated and tested
  - read back and storage of the gained delay value by software
    - local storage / power on reload (EEPROM) by firmware also possible
  - pros: accurate, half automated
  - contra: manual interaction needed

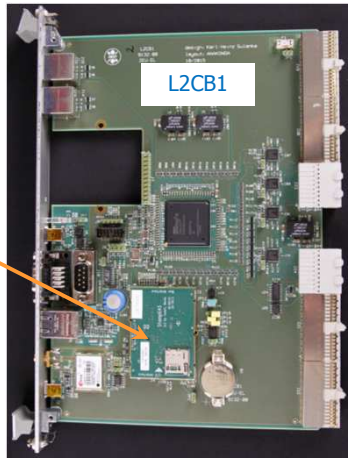
1PPS & Clock Calibration, cont.

- Method 3, step by step 1PPS scope based phase comparison and verification, delay adjustment by software
  - delay is not significantly dependent on temperature and time
  - one time calibration after Digital Trigger installation is sufficient
  - central FEB as reference, using onboard test points + good scope with diff probes
  - read back and storage of the gained delay value by software
  - pros: very accurate
  - contra: manual interaction needed

➢ Method 3 would be my preferred one

- only required once, at the camera assembly phase
- minor effort, if something in the hardware chain CTDB to FEB got changed (e.g. repair)

L2, OPCUA Implementation



- David Melkumyan:

  „I'm done with preparation of the C++ OPC UA SDK binaries for the embedded system...”

- Marek Penno, Marko Kossatz will provide the „hardware access layer“
- presently linux commands do exist, to access the CTDBs, e.g.:

  cta_rw

  root@CTA_L2CB1:~# cta_rw -s2 -w0 -v1234

  write to register [0x0] on slot 2: 0x1234

  root@CTA_L2CB1:~# cta_rw -s2 –rff

  read from [0xff] from slot 2: 0x4

  cta_power

  root@CTA_L2CB1:~# cta_power -s2 --on –all

  root@CTA_L2CB1:~# cta_power -s2 -c7 --on

  root@CTA_L2CB1:~# cta_power -s2 -c7 --off

- more commands will follow soon

Available Hardware and Production planned

- presently available:

item	amount @ CEA	amount @ DESY	amount @ LPNHE	remark
DTB4	21	10	3	Digital Trigger Backplane, 34 pcs.
CTDB1	2	3		Clock & Trigger Distribution Board, 15 chan. each
L2CB1	2	3		L2 Controller Board
L2-Crate	1	2		L2 Crate incl. L2 backplane

- planned production in 2018:

item	amount	date of delivery	remark
DTB4	70	01.04.18	produced at DESY Hamburg
CTDB1	20	01.03.18	produced at DESY Zeuthen, first test of a fully populated L2-crate possible
DTB4	210	01.09.18	produced at DESY Hamburg

Open Questions

- L2-crate
  - how big is the overlap with lower clusters ?
  - is it possible to establish the 24V main power connection by sliding in the L2-crate ?
    - e.g., by using MC power connectors

Type Type Type	Bestell-Nr. Order No. No. de Cde	Gewindeanschluss Threaded bolt connection Connexion sur tige filetée	Leiterquerschnitt Cu Conductor cross section Cu Section du conducteur Cu	Nenn-Ø Stift / Buchse Nominal Ø pin / socket Ø nominal broche / douille	Ausziehkraft Withdrawal force Force d'extraction	Max. Anzugsdrehmoment * Max. tightening torque * Couple de serrage max. *	Belastungsstrom Rated current Intensité assignée	Kontaktwiderstand Contact resistance Résistance de contact	Kurzschlussstrom (1s) Short circuit current (1s) Intensité de court-circuit (1s)	Kurzschlussstrom (3s) Short circuit current (3s) Intensité de court-circuit (3s)
			mm²	mm	N	Nm	A	µΩ	kA	kA
EBB8-V0	01.0474	M8	35	8	20	6	160	60	3	1,5
EBS8-V0	04.0427	M8	35	8		6	160		3	1,5
EBB10-V0	01.0475	M10	50	10	30	10	200	50	5,5	3
EBS10-V0	04.0428	M10	50	10		10	200		5,5	3
EBB14-V0	01.0431	M16	120	14	50	22	300	50	12	8
EBS14-V0	04.0431	M16	120	14		22	300		12	8

- auxiliary power supply, e.g. pulse CS5.241 (32x124x117mm)
  - installation in the PDB or outside the L2-crate possible ?

  => instead 240V AC only 24V connection to the L2-crate required

Next Steps

- organizing the production of 70 DTB4s at DESY Hamburg and 20 CTDBs at DESY Zeuthen
- further firmware developments
  - DTB4
    - improved trigger masking schema
    - L0-TDC for 1PPS calibration as an option (?)
    - more trigger alghorithms (?)
  - L2CB1
    - test firmware to check the signal integrity for the 265 L1 connections
    - L1 up delay calibration by a programmable 2_of_265 AND function
    - storage (FIFO) / readout of the L1 pattern
- L2CB1 user manual update
- OPCUA development
  - test setup, second L2-crate+CTDB1+DTB4, to play with
- L2 crate, depending on the outcome of this meeting
  - auxiliary power supply, integration needed ?
  - connection sheets + plugs / sockets for the 24V main power (50mm2 wire) will be prepared

Answering on Julies Questions

- remaining issues of prototypes
  - L2-crate mechanics and auxiliary power supply position need to be agreed on
- test benches, test procedures, status
  - full test setup do exist
  - test procedures exist, but not yet documented
- administrative procedures
  - not needed
- SCHEDULE
  - see slide „Available Hardware and Production planned"
- money
  - DESY will pay for the first full trigger setup (~60 k€),
  - if it performs like expected and if accepted by the NectarCam team, DESY will pay the trigger for the remaining 14 NectarCams
- documentation, status
  - DTB4 √
  - CTDB1 √
  - L2CB1 -, update needed

Thanks !

Any Questions ?

Backup Slides

CTDB, Power Switch

- R16 (0.1Ω) for current sensing
- power switch U13 (FPF2702MX)
  - TTL-level on/off input (control by FPGA)
  - short circuit proof
  - power ramping (7.5 ms min), switching to current mode if overcurrent
- R63 for **max. current**, see Table 1.
  - two values tried (120K and 270K)
  - see measurements on next slide

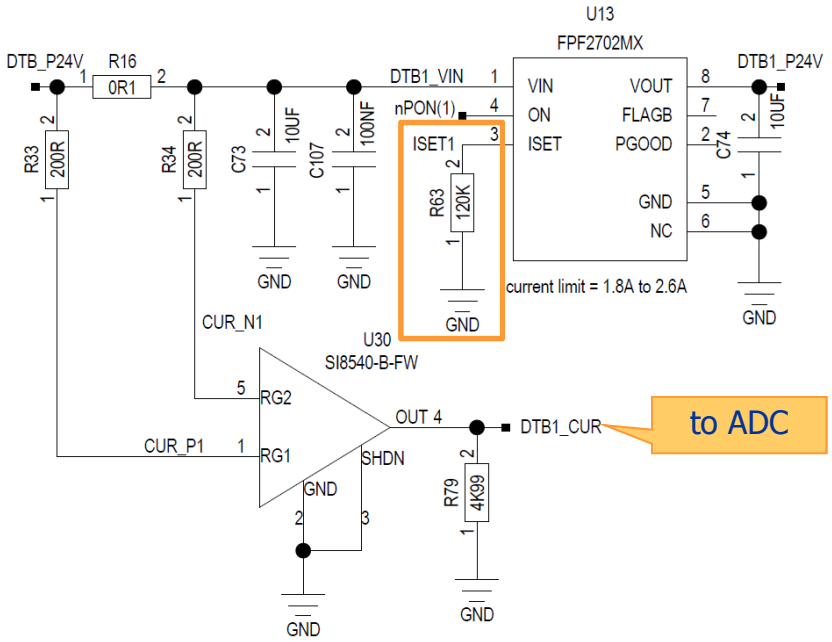
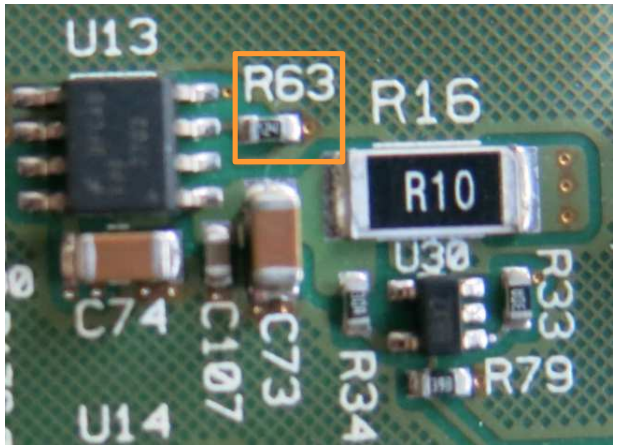


Table 1. R_{SET} Selection Guide

R_{SET} (kΩ)	Current Limit [A]			Tol. (%)
	Min.	Typ.	Max.	
111	2.00	2.50	3.00	20
124	1.79	2.24	2.69	20
147	1.51	1.89	2.27	20
182	1.22	1.52	1.83	20
220	1.01	1.26	1.51	20
274	0.81	1.01	1.22	20
374	0.59	0.74	0.89	20
549	0.40	0.51	0.61	20



DT Costs

- 1000 DTBs assumed
- driven by the DTB
- L1 (DTB) ~ 200 €
- L2 ~5000 €
- Sum = 58000 €
- per pixel ~ 31 €

	A	B	C	D	E	F	G	H
1	Baut Posit	Benennung / Type / W	Hersteller	Hersteller-Nr.	Einze stüc	Menge /VE	Price if 1000 pcs.	Colu
2	C62,C63, C64,C65, C66,C67, C8	Capacitor 1206 47uF 10V 20%	MURATA	GRM31CR61A476ME15	0,26	7	1,82	
3	C9	Capacitor 2220 10uF 50V 10%	KEMET	C2220X106K5RAC	1,10	1	1,10	
4	F1	Misc SERIE 453 T-1A 1A	LITTELFUSE	0154001.DR	1,53	1	1,53	
5	J1,J2,J3,J4 ,J5,J6	Connector EHF-120-01-L-D Gold-Plated 1.27 mm Terminale block 0'	Harwin	M50-3552042	1,92	6	11,52	
6	J11,J12	Connector 6469025-1 Gold-Plated Header Shielded z-pack Bus-Kontaktblock High Speed	TE CONNECTIVITY	6469025-1	5,60	2	11,20	
7	J13	Connector CAT5 Gold-Plated Female Shielded Straight	MOLEX	85508-5001	2,24	1	2,24	
8	J14	Connector 1840417-4 Gold-Plated Phosphor Bronze vertical	TE CONNECTIVITY	1840417-4	5,00	1	5,00	
9	J17	Connector 87832-1420 2 mm Male Straight Zweireihig	MOLEX	87832-1420	0,82	1	0,82	
10	L2	Inductor 10uH Ferrite Inductor Power Magnetic Shielded	WUERTH ELEKTRONIK	74488430100	1,44	1	1,44	
11	L5	Inductor 74408943022 High Q factor Inductor High Current Low DC Resistance Power 2,2uH	WUERTH ELEKTRONIK	74408943022	1,60	1	1,60	
12	L1,L2,L3, L4,L7	ferrite 0805, 1A, 0R3, 1K	WUERTH ELEKTRONIK	742792096	0,14	5	0,70	
13	U1	IC XC6SLX16-3CSG324I FPGA	XILINX	XC6SLX16-3CSG324I	**37,17**	1	37,17	
14	U2	IC AT45DB081D-SU Flash Memory FLASH Serial	ATMEL	AT45DB081D-SSU	1,60	1	1,60	
15	U3	IC ADCMP604BKSZ-R2 Comparator LVDS Fast	ANALOG DEVICES	ADCMP604BKSZ-R2	2,65	1	2,65	
16	U5	IC TMP05BRTZ Temperature Sensor	ANALOG DEVICES	TMP05BRTZ	1,17	1	1,17	
17	U6	IC LT3680EMSE#PBF Regulator Supply Positive	LINEAR TECHNOLOGY	LT3680EMSE#PBF	5,06	1	5,06	
18	U7	IC MCP1826S LDO Regulator Voltage Regulator, Positive, 2.5V	MICROCHIP	MCP1826S-2502E/DB	0,52	1	0,52	
19	U8	IC MCP1826S LDO Regulator Voltage Regulator, Positive, 1.2V	MICROCHIP	MCP1826S-1202E/DB	0,52	1	0,52	
20	V1,V2	Diode DO-214AC MBRA340T3G 40V	ON SEMICONDUCTOR	MBRA340T3G	0,16	2	0,32	
21	V3,V4,V5, V6,V7,V8, V9	Diode SOT323 BAT54SW 30V	NXP Semiconductors	BAT54SW	0,33	7	2,31	
22	U9	IC DS2431P+ EEPROM ,1KB,1-WIRE,TSOC6	MAXIM	DS2431P+	0,70	1	0,70	
23	C76	EMI filter, 1206, 22nF, 2A, 50V	MURATA	NFM3DPC223R1H3L	0,23	1	0,23	
24	SW1,SW2	push button switch, SMD	Bourns	7914J-1-000E	0,40	2	0,80	
25	J1..J6, cable connector	socket, IDC, 1.27MM, 40 Way	Harwin	M50-3302042	1,94	6	11,64	
26	cable	flat cable, 30 AWG, 7x0.1mm, 50 way, 122 ohm, 0.635mm, PVC	3M	3754-40	0,21	3	0,63	
27	J15, cable connector	socket, 2x4 way, crimp, HE14 series	TE CONNECTIVITY	281839-4	0,27	1	0,27	
28	J15, crimp contacts	crimp contacts, AWG 24-28, 0.8...1.5mm,	TE CONNECTIVITY	182734-2	0,14	4	0,56	
29		cable Cat.6a, 3m	KabelScheune	PP6.030.GE	4,19	1	4,19	
30	PCB	PCB, 8 layers	Contag	8884-00	**66,00**	1	66,00	
31	assembly				**20,00**	1	20,00	
32					L1	sum	**195,31**	
33					L2	sum	**4800,00**	
34						**overall sum**	**56557,15**	
35						**sum / pixel**	**30,49**	

Prototype Status, Summary

- Hardware
  - the 4 custom made board types are fully functional w/o any known PCB bugs
  - presently new revisions are neither planned nor needed
- Firmware
  - DTB4
    - progr. trigger type: 3NN_of_37, OR_1_of_7, OR_1_of_37, AND_2_of_37
    - progr. trigger window (1,**3**,5,7 ns or no limit)
    - progr. delays: 1PPS, L1A, L0s
    - SPI bus interface, pixel masking, etc …
  - CTDB1
    - SPI bus interface
    - power switching
    - FEB current measurement incl. firmware fuse
  - L2CB1
    - high speed memory interface to the ARM MCU
    - SPI bus interface (for CTDB control)
    - L1 masking
    - L1 delay programming

Prototype Status, Summary cont.

- Software
  - L2CB1
    - remote firmware update
    - power switching
    - register read / write tool