Digital Camera Trigger Status

May 2013

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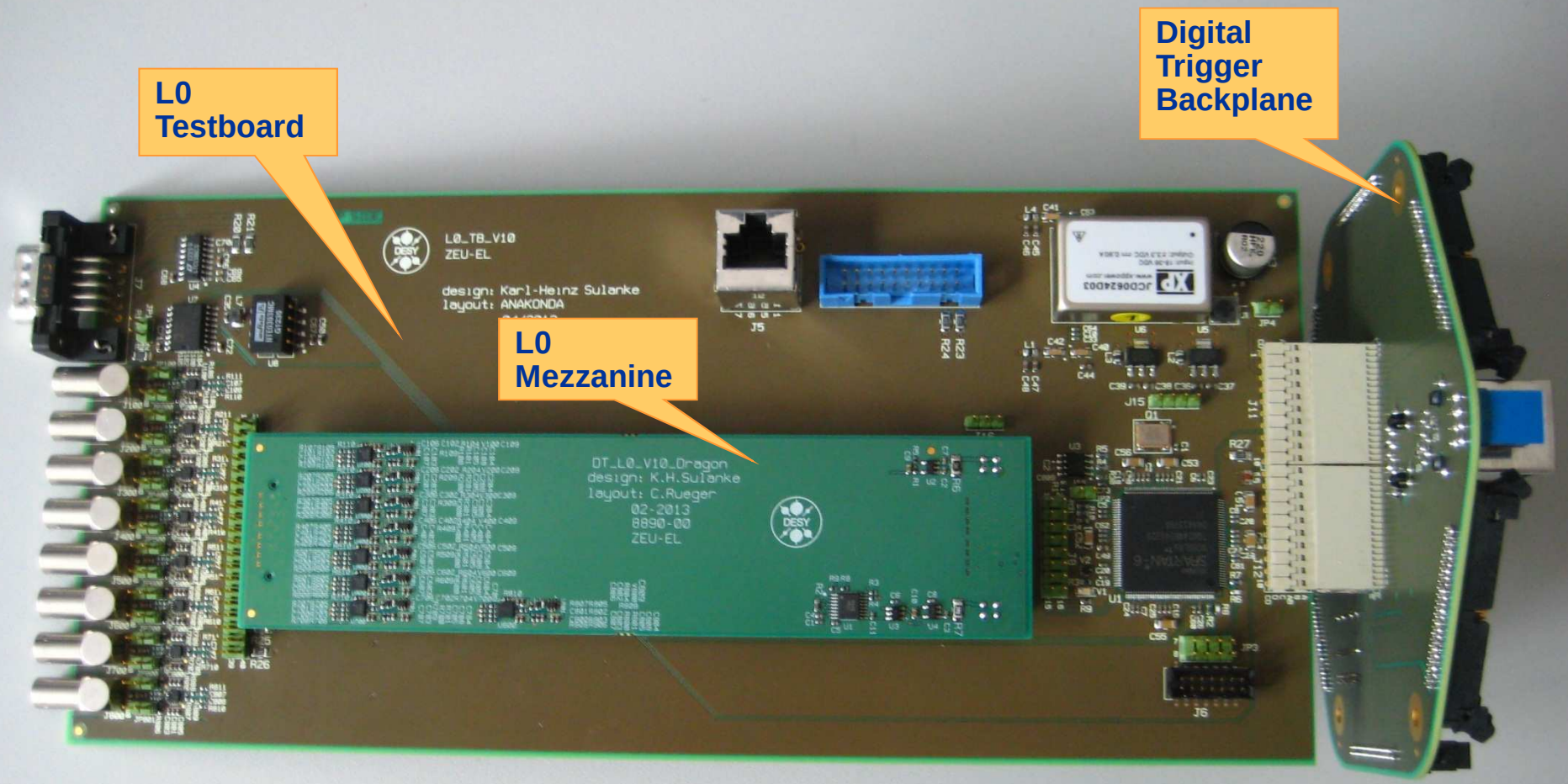
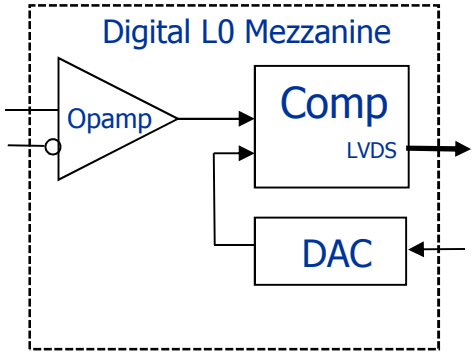
DESY

Three New Boards Developed



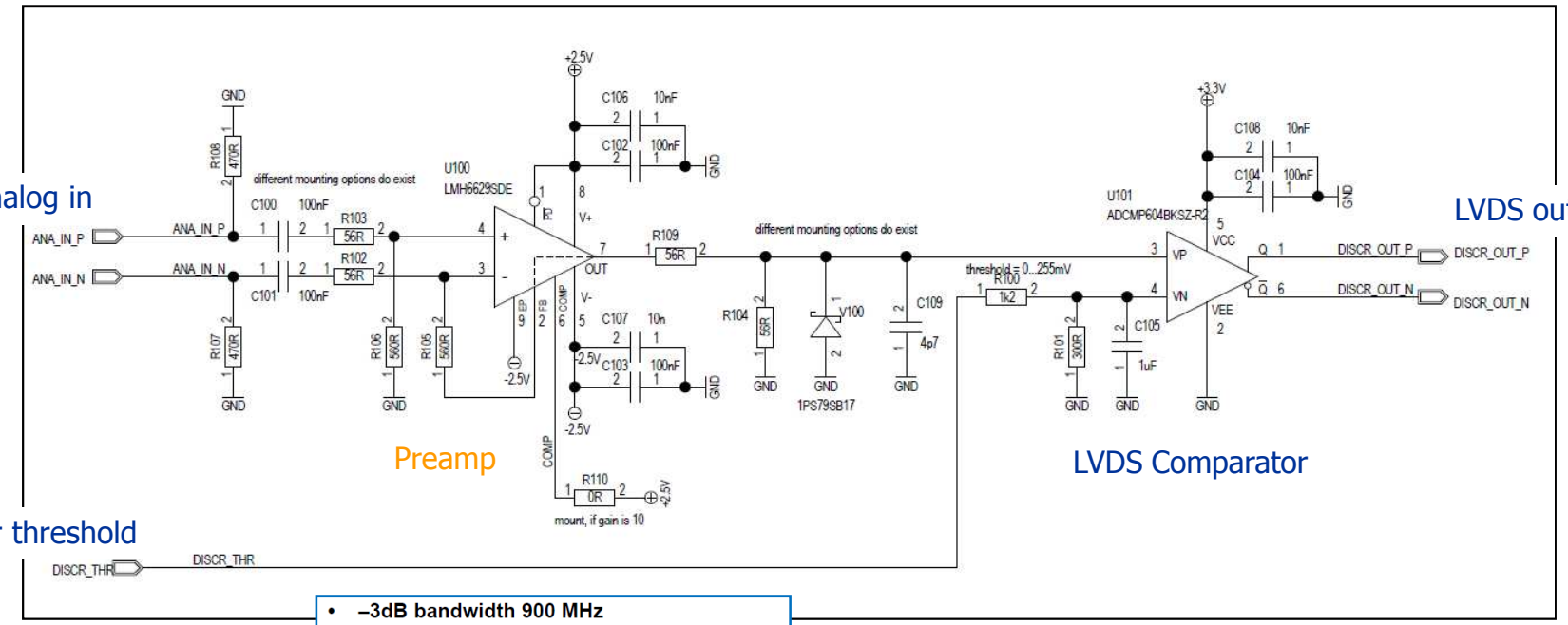
Digital Trigger L0 Mezzanine Board

- Schematic simulated, very low noise preamplifier
- Two PCBs, a DRAGON - and a NECTAR - version
- 6 + 6 L0 boards assembled
- First test results expected next week



Diff. Analog in

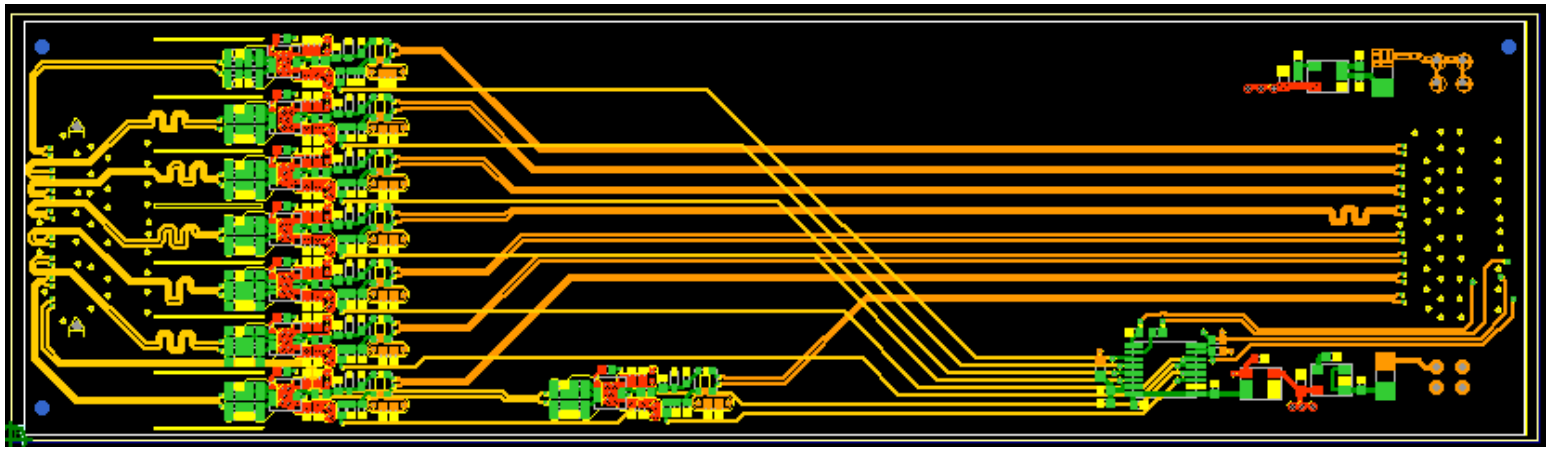
LVDS out

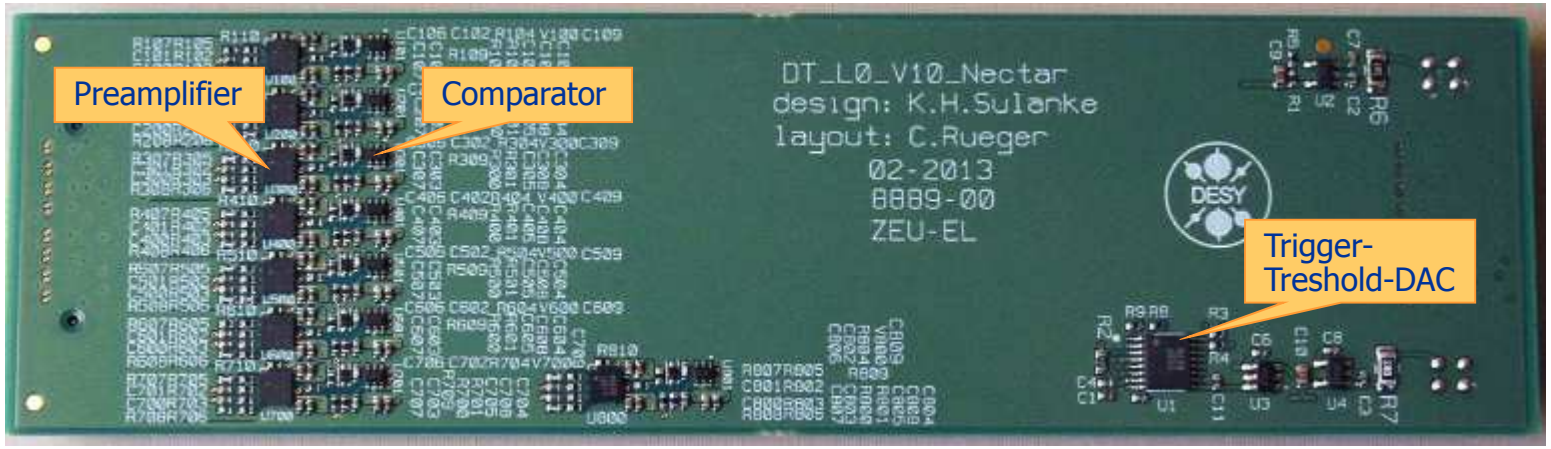


- **–3dB bandwidth 900 MHz**
- **Input voltage noise 0.69 nV/√Hz**
- **Input offset voltage max. over temperature ±0.8 mV**
- **Slew rate 1600 V/ µs**

Digital Trigger L0 Mezzanine Board

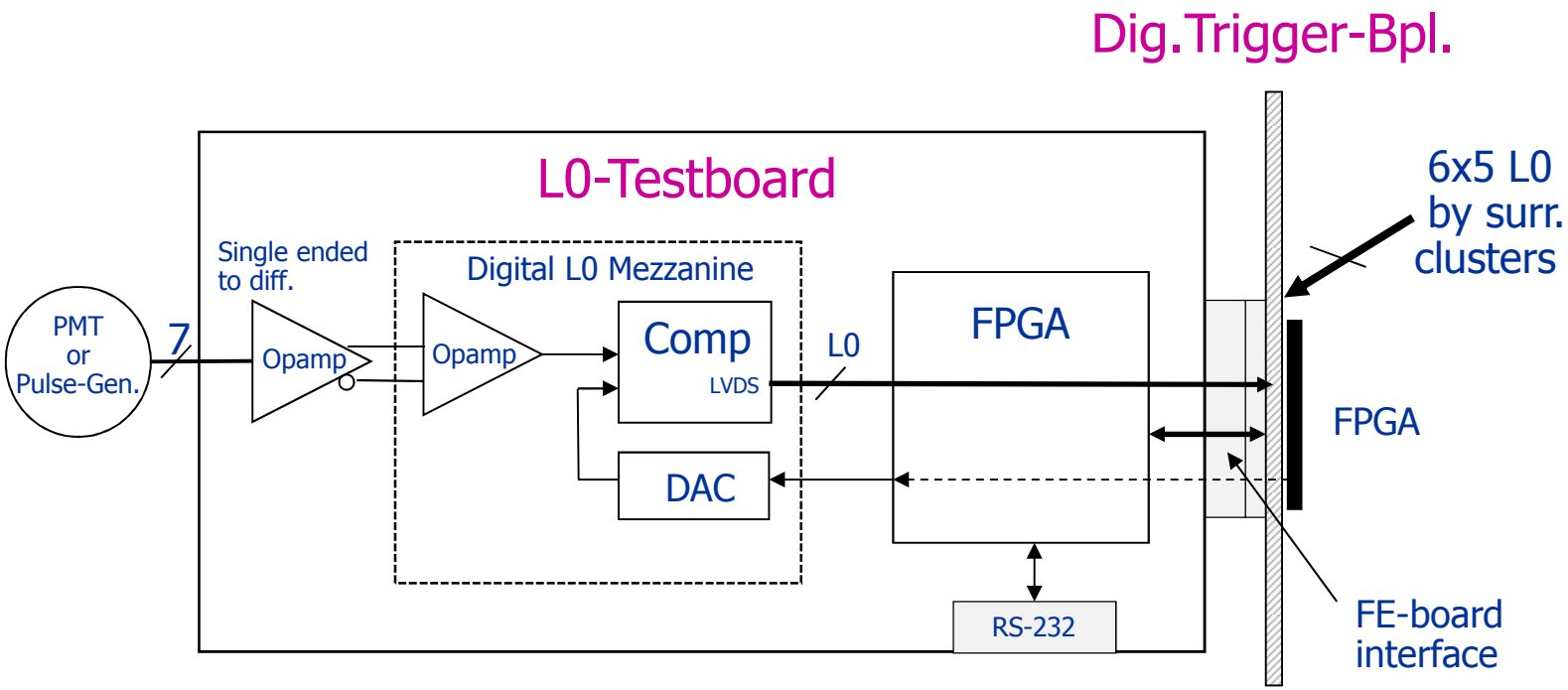
- 6 layer PCB with length-tuned signal lines





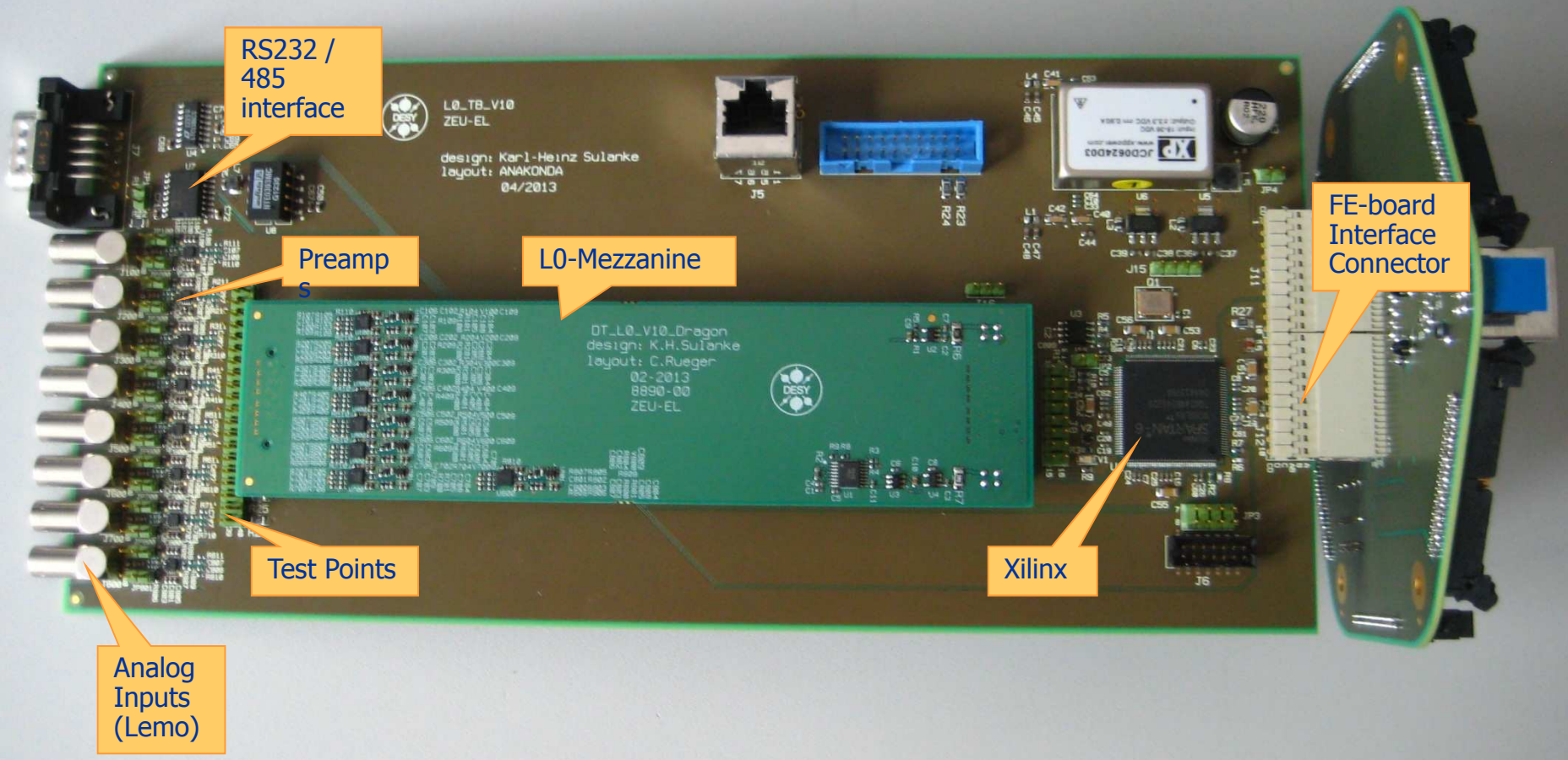
Digital Trigger L0 Test Board

- Testing the L0 boards AND the FE-board interface of the Dig. Trigger Backplane
- Xilinx with RS232 / RS485 interface, to set the discriminator thresholds etc.

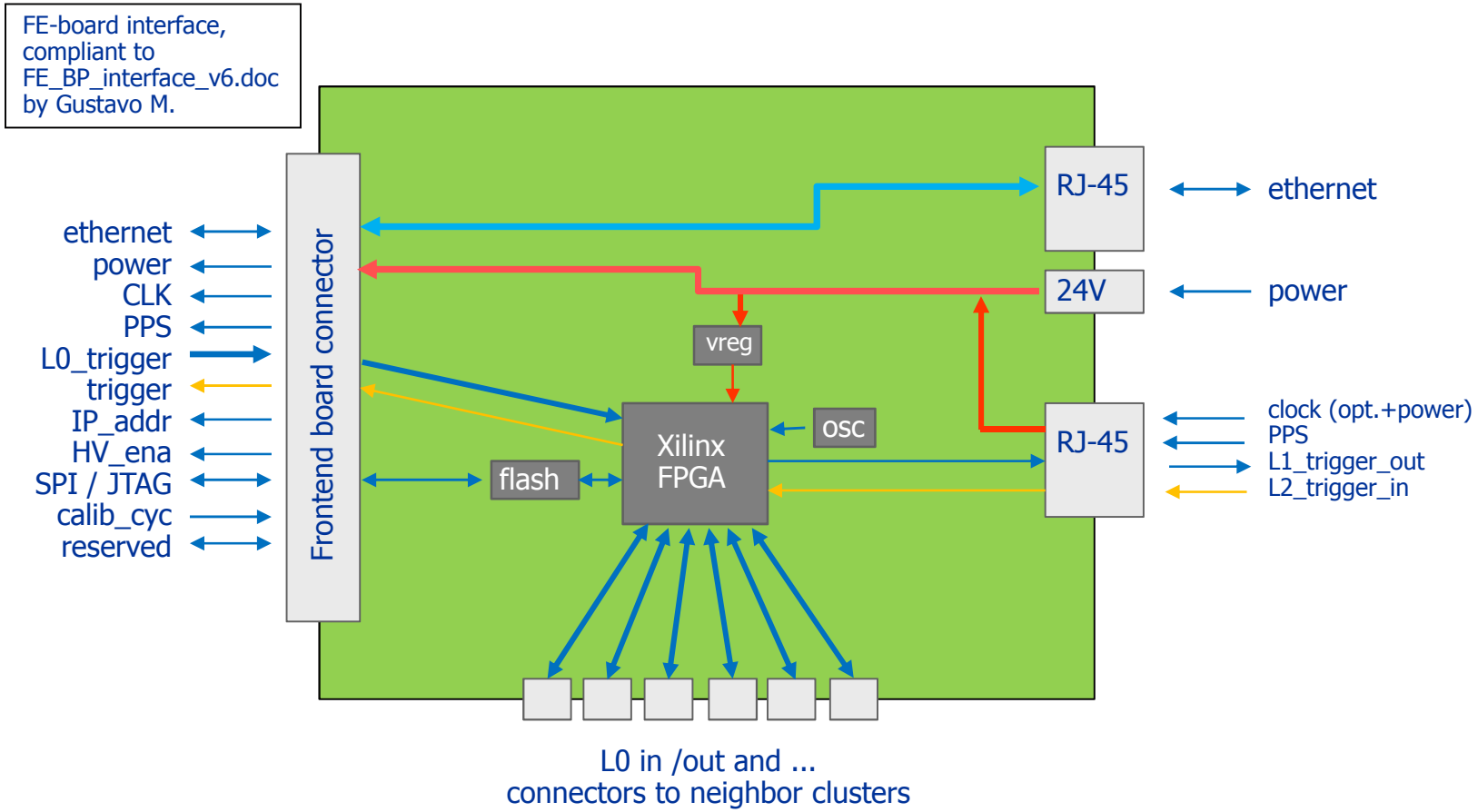


Digital Trigger L0 Test Board, cont.

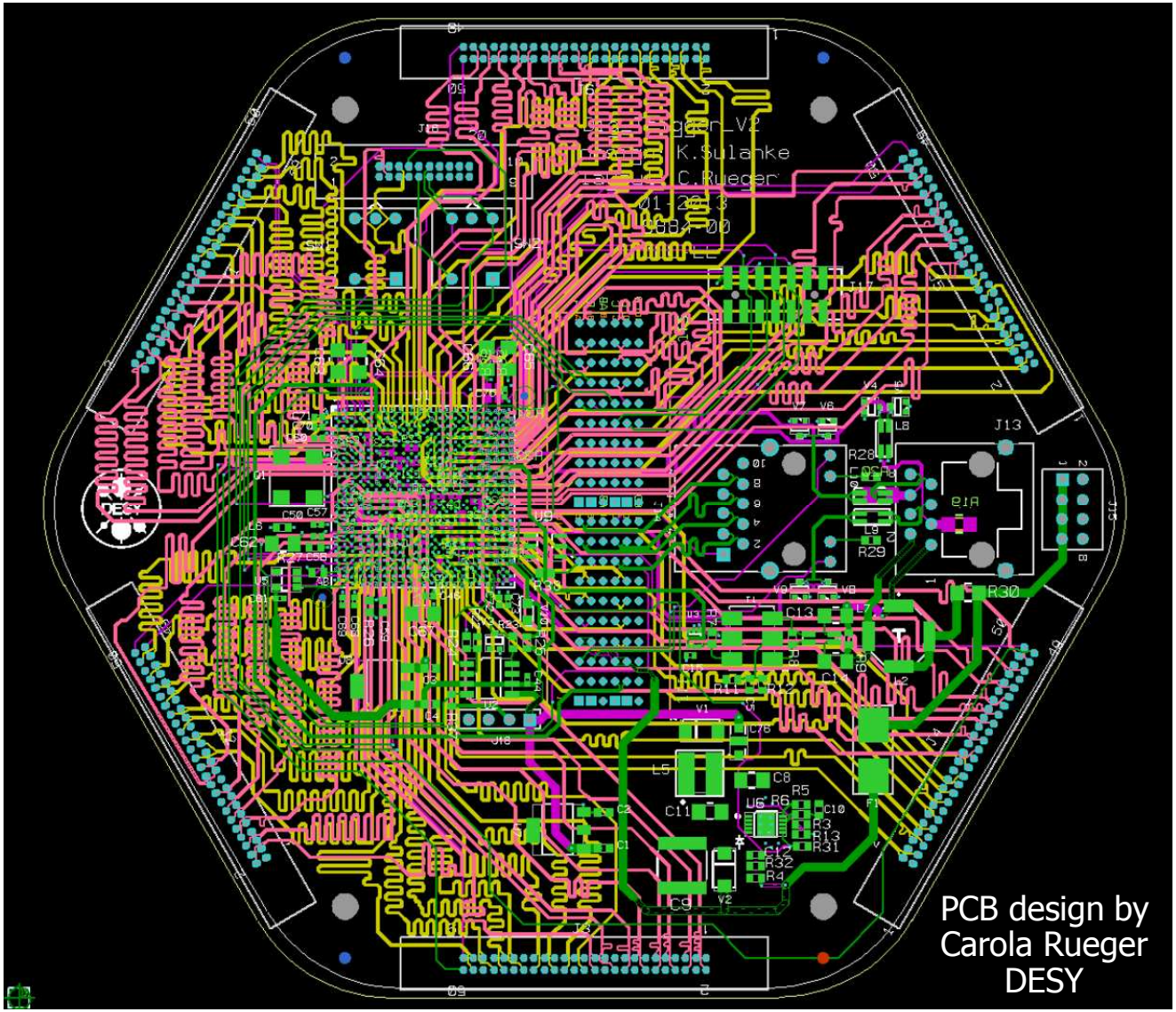
- 120 mm x 260 mm, 6 Layer PCB, various analog and digital test points
- DESY workshop delivered the first assembled board last Friday



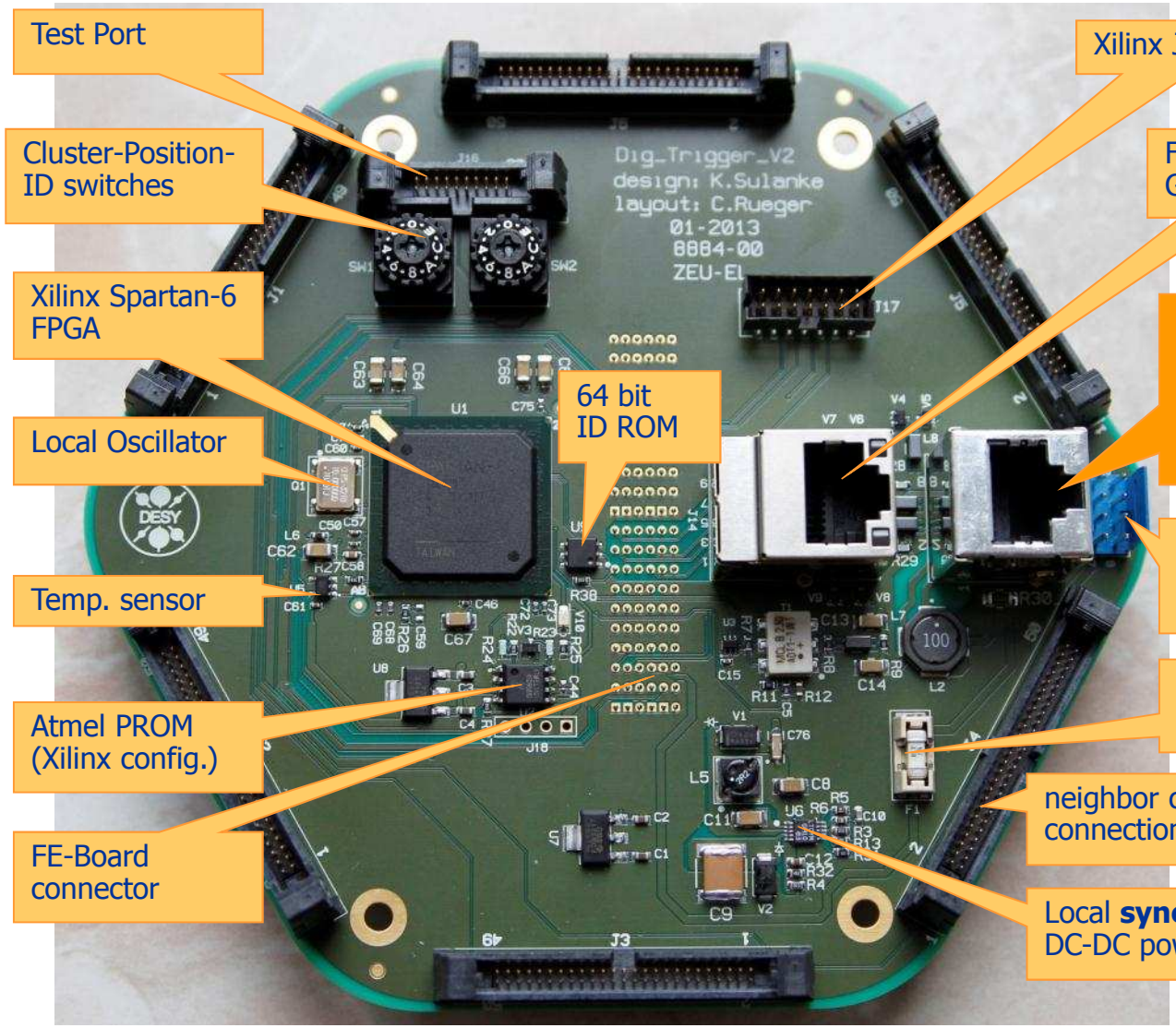
The Digital Trigger Backplane Rev. 2



Digital Trigger Backplane, 8 Layer PCB



Digital Trigger Backplane, cont.



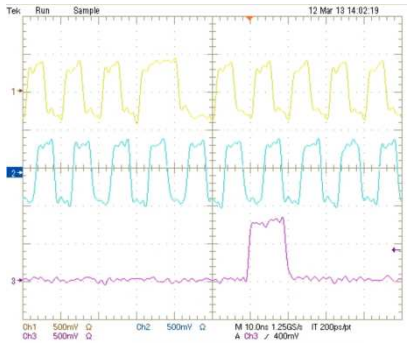
Digital Trigger Backplane, Status

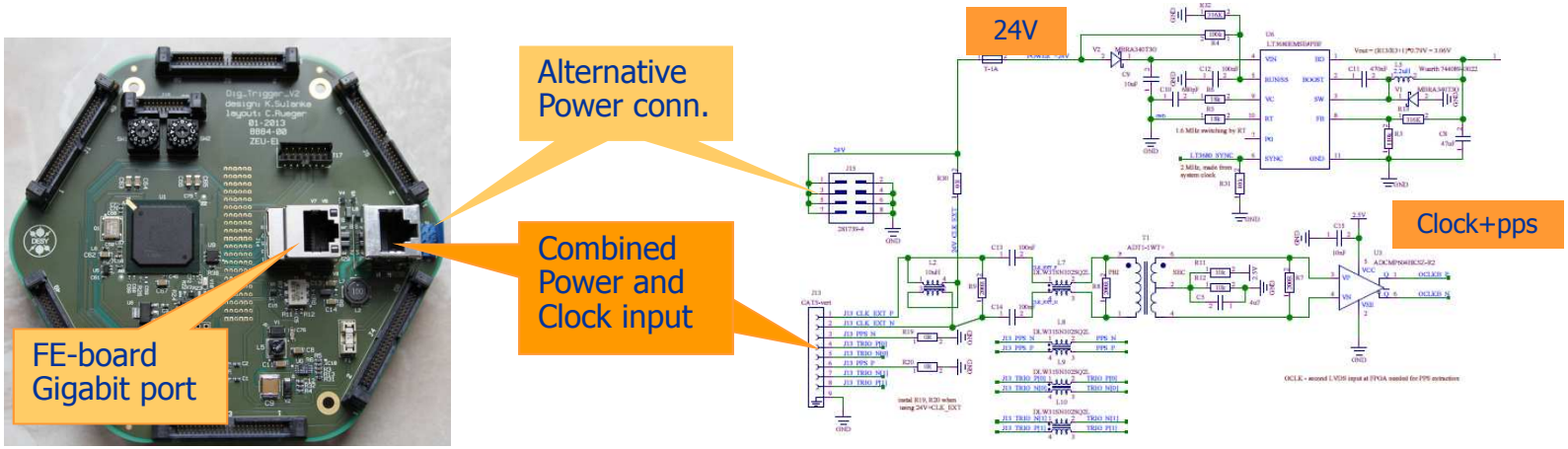
- 3 boards (of 5 PCBs) assembled by the DESY workshop
- Tests :
  - Power supply √
  - Xilinx configuration via JTAG or PROM √
  - Local and external clock √
  - LVDS Interface (signal integrity) to neighbor clusters √
  - Inverse mode (for testing), used as a 37 bit pattern generator √
    - Minimum (clean) signal width is 1.25 ns
  - Combined power / clock / pps / L1_out / L2_in RJ45-connection √
    - Saves cabling
  - Various trigger alghorithms (firmware), ongoing
  - distributed schema for clock / PPS / L1 (firmware), -
  - Temperature sensor, -
  - FE-board interface , -

Combined Power and Clock Input

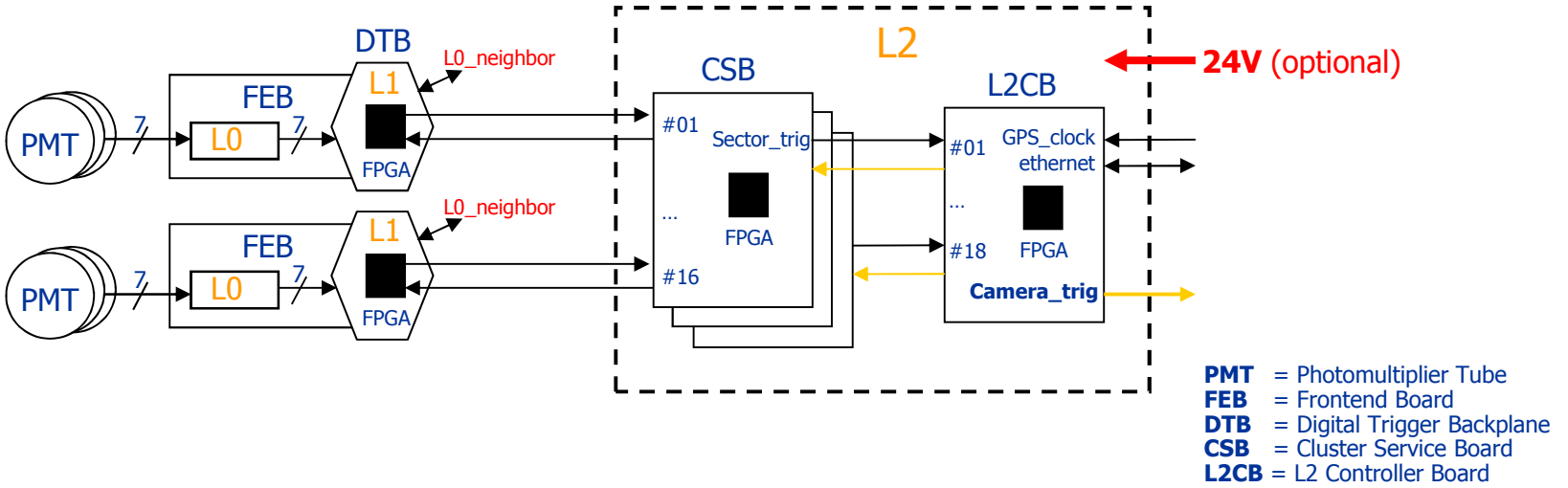
- 24V, clock, and PPS over a single wire pair
- requires a single cat5e cable per cluster only (+ gigabit ethernet cable)
- Current jumps of 0.8 A did not influence the (recovered) clock quality

Cat5e - Wire Pair	Standard mode	Combined mode
1	Clock_in	Clock_in / PPS_in / 24V
2	PPS_in	GND
3	Trig_L1_out	Trig_L1_out
4	Trig_L2_in	Trig_L2_in





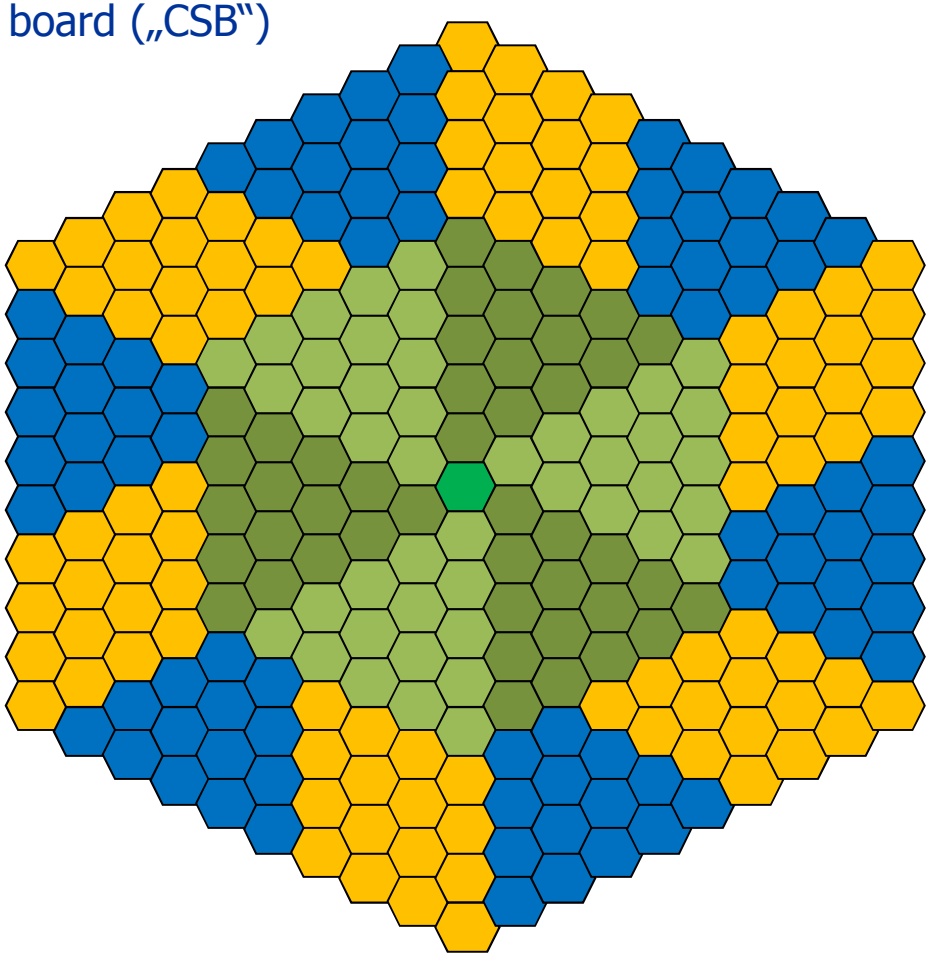
The Centralized Trigger Schema with L2



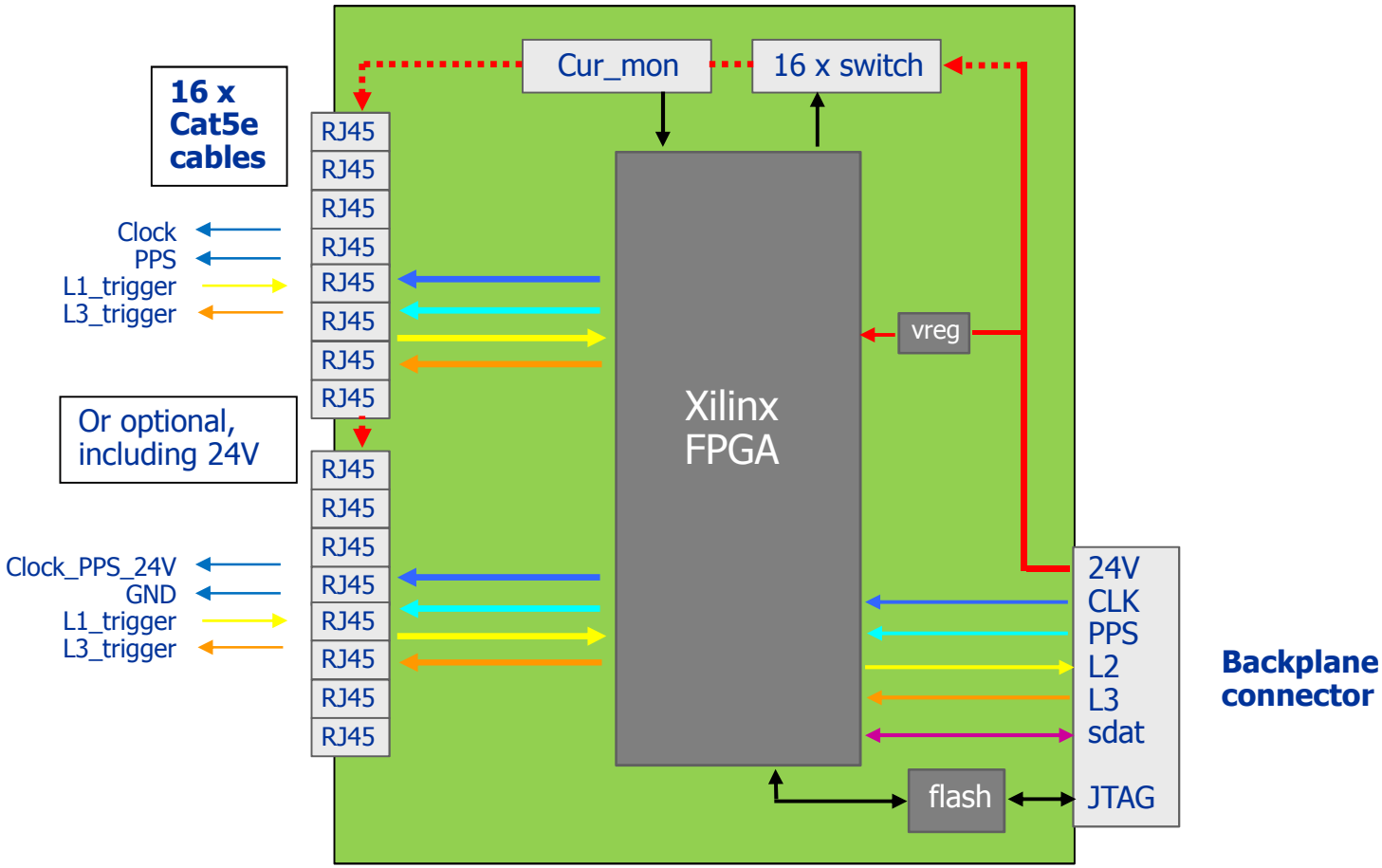
- L2 also based on Xilinx-Spartan 6 FPGAs
- L2 is a crate, ~ 50 x 20 x 20 cm, ~ 11 kg
  - 18 x CSB (Cluster Service Board)
  - 1 x L2CB (L2 Controller Board)
    - Ethernet interface
    - Optical / electrical camera trigger output

L2 Trigger Sectors, MST, Example

- 271 cluster shown (1897 pixel)
- Each sector comprises 14..16 clusters and is connected to a certain L2 board („CSB“)



The Cluster Service Board (CSB)



Summary

- The Digital Trigger Backplane supports both, a distributed and a centralized schema, for the L1 trigger, the clock and the PPS-signal
- Centralized trigger schema preferred by me
- Boards needed for a distributed schema (preferred by the analog trigger group):
  - Digital Trigger L0 mezzanine
  - Digital Trigger Backplane
- A lot of firmware writing and hardware testings needed now
- L2 hardware development with lower priority
  - Single CSB sufficient for a mini camera of up to 16 clusters
- Design progress in time with the FE-board (Nectar, Dragon) development

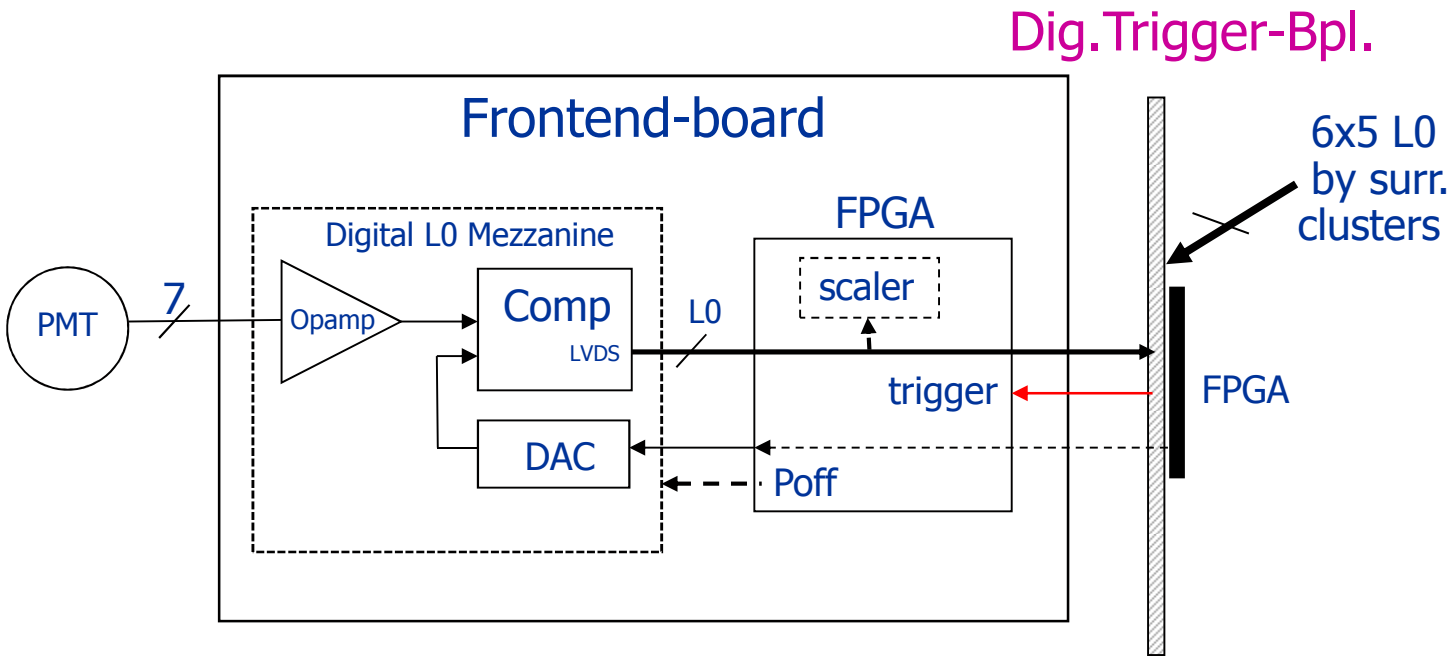
Outlook

- Assembly of about 25 Digital Trigger Backplanes planned (3 x 7 plus spares) until end of July
- CSB prototype will be available end of September

Back Up Slides

Digital L0 through Frontend-Board FPGA

- Allows Frontend-board-FPGA with scaler
- uniform FPGA internal delay (by constraints) preferred
- Trigger threshold DAC control by trigger FPGA, optional
- Separate power island with software controllable shutdown doable

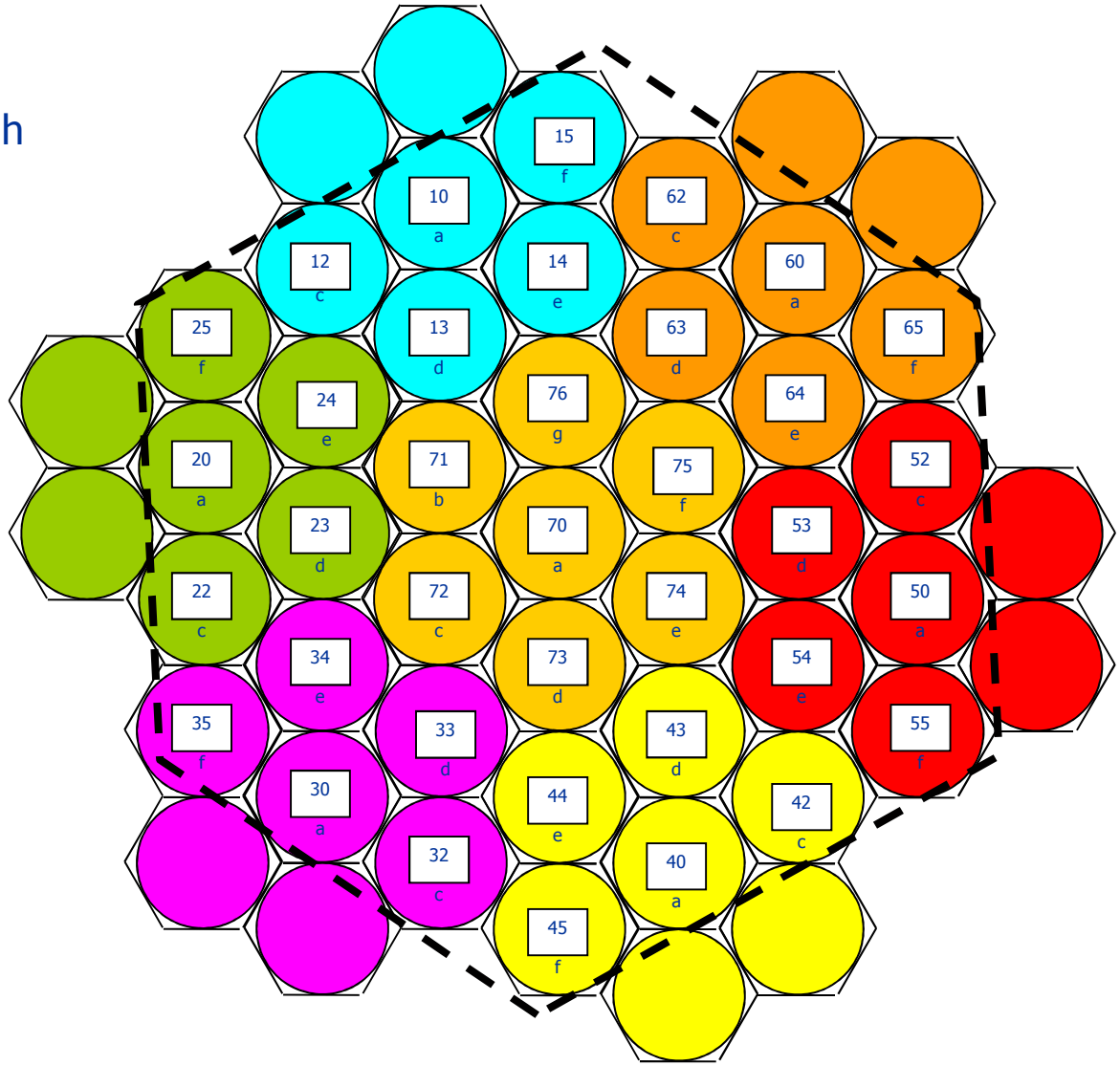


Digital Trigger Backplane, List of Key Hardware Features

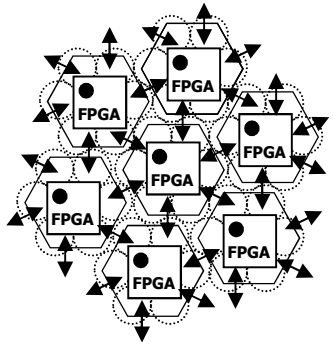
- Nominal power consumption: 1.5 W
- Weight : 95 g + 10 g cabling to neighbor clusters -> 28 kg for LST
- Automatic neighbor cluster recognition (border zone)
- Synchronous DC-DC converter (24 V to 3.0 V …)
- Local clock and external clock input (any diff. > 0.1V pk-pk)
- FPGA load by JTAG cable or PROM or remote (by FE board)
- 6 x bidirectional L0 signal connection with neighbor cluster
- Temperature sensor (allows automatic delay correction, if needed)
- adjustable 8 bit cluster position ID (for unique, position-independant, firmware)
- Gigabit ethernet pass through connection to FE-board
- RJ 45 connector as combined power and clock input (single cat5e cable)

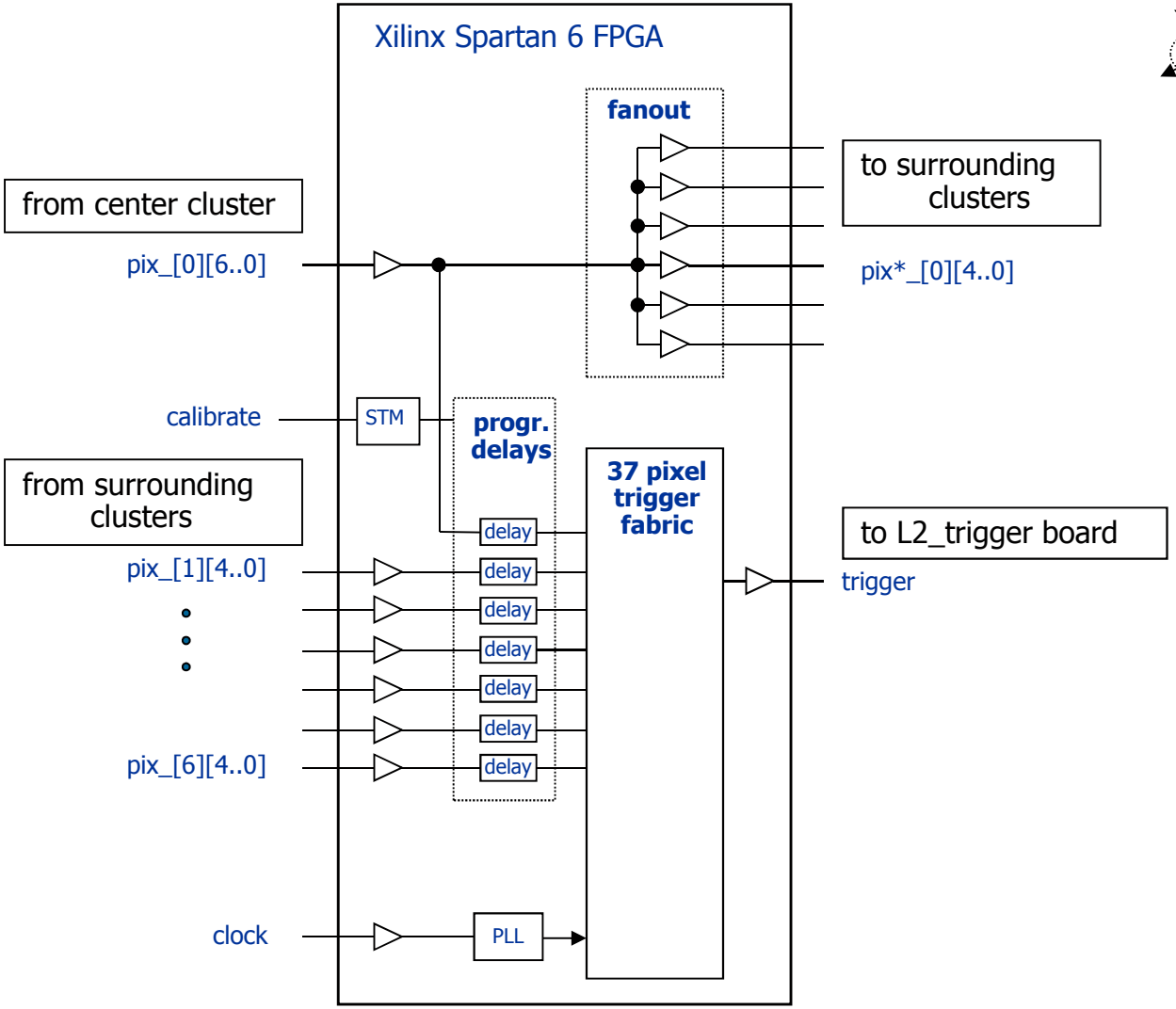
From 49 Pixel to 37 Pixel Regions

- Overlap still big enough
- Saves FPGA pins and money
- Allows daisy chained schema for clock/pps



The DTB-FPGA's Functionality





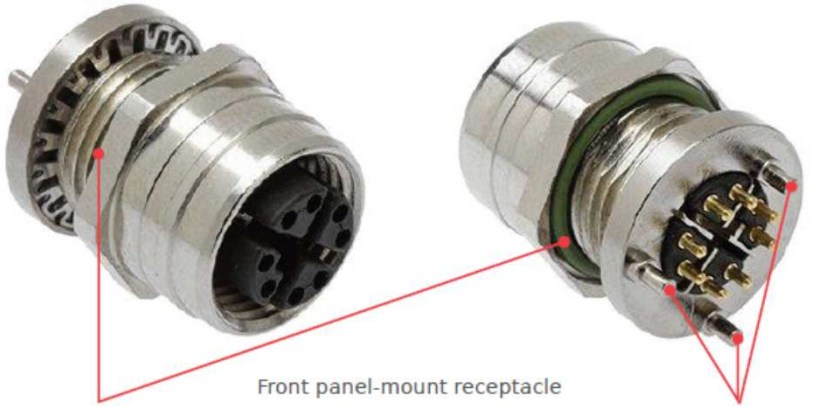
Digital Trigger Backplane, Basic Firmware Features

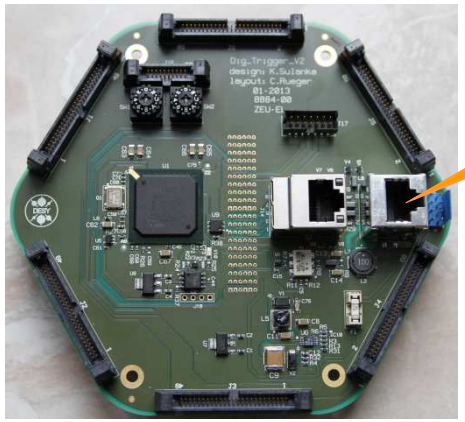
- 37 or 49 pixel areas, depending on the trigger / clock mode (distributed or centralized)
- Minimum Trigger window is 1.25 ns
- Individual L0 delay calibration in 50 ps steps

M12 Cat6 , Combined Power / Clock Input

- Instead of RJ45, more robust
- by Harting, Molex, ...

M12 Male-to-Male Cable Assemblies





To be replaced by M12