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A Digital Camera Trigger for the Cherenkov Telescope Array

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Abstract: The cameras of the Cherenkov Telescope Array (CTA) will be equipped with a local trigger logic that uses the pixel amplitudes to enrich possible shower images and to suppress background signatures. We describe a possible camera trigger, based on the processing of overlapping pixel regions in a camera. The trigger consists of three stages. The first stage (L0) is an accurate high speed PMT pulse discriminator. The second stage (L1) is a single, low cost FPGA, processing overlapping 37-pixel regions. Different trigger algorithms (such as three-next-neighbor trigger or more sophisticated schemes) can be implemented and can even run in parallel. Besides its flexibility, the possibility to adjust the individual L0-delay in the sub nanosecond range is another major advantage of the FPGA-based trigger. Overall, a 1.2 ns trigger window can be achieved this way. The third stage (L2) is either implemented in a central cluster FPGA or as a separate hardware unit. First successful tests of the digital trigger scheme will be presented.

Keywords: Cherenkov telescopes, trigger, readout, FPGA.

1 Introduction

The astroparticle physics community aims to design and build the next generation array of Imaging Atmospheric Cherenkov Telescopes (IACTs), that will further expand the very-high energy astronomy domain [1, 2, 3]. In order to gain an order of magnitude in sensitivity in the energy range from a few GeV to tens of TeV, the Cherenkov Telescope Array (CTA) will employ 50-100 IACTs of various sizes equipped with 1000-4000 channels per camera. The increased number of channels (two orders of magnitude with respect to the current IACT arrays such as H.E.S.S. [4] or VERITAS [5]) will require well elaborated camera trigger and readout design in terms of cost and performances.

The challenge of the camera trigger is to extract gamma-like events out of a tremendous amount of noise, caused by the Night Sky Background (NSB). The described trigger implementation is based on a low cost FPGA which processes overlapping 37-pixel regions. A simple strategy would be to look for the coincidence of signals of neighboring pixels in a narrow time window. Other algorithms such as majority trigger, or sliding doublets or triplets, can be implemented as well or even run in parallel. Due to the FPGA reprogrammability other innovative algorithms can be tested. A unique feature of this trigger is the ability to deal with a sliding trigger window. The trigger design, initially developed for the mid-size CTA telescopes, can be easily adapted for other telescope types [6].

2 Architecture

The trigger scheme shown in Fig. 1 consists of 3 levels, L0 to L2. The L0 stage is a pre-amplifier followed by a programmable discriminator. Seven of them, one per pixel, are located on the front-end board (FEB). The discriminator output signals are passed to the L1 stage, the digital trigger backplane (DTB). The L1 signals of each DTB are connected via a standard Cat5e cable to the Cluster Service Board (CSB). Eighteen CSBs are plugged to the L2 crate. Each CSB services up to sixteen DTBs. Besides the L2 decision, other tasks, like clock + Pulse Per Second (PPS) and power distribution are being fulfilled by the CSB as well. Finally, the L2 Controller Board (L2CB) processes the eighteen L2 signals and generates the camera trigger.

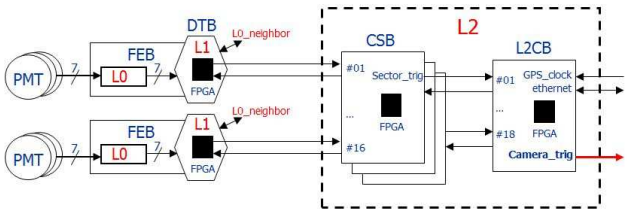

Figure 1: Architecture of the Digital Camera Trigger

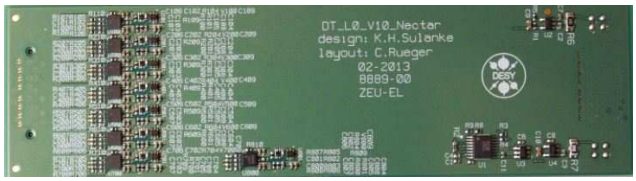

Figure 2: L0 Mezzanine Board

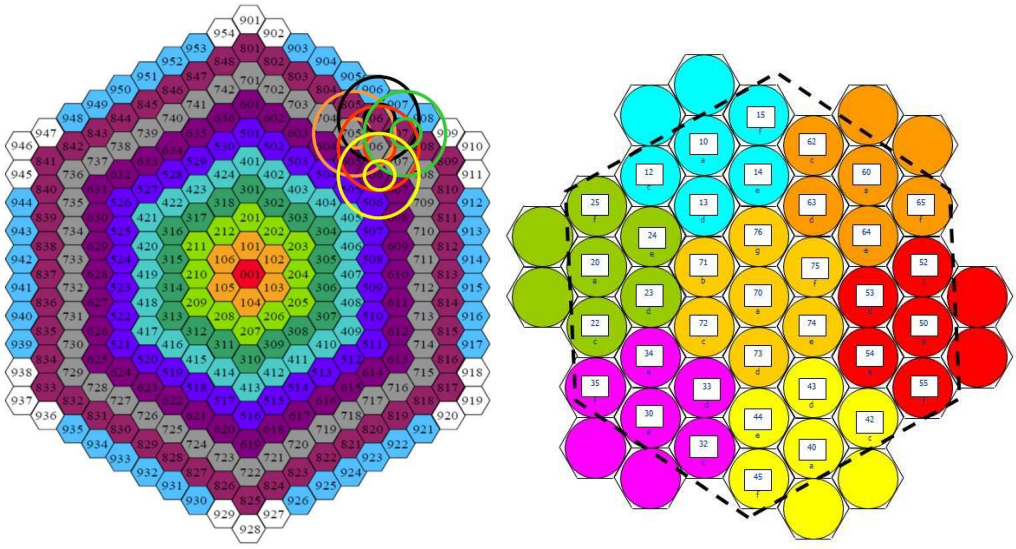

Figure 3: *(left)* Camera of a mid-size CTA telescope. Each hexagon represents a 7-pixel cluster. A "super-cluster" of 37 overlapping pixel regions centered on each cluster provides the L1 trigger. *(right)* Zoom on 37-pixel region.

2.1 L0 trigger

The L0 Mezzanine (piggy back) board (see Fig. 2) accommodates seven very low noise preamplifier circuits. The differential analogue input signal can be AC coupled or DC coupled, depending on the parts mounted. DC-coupling is possible due to the very low input offset voltage of the preamplifier. The advantage is the independence of the signal baseline with respect to the PMT pulse rate. The preamplifier output signal is connected to a LVDS comparator. The discriminator threshold is either controlled by the front-end board FPGA or the L1 trigger board, using an eight channel serial DAC.

2.2 L1 trigger

The L1 trigger is based on the L0-signal processing of overlapping 37 pixel regions (see the scheme in Fig. 3). A single low cost FPGA distributes the L0-signals of a cluster to its 6 surrounding clusters. In parallel, it receives the corresponding signals from the 6 surrounding clusters.

The block scheme of the L1 trigger board is shown in Fig. 4. Its main part is the FPGA, which generates the L1 trigger by processing the L0 signals from the cluster itself and the six surrounding clusters. Their L0 signals are collected by short flat cable connections, seen in Fig. 7. These cable connections are also being used to provide the

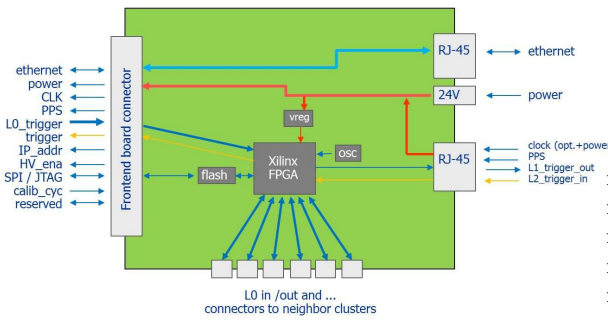

Figure 4: The block scheme of the L1 trigger board

surrounding clusters with the L0 signals from the central cluster. The L0-fanout is one of the FPGA functions.

At the same time, the L1 trigger board is the backplane for the front-end board (Nectar or Dragon board [7, 8]). The connector on the left-hand side provides the front-end board interface.

A gigabit ethernet connection, to be used for the front-end board readout and control is looped through. The same is true for the 24V raw voltage. The L1 trigger board has its own DC-DC voltage regulator (24V to 3V) to keep it independent from the front-end board. The second RJ45 connector, see Fig. 4, right-hand side, carries the common clock and the PPS signal. They are being "refreshed" by the FPGA, before propagating to the front-end board connector. The FPGA-internal PLLs allow to modify the clock according to the front-end board needs. In a special case (PCB mounting option), the clock line (wire pair) can be used in a threefold way, carrying 24V DC, the clock, and the PPS signal. Doing so, only two cables connection per cluster are required. Besides the already mentioned signals, ethernet, power, clock and PPS, the L0 signals from the front-end board and the camera trigger signal to the central cluster are being exchanged.

Finally, it should be mentioned that each L1 trigger board houses its own unique 64-bit ID ROM, to be used by the front-end board Ethernet for the IP address.

After power on, the trigger scheme gets loaded into the FPGA from a serial PROM (Programmable Read Only Memory). However, the trigger scheme can be updated by the front-end board via its Ethernet connection within less than a second.

The trigger fabric, main part of the FPGA firmware, processes 37 L0 signals (see the schemes in Figs. 5,6). Various trigger algorithms can be used. A first revision of the L1 trigger board is based on an Altera FPGA. This FPGA allows the very accurate tuning of its internal delays. It has been demonstrated that a 3 Next Neighbor (3NN) algorithm performs well, when the FPGA runs in an asynchronous mode. More complex algorithms, such as a time distributed trigger, require the FPGA to run in a synchronous mode. The L1 trigger signal can be passed into

three directions. Firstly, to the DAQ FPGA of the front-end board, allowing the initiation of the Analog Pipeline readout. Secondly, the L1 trigger information can be transferred to the central cluster, which hosts a special firmware allowing to distribute the L2 trigger to all clusters. A third way, the use of a separate L2 crate is the preferred one which we describe below in sec. 2.3.

Besides its simplicity and flexibility, the FPGA approach of the digital trigger has another great feature. Each of the 37 L0 signals has to pass its individual delay line before entering the trigger fabric. The second revision of the L1 trigger board, shown in Fig. 7, is based on a Xilinx Spartan 6 FPGA. The individual delays can be adjusted in steps of 50ps. Provided a periodically pulsed central laser diode is available, the FPGA can run an auto calibration cycle, initiated by the front-end board FPGA.

2.3 L2 Crate

The L2 crate with its components, the Cluster Service Board (CSB) and the L2 Controller Board (L2CB), is still in the development phase. It will host 18 CSBs, 1 L2CB and a backplane. The size is about 50x20x20 cm^3. The weight is roughly 11 kg. All boards are powered by the 24V used for powering the 7-pixel clusters. The estimated power consumption is 50 W.

2.3.1 CSB

The CSB controls up to 16 clusters via a single Cat5e cable. It receives the L1 trigger and distributes the following signals to the clusters: clock, PPS, camera trigger. Additionally it allows to power (24V) the cluster board, using the same Cat5e cable. Besides an individual power on/off, the cluster current can be monitored as well. The trigger functionality is defined by the on board Xilinx FPGA. Depending on the cabling, sectors, consisting out of 14 to 16 clusters, could get processed. The simplest function to generate the camera trigger would be a big OR over all incoming L1 trigger. More sophisticated ones are easy to implement. The partial readout of interesting camera regions only, can be organized easily.

2.3.2 L2CB

The L2CB has two interfaces, one pointing outwards from the camera, the other pointing to the inside, establishing the connection to the CSBs. The outside interface has inputs to a central timing unit and an Ethernet port. The Ethernet connection is being used to gather slow control information (e.g. cluster power consumption), for cluster-power switching and for configuring the trigger. Event-number driven time stamps could get transferred via this channel as well. The interface to a timing unit is the connection to a central clock / PPS source. The inside connection, the L2-crate backplane, carries the clock / PPS signals and the camera trigger. Additionally, there is a bidirectional serial communication channel to each CSB for exchanging slow control and trigger-configuration-related data.

3 First Test Results

Although the described system is not yet fully available, first tests did show excellent results. Due to its symmetric structure, the L1 trigger board can be used as a versatile trigger pattern generator. This way, the proper functionality of the 3NN algorithm for a complete 49-pixel area has been demonstrated. A first version of an asynchronous FPGA design, based on the 3NN trigger algorithm, did show excellent results. For any three (of 49) connected pixels (e.g., see Fig. 8), the coincidence of L0 signals for a time period down to 1 ns has been found to be sufficient to get a L1 trigger. Furthermore, an integrated test, based on a mini camera (3 cluster, Dragon boards + L0 boards by R. Paoletti [8]) took place, see Fig. 9. In this case the L1 trigger board was directly triggering the readout of the front-end board. The gathered waveforms did prove the proper functionality of the L1 boards.

4 Outlook

Both, for the L0 and the L1 trigger, second versions have been built. From the hardware point of view this is enough to build a fully functional camera trigger. Still, the addition of a L2-crate could make the camera trigger generation easier, reduce the trigger latency and allow to combine it with the power and clock / PPS distribution. The FPGA-based L1 trigger allows the implementation of various innovative trigger algorithms. Very first tests are encouraging. Integration tests are planned for the Nectar and the Dragon boards [7, 8] by the end of 2013.

Acknowledgment: We gratefully acknowledge financial support from the agencies and organisations listed in this page: http://www.cta-observatory.org/?q=node/22.

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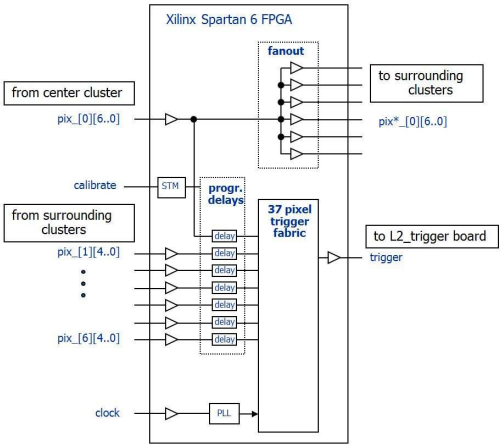

Figure 5: FPGA block scheme

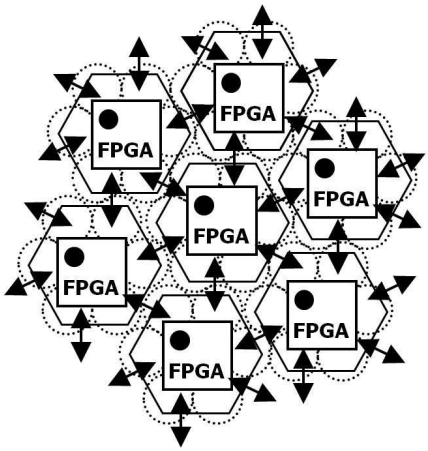

Figure 6: FPGA interconnection scheme

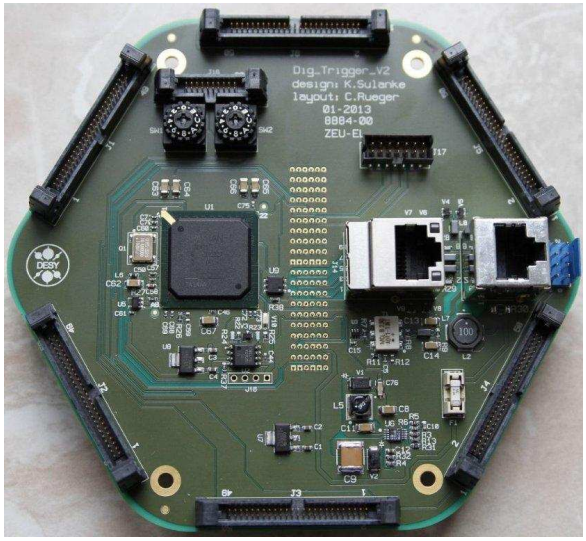

Figure 7: L1-board, the Digital Trigger Backplane, Rev. 2.

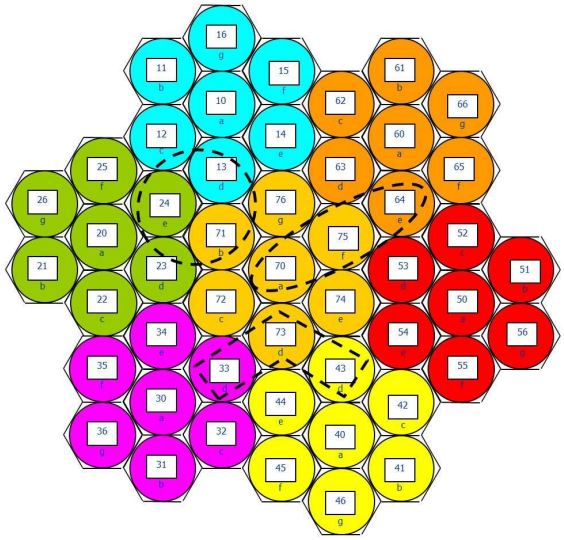

Figure 8: 3NN example, 3 of about 500 possible combinations shown

Figure 9: Dragon-Cam Japan, consisting of 3 clusters, with L1 boards (Rev. 1) plugged