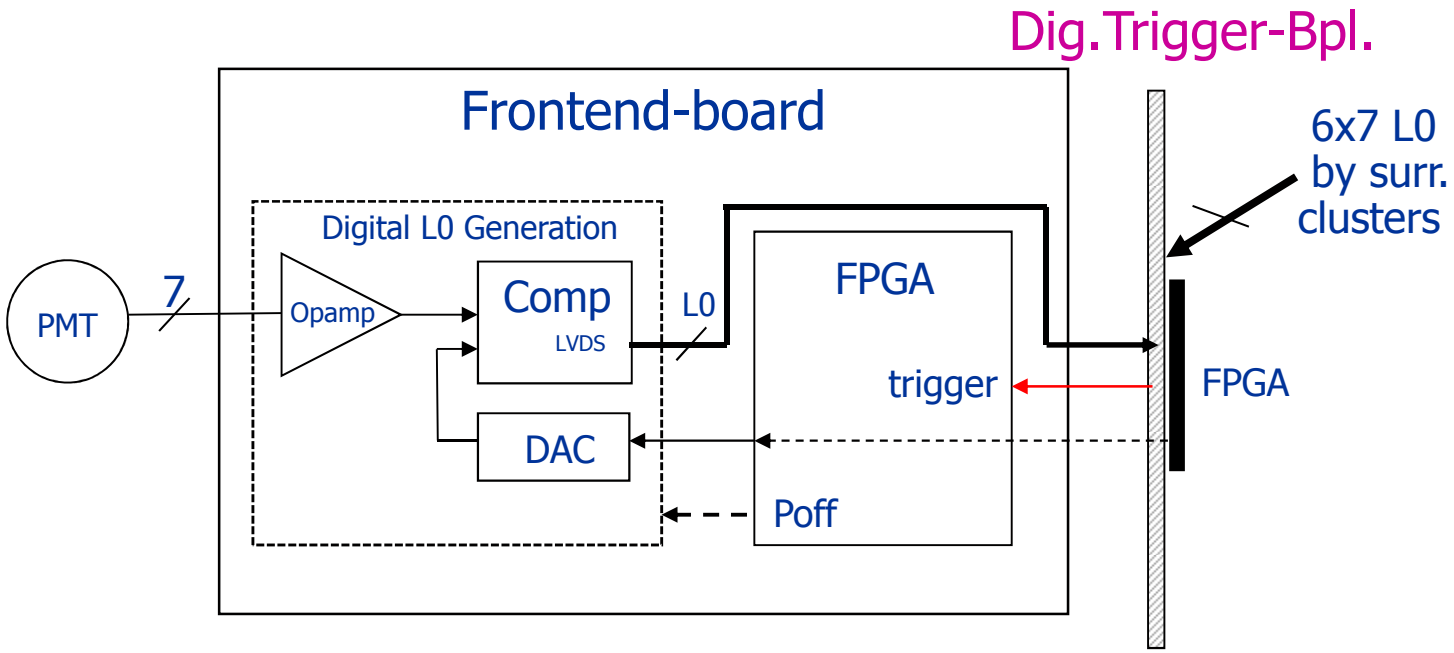
Digital L0 bypassing Frontend-Board FPGA

- Length matched Dig. L0 signals NOT connected to the frontend-board-FPGA
- Trigger threshold DAC control by trigger FPGA, optional



Digital L0 through Frontend-Board FPGA

- Allows Frontend-board-FPGA with scaler
- uniform FPGA internal delay (by constraints) preferred
- Trigger threshold DAC control by trigger FPGA, optional
- Separate power island with software controllable shutdown