Digital Trigger, Coca-Aspects & Status

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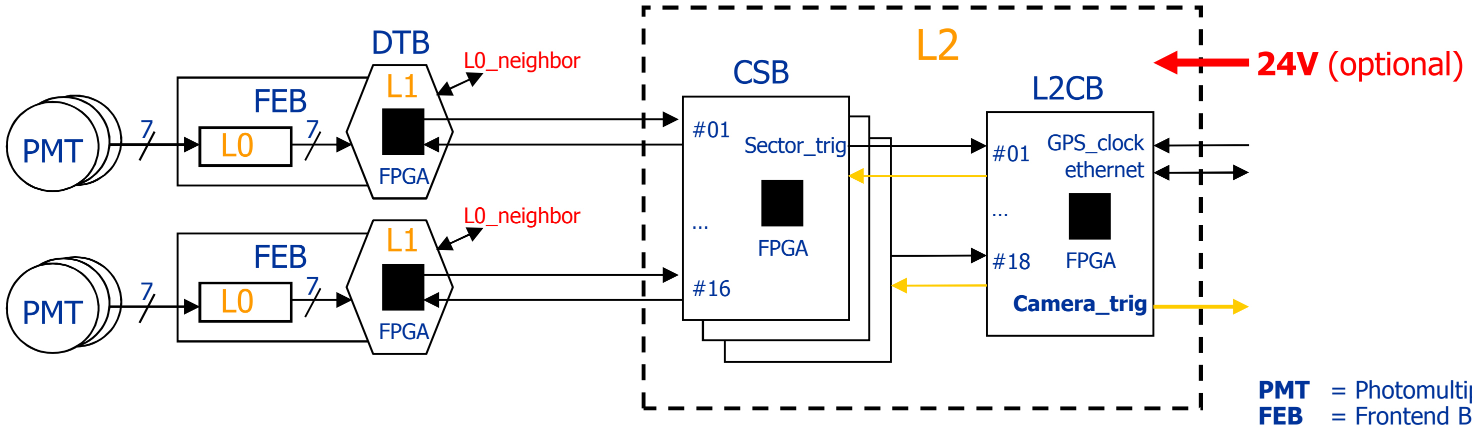
DESY

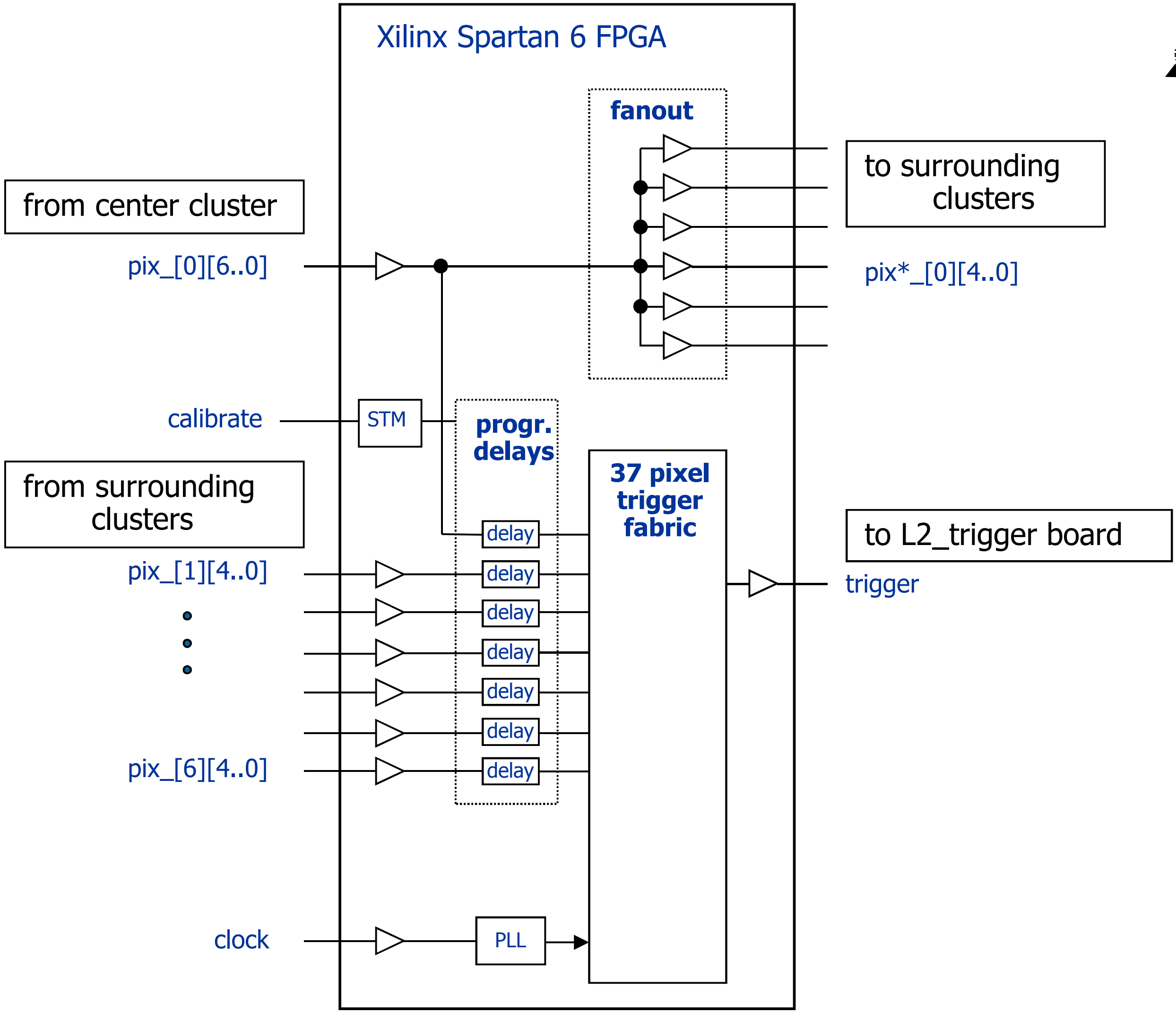
The Digital Trigger Scheme

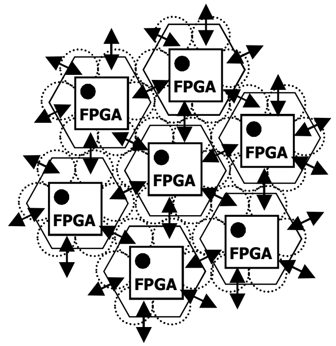


PMT = Photomultiplier Tube
FEB = Frontend Board
DTB = Digital Trigger Backplane
CSB = Cluster Service Board
L2CB = L2 Controller Board

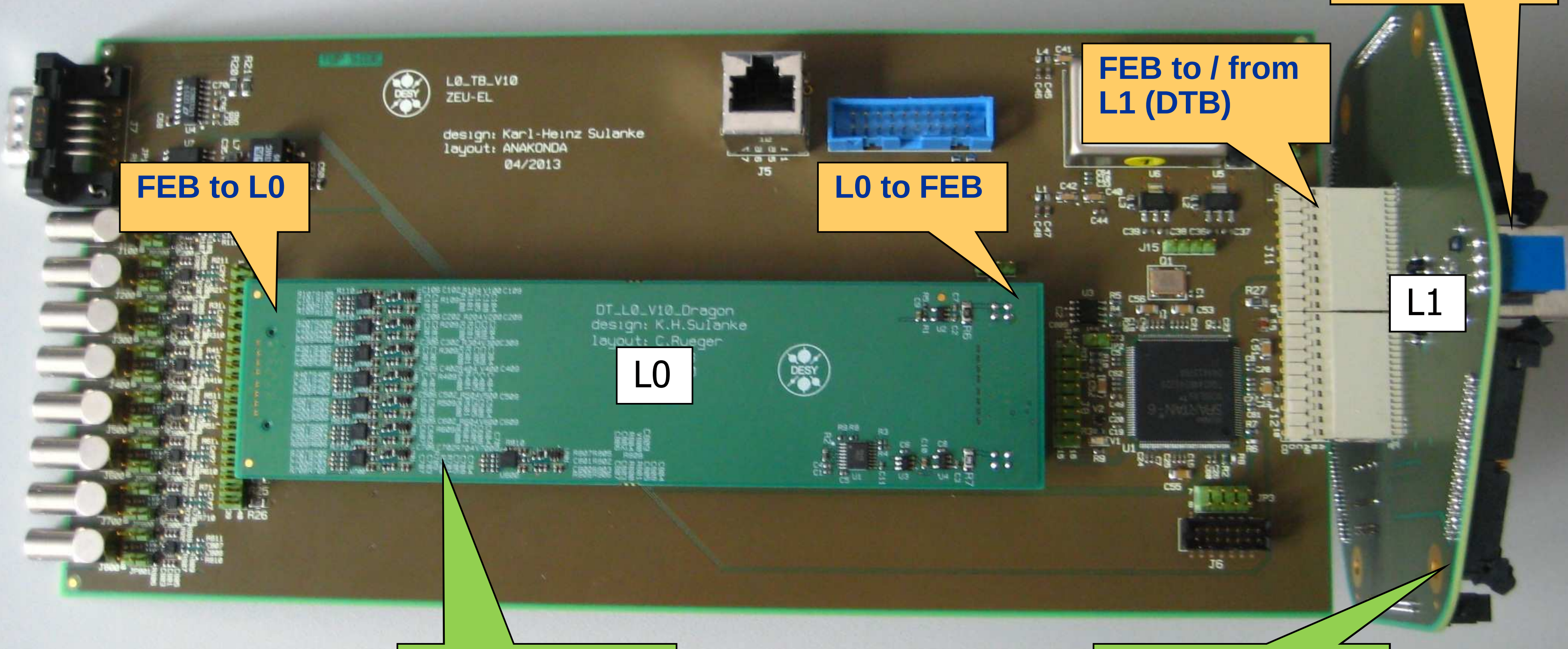
- L0, 7 pixel, mezzanine board, very low noise preamp + comparator + DAC
- L1, 37 pixel, Digital Trigger backplane, based on Xilinx-Spartan 6 FPGAs
- L2, is a crate, ~ 50 x 20 x 20 cm, ~ 11 kg
  - 18 x CSB (Cluster Service Board)
  - 1 x L2CB (L2 Controller Board)
    - Ethernet interface
    - Optical / electrical camera trigger output

L1, DTB-FPGA's Functionality





Electrical and Mechanical Interfaces



CoCa … Interface Definitions

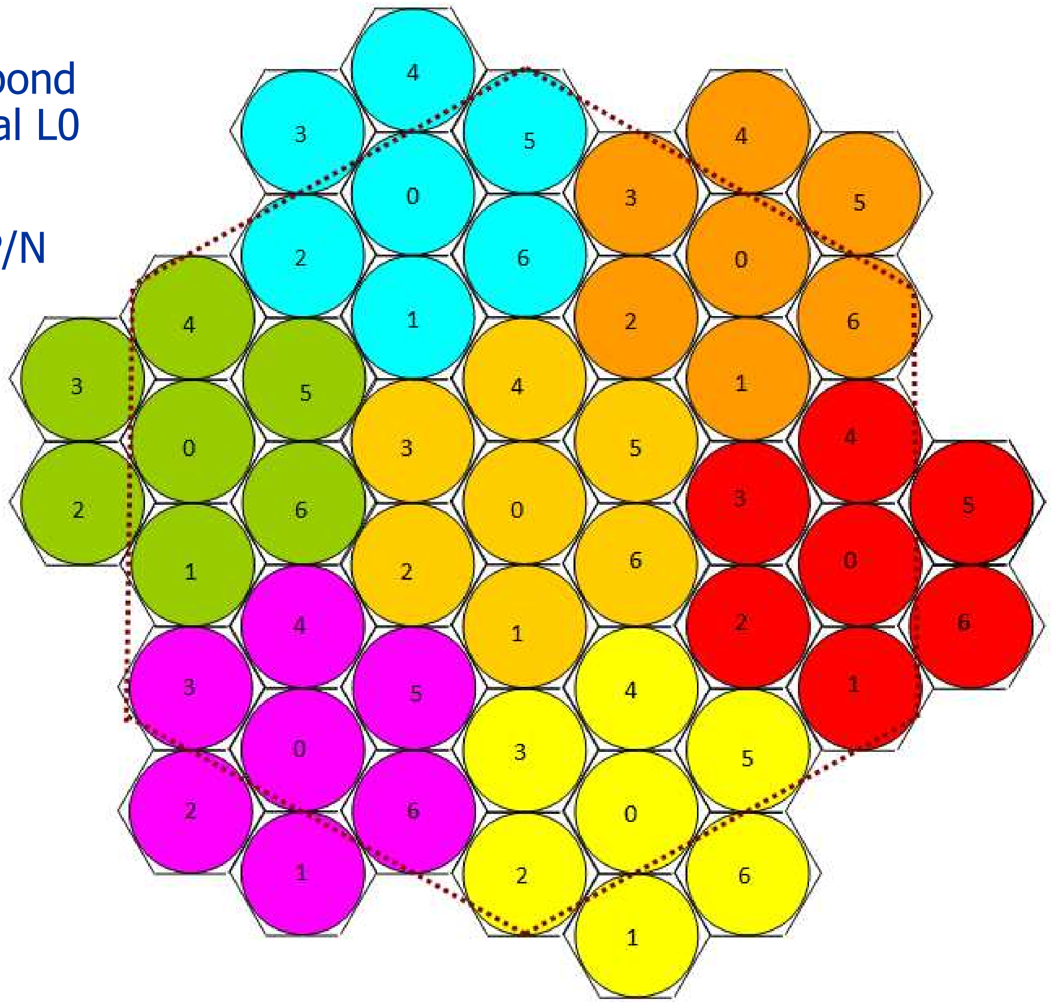
- Focal plane, pixel – Id mapping within the cluster, **defined ?**
  - essential for trigger firmware designs
- L0 (Mezzanine board)
  - Mechanical defined, but two versions, Nectar and Dragon, ☹
  - Electrical / logical (SPI) √
- L1 (Digital Trigger Backplane)
  - mechanical √ , but rev. 2 not up to date with the latest FEB conn. angle
  - electrical (power, digital signals) to FEB √
  - electrical to outside (power, ethernet, clock, PPS, L2) √
- L2 (for the digital trigger only)
  - Still in the design phase
  - Will match the interface definitions for the FEB backplane and the TIB (Trigger Interface Board)

Focal Plane, Pixel-ID Mapping

Shown Pixel-IDs do correspond to the **FEB interface** digital L0 signal definition

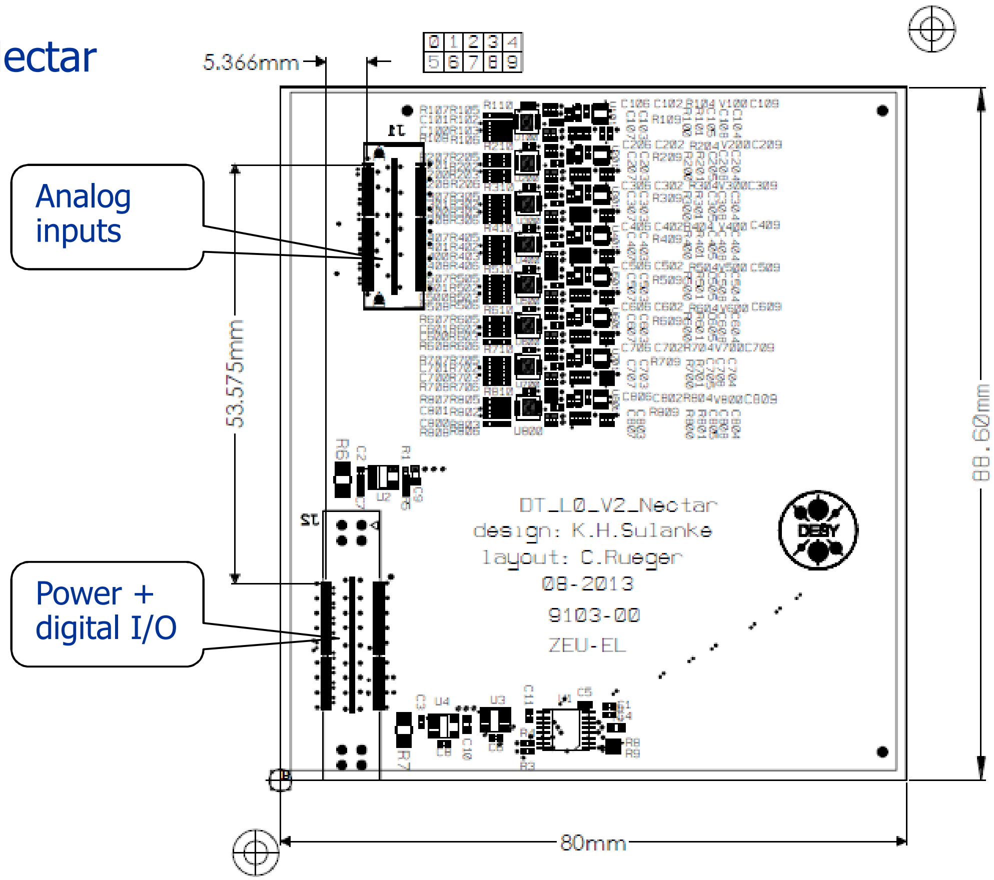
DIG_TRG_OUT0..6_P/N

?



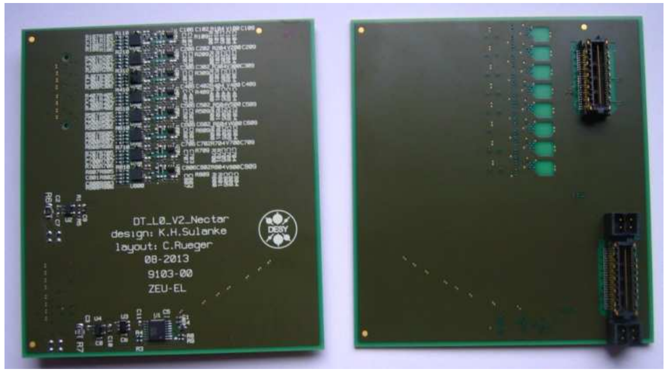
L0, e.g. the mechanical interface

- DT_L0_Nectar



L0 Mezzanine Boards

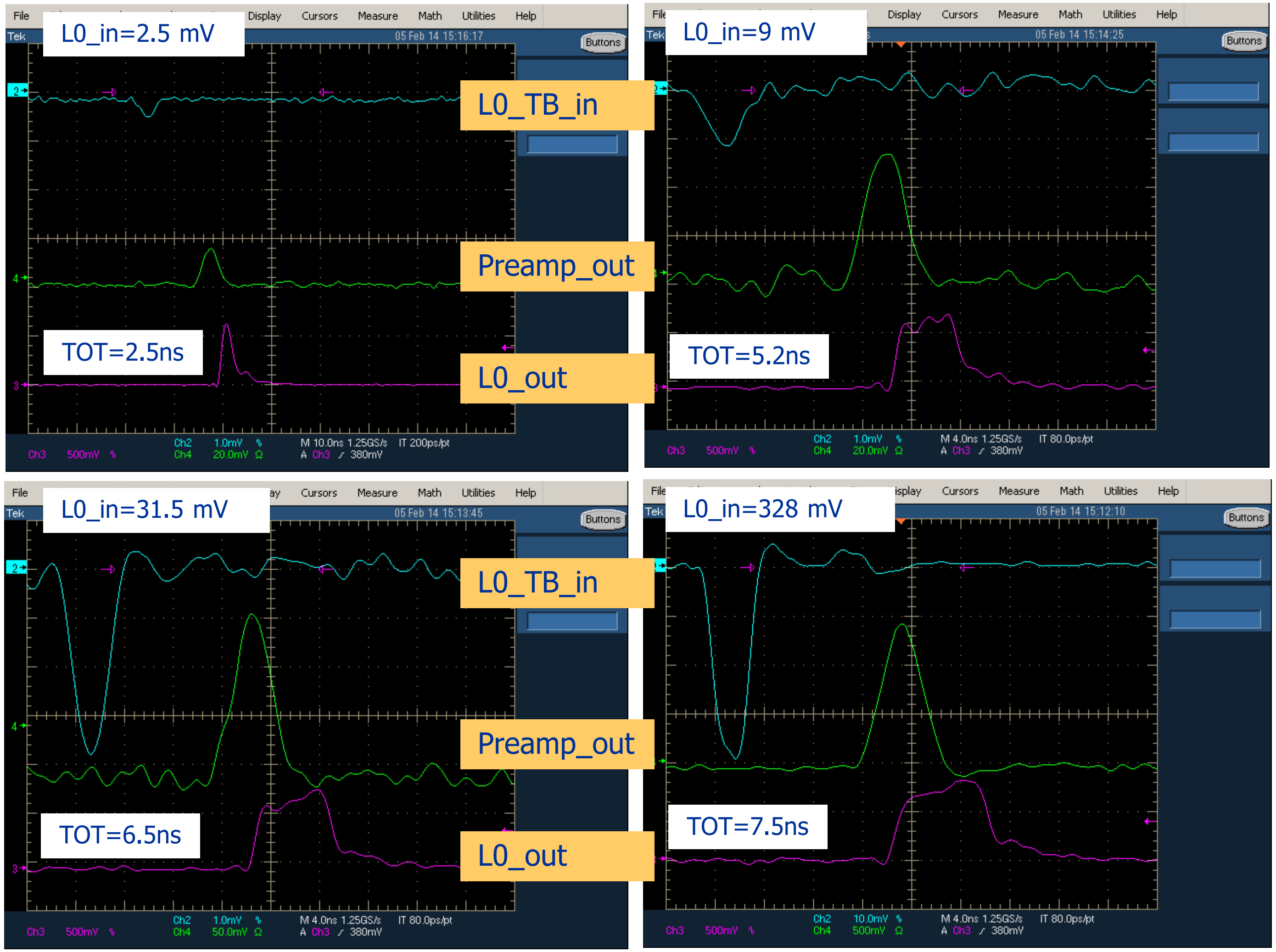
- Nectar-L0



- Dragon-L0s

Improved L0, TOT with 12 mV Threshold

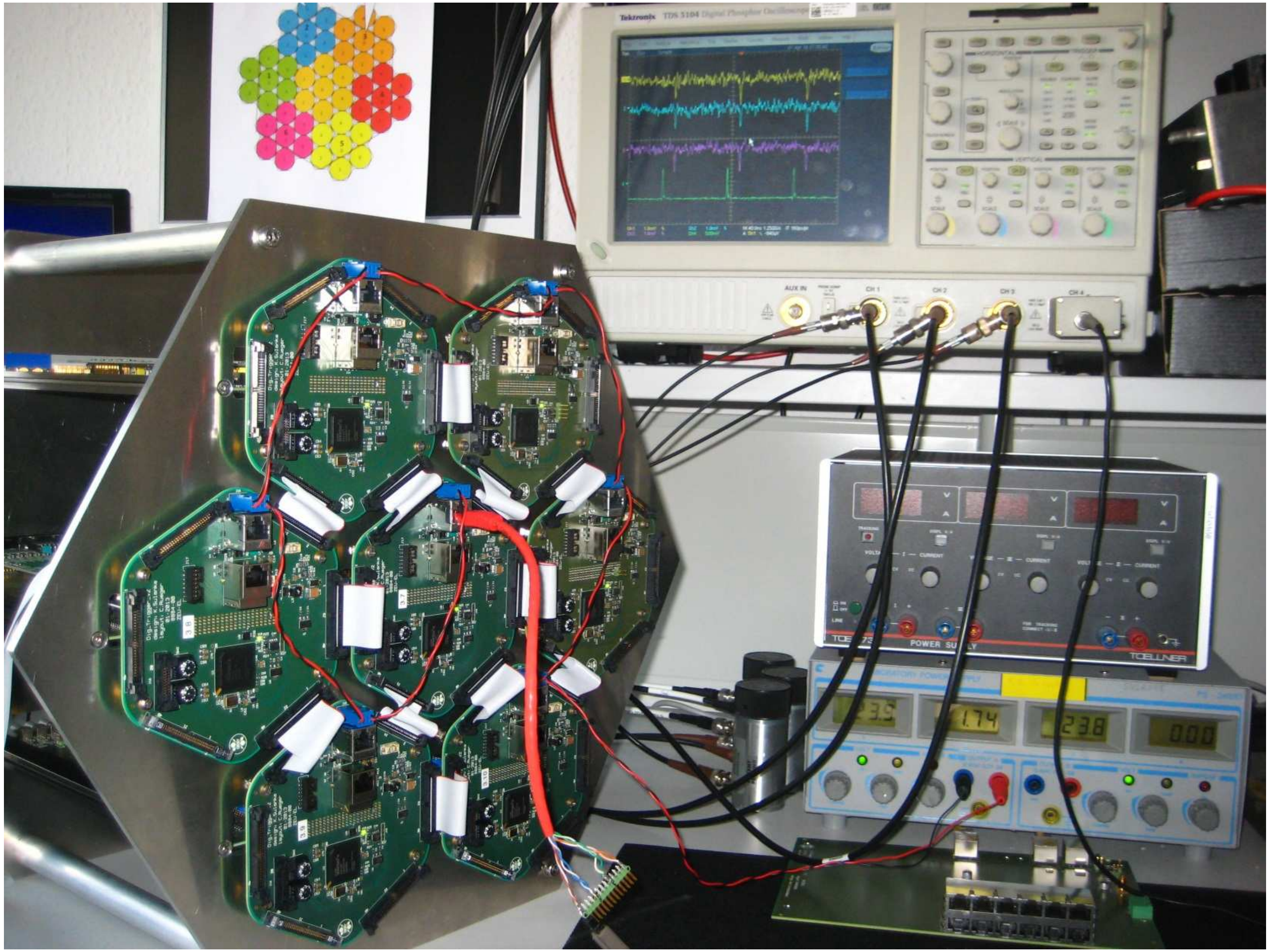
- Measurements done, using the L0 Testboard (TB_gain = 8.3, L0_gain = 6.1)



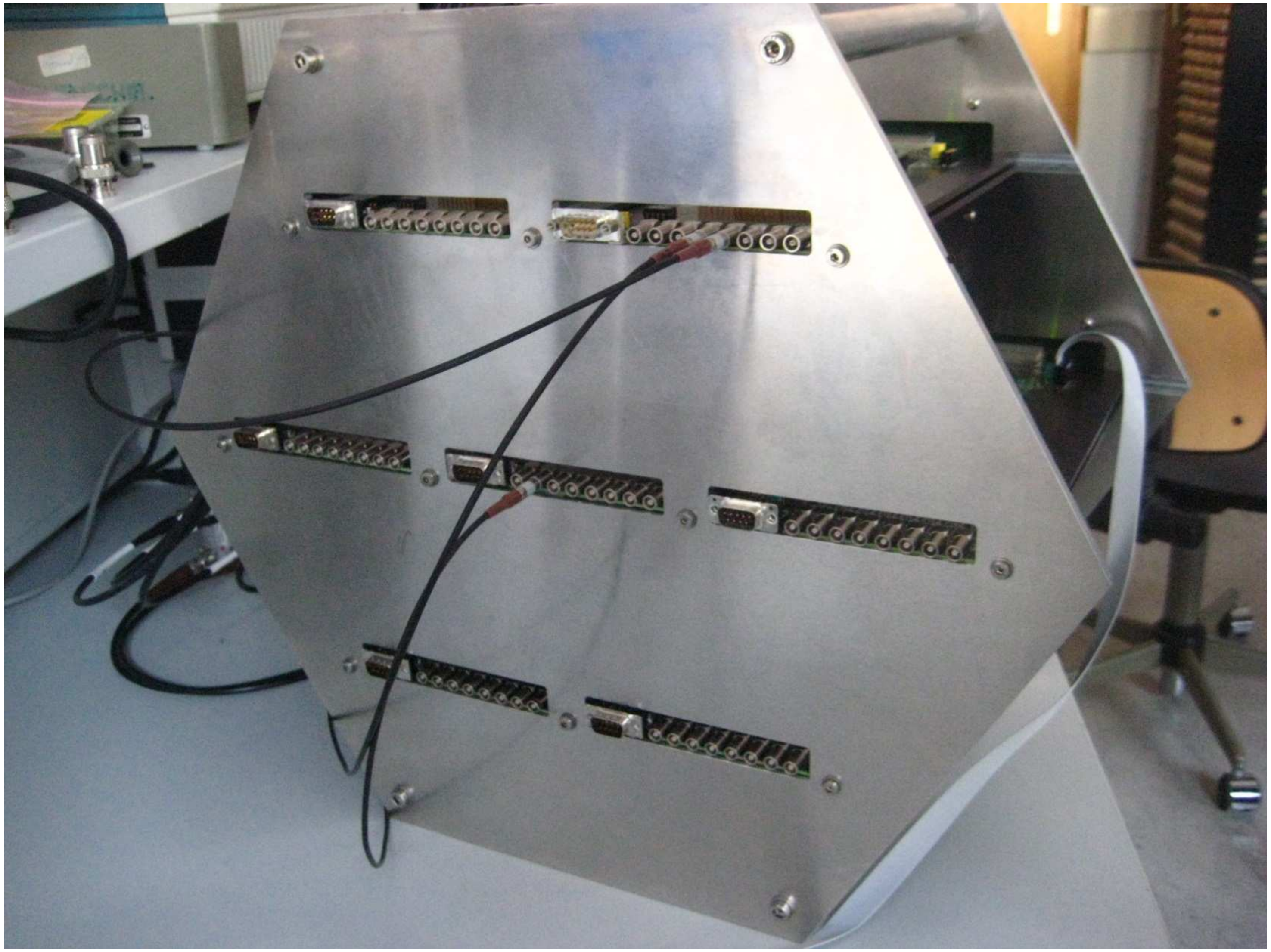
3NN Trigger Firmware Revision 002

- 3NN of 37 pixel (Rev 001 bug fixed)
- synchronous design, runs from local oscillator (25 Mhz)
- Firmware automatically detects missing neighbor clusters
- „plug and play“ version
- Sampling rate **950 Mhz**
- L1 pulse shaped , 2.1 ns length
- Trigger latency ~100 ns
- Trigger time resolution 1.05 ns
- Trigger jitter +/- 1.05 ns
- Test setup with 7 connected clusters
  - all 3NN combinations checked using PMT like signals (> 0.5 mV pk) and a gain of 48 (testboard_gain * L0_gain)
  - global clock tested as well, using Axel Kretzschmann clock fanout (rev. 1)

Digital Trigger Test Setup at DESY

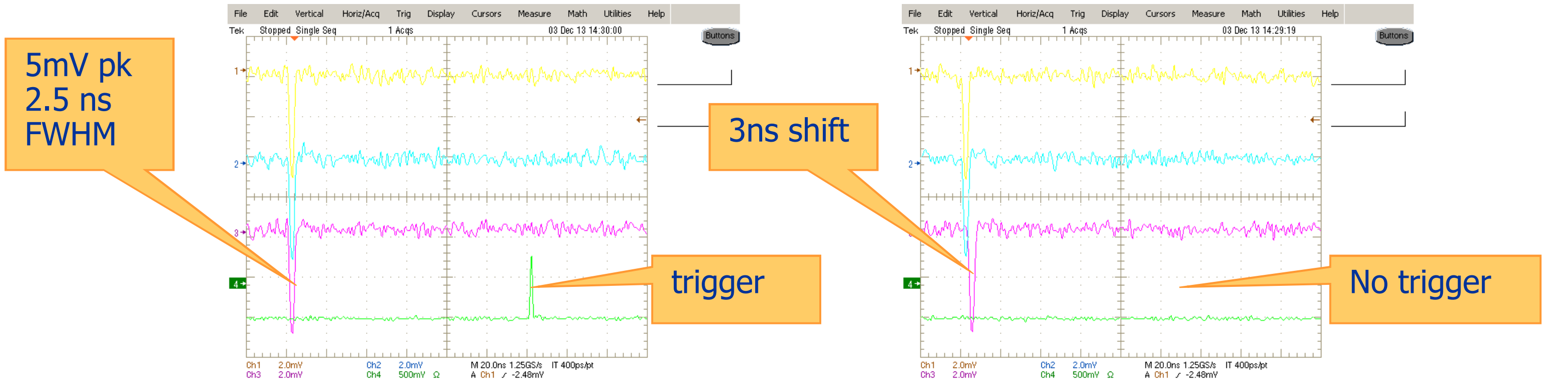


Digital Trigger Test Setup, Back Side

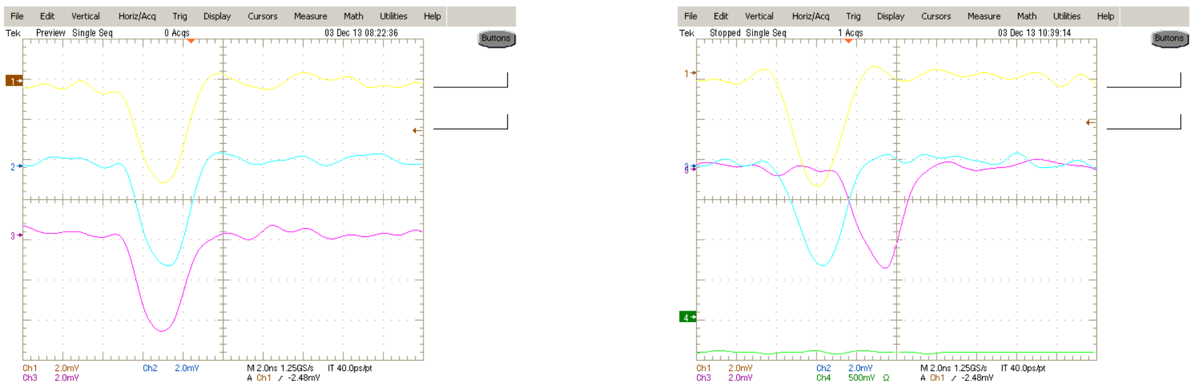


3NN Trigger Test Results

- 100% trigger and 0% trigger situation



- Analog input signals, zoomed time scale



L0, L1, L2 Production Status

- 10 more DTBs produced and successfully tested
- 16 DTBs available now and partly distributed already
- NectarCam, Saclay, almost ready for the next test setup (5 modules)
  - 5 additional DTBs and 2 L0s are in place
  - 3 other L0s will be reworked (adapting resistors) this week
- DragonCam, Japan
  - 3 DTBs and 3 L0s in place
- Digital trigger test setup at DESY extended
  - 7 x Testboard + L0 + L1 (DTB)
- Dig_trigger_v3 with corrected FEB connector angle expected in 2014-09
- L2 stage (including clock distribution) still in the schematic design phase
  - available in 2014-08
  - Intermediate solution by Axel Kretzschmann, to be tested this week

Summary and Outlook

- A 7 cluster test setup has been installed, to be used with real signals
  - L0 performance improved after changing gain setting resistors
  - L0 and L1 are functional after power on w/o software interaction
  - Noise floor of about 0.3 mV pk measured (testboard input)
    - Corresponds to 2.4 mV diff. L0 input
- Integration tests (NectarCam, DragonCam) are ongoing
- Combination L0-ASIC (analog trigger) + DTB still needs to be tested
  - L0-ASIC mezzanine for testing would be great
- More trigger firmware developments planned:
  - E.g. trying the time gradient trigger
- L2-stage and DTB_rev3 with new FEB connector angle in 2014-09