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## Digital Trigger, Topology, Connectors and Cables, Rev.1

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List of Abbreviations			
SPI	Serial Peripheral Interface	TIB	Trigger Interface Board
L2CB	L2 Controller Board	DTB	Digital Trigger Backplane
CTDB	Clock & Trigger Distribution Board	FEB	Frontend Board
L2BP	L2 Backplane	PMT	Photomultiplier Tube
LVDS	Low Voltage Digital Signalling	TOT	Time Over Threshold
L1A	L1 Accept	FPGA	Field Programmable Gate Array
TH	Through Hole	ATB	Analog Trigger Backplane


History		
Version	Date	Observation
1	24/10/2016	Draft

Distribution
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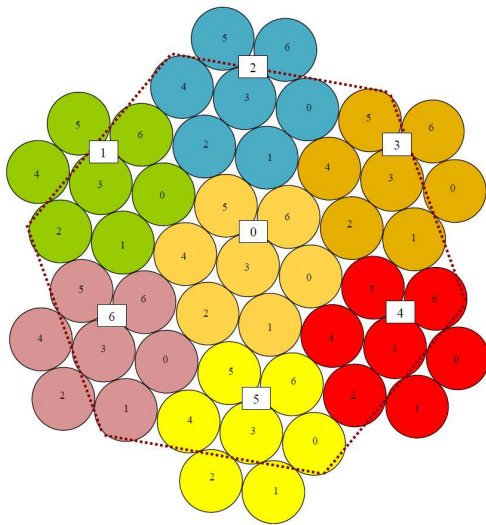
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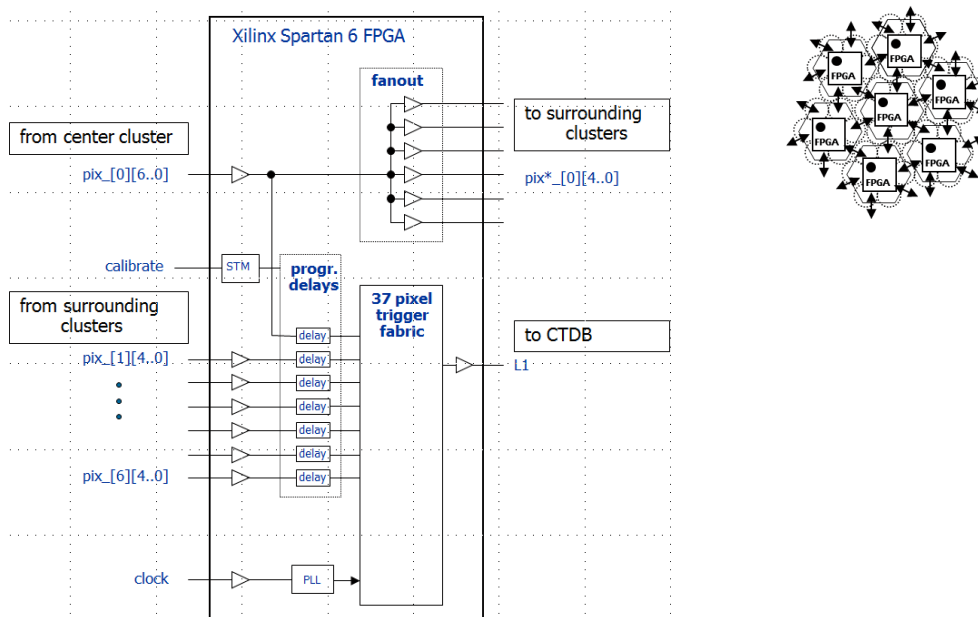
## 1 Trigger Topology

On the FEB PMT signals are being discriminated by the L0 – ASIC. The gained L0 (TOT LVDS) signals are passed to the DTB's FPGA. The FPGA distributes these signals to its surrounding six neighbor DTBs. In parallel it receives their L0 signals. This way each FPGA has access to an overlapping hexagonal shaped 37 pixel area, see Fig. 1 .




**Figure 1:** The 37 Pixel Area

See Fig. 2, the DTBs FPGA generates the L1 trigger signal by processing 37 L0 signals.

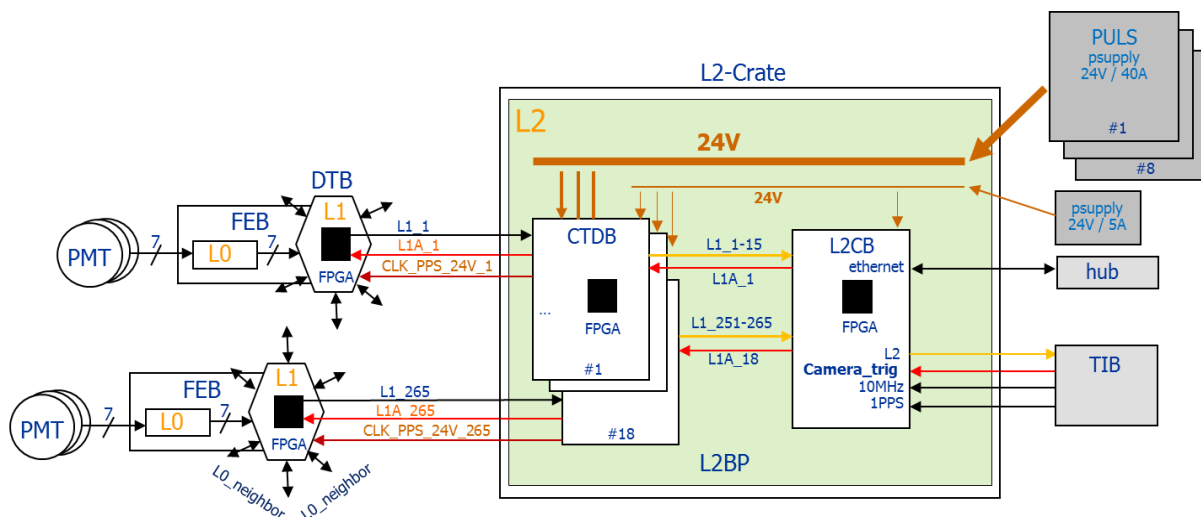


**Figure 2:** The DTB-FPGAs functionality

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Not shown in Fig. 2 is a SPI bus connection to the FEB. It allows to access DTB registers, e.g. to adjust delays of the 1PPS signal, the L0 signals or the L1A trigger.

Each of the DTBs is connected to a CTDB via a standard Cat6a patch cable, 3m in length. This cable carries five signals, the L1, L1A, a common clock, a common 1PPS and the FEB-BUSY (not shown in Fig. 2). Optional it can also be used for the 24V power connection. 265 L1 signals are being passed to the L2CB via the L2BP. All signal paths within the L2BP are of the same length (+/- 5 mm). Presently the FPGA of the L2CB performs simply an OR over the incoming L1 trigger signals to generate the L2 trigger. More sophisticated L2 trigger algorithms could be implemented, because all L1 signals are concentrated in a powerful FPGA. The L2 trigger signal is passed to the TIB. In case the L2 trigger is accepted, the TIB sends a camera trigger back to the L2CB, where it is distributed to the 18 CTDBs. Each of the CTDBs can provide up to 15 DTBs with their appropriate signals. Besides the L2CB, the L2 crate houses 18 CTDBs.




**Figure 3:** Digital Trigger Topology

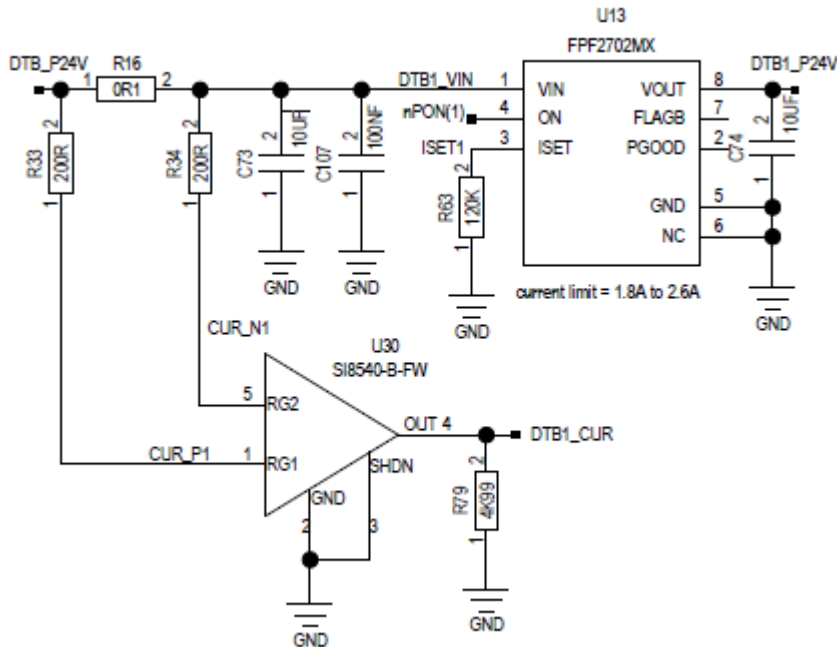
## 2 Power Distribution via L2-Crate (optional)

Optional, the L2-Crate can be used to distribute the power to the FEBs via the CTDBs. Separately mounted copper rails on the L2BP are able to carry the overall current. The PULS power supplies, providing up to 40A each, can be connected to the copper rails in parallel. The return (GND) path is either the camera chassis (preferred way) or the shield of the Cat6a cables, used for the CTDB to DTB connection.

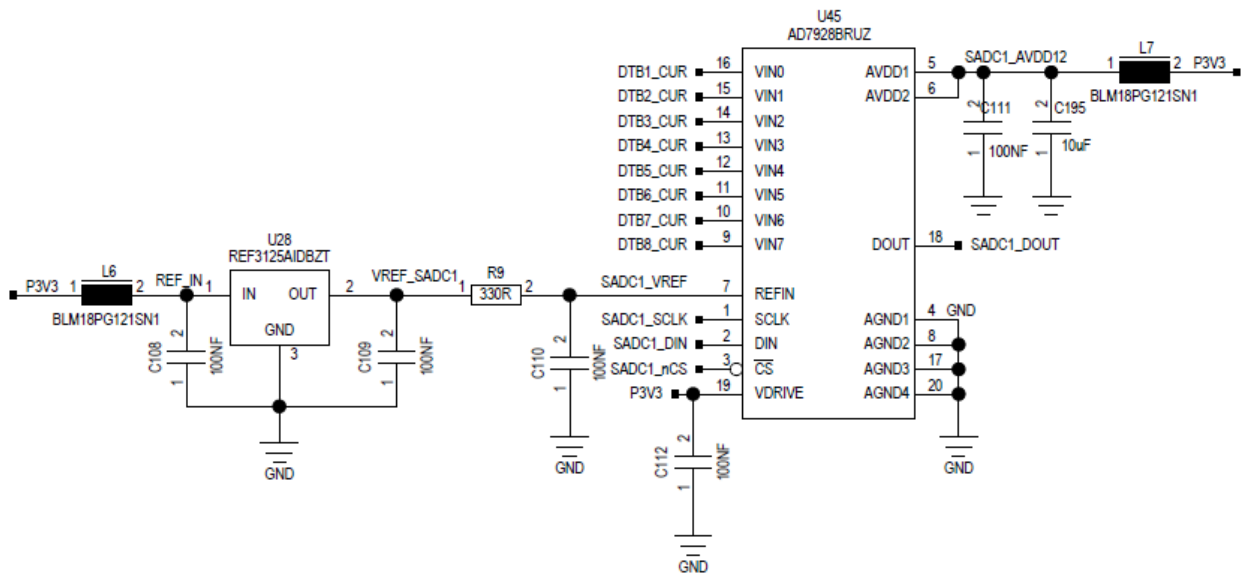
It is recommended to power the CTDBs and the L2CB itself by a separate small power supply, being powered up in advance, e.g. 30 seconds before the main (PULS) power supplies. This way all L2-FPGAs are loaded already, providing a defined start up condition.

Figure 4 shows one of the 15 power switch circuits, located on the CTDB. The FPF2702 has a lot of nice features, like adjustable over current protection (R63), thermal shutdown, blanking time (to deal with power on spikes), etc. . The current sensing resistor R16 is used together with an ADC (Fig. 5) to continuously monitor the FEB current. A CTDBs FPGA firmware fuse will be implemented. Current readout and current limits will be set by the L2CB via Ethernet and SPI (L2BP).


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**Figure 4:** CTDB, integrated power switch and current sensing



**Figure 5:** CTDB, one of two ADCs, used for the FEBs current measurement

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### 3 From DTB to L2CB, Cables and Connectors

#### DTB

Item	from	to	RefDes	Manufacturer-Id	Remark
FEB connector	FEB	DTB	J11,J12	<a href="#">TE 6469025-1</a>	same like for ATB
Ethernet conn.	DTB	FEB	J14	<a href="#">TE 1840417</a>	vertical
clock, trigger & power conn.	CTDB	DTB	J13	<a href="#">Molex 85508-5001</a>	vertical, 1.5A / pin
Cat6a cable, 3m	CTDB	DTB		<a href="#">PP6.030.GE</a>	Twisted-Pair-Cable, S/FTP PIMF, 4x2xAWG26/7 (7 x 0,160 mm) Cu, <u>~3.2A per wire pair</u> , final decision about the cable type not yet taken
L0 fanout / reception	DTB	DTB	J1,J2,J3, J4,J5,J6	<a href="#">Harwin M50-3552542</a>	vertical, TH, 50 way
L0 exchange cabling	DTB	DTB		<a href="#">3M 3754</a>	flat cable, 50 way,
L0 cable conn.	DTB	DTB		<a href="#">Harwin M50-3301042</a>	

#### CTDB

Item	from	to	RefDes	Manufacturer-Id	Remark
clock, trigger & FEB power conn.	CTDB	DTB	J8, J9	<a href="#">Harting</a> <a href="#">09 45 551 1126</a>	horizontal, 6 ports, 1.5A
clock, trigger & FEB power conn.	CTDB	DTB	J10	<a href="#">Harting</a> <a href="#">09 45 551 1123</a>	horizontal, 3 ports, 1.5A
24V power connector	L2BP	CTDB	J2	<a href="#">TE 5-5223961-1</a>	16A / contact -> 48A
clock, trigger, SPI, local 24V	L2BP	CTDB	J1	<a href="#">TE-6469028</a>	

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## L2CB

Item	from	to	RefDes	Manufacturer-Id	Remark
clock, 1PPS & trigger conn.	L2CB	CTDB	J23,J24	<a href="#">TE-6469081-1</a>	
L1 trigger conn., local power	CTDB L2BP	L2CB	J19..22	<a href="#">TE-5646488-1</a>	
RJ45 hor.	L2CB	TIB	J14,J15	<a href="#">Stewart SS6488S-NF</a>	10MHz, 1PPS reception from TIB, trigger / busy exchange

## L2BP

Item	from	to	RefDes	Manufacturer-Id	Remark
24V power connector	L2BP	CTDB	J117, J118,..	<a href="#">TE 5-5223955-2</a>	vert., 16A / contact -> 48A
M4 power tap 10 pin pressfit	L2BP	CTDB	J135, J136...	<a href="#">ERNI 214782</a>	IEC60512 test 5b, 40A @ 20°C, 24A @ 70°C
clock, trigger, SPI, local 24V	L2BP	CTDB	J1..J9, J13.J21	<a href="#">TE 6469025-1</a>	vert. header, 2x2+2 rows, pressfit
clock, PPS, trigger, SPI	L2CB	CTDB	J113, J114	<a href="#">TE 6469083-1</a>	vert. header, 3 rows, pressfit
clock, trigger, SPI, local 24V	L2CB	CTDB	J111,J112, J115,J116	<a href="#">TE 5646532-1</a>	vert. header 5 rows, pressfit
busbar 20x10 copper	L2BP	CTDB		<a href="#">Rittal SV 3585.005</a>	DIN 43 671, 428A DC