Digital Camera Trigger for the NectarCam CTA

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Kalle Sulanke

DESY Zeuthen

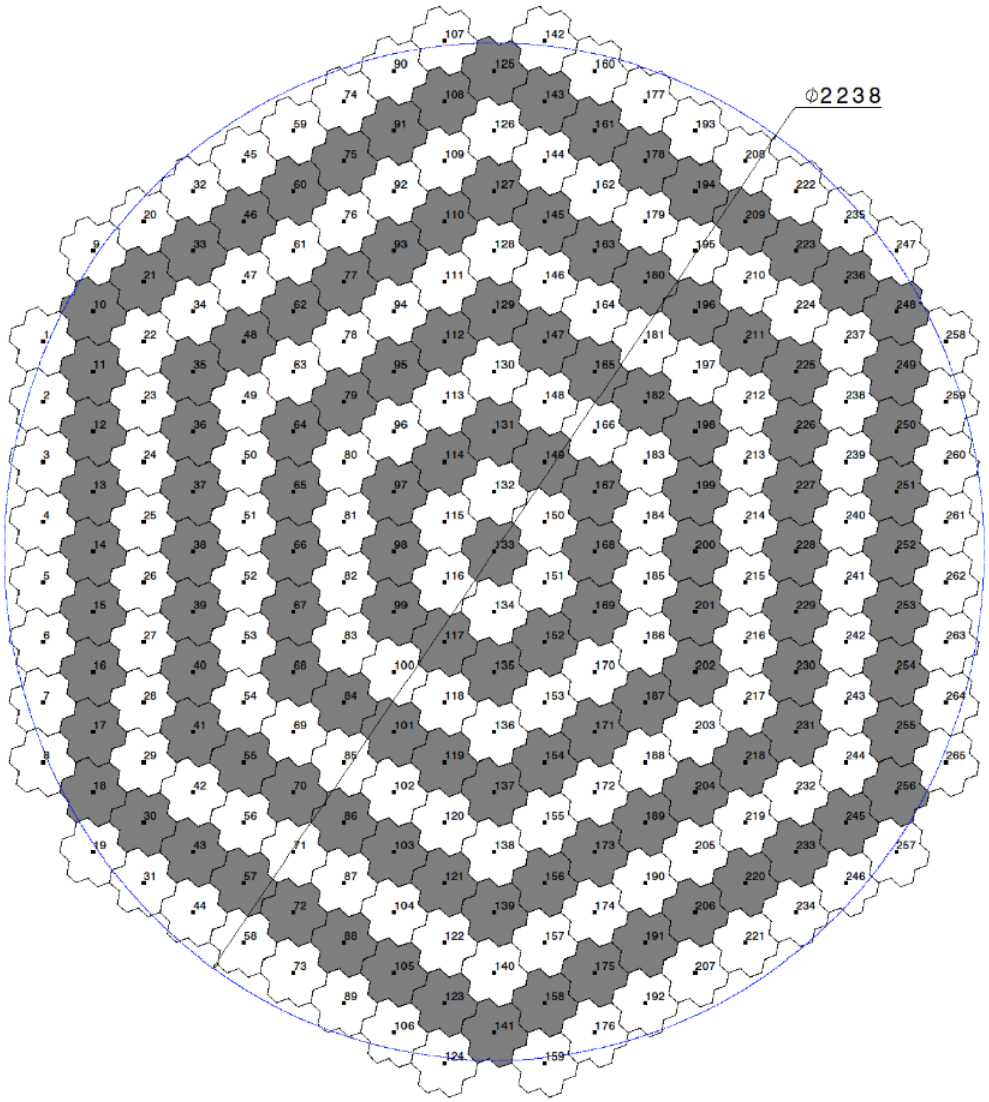
Contents

- NectarCam
- trigger down select
- the trigger schema
- hardware
- firmware
- calibration
- testing
- outlook

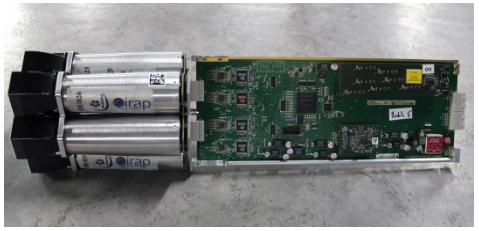
The MST Camera “NectarCam”

- PMT based, 265 cluster a´ 7 PMTs , 1855 Pixel
- PMT-d : 38 mm (1.5 Zoll, z.B. Hamamatsu PMT R11920-100)
- Pixel-grid : 50 mm by Winston cones
- Size of the pixel-array : ~ 3.8 qm
- Weight : up to 2000 kg

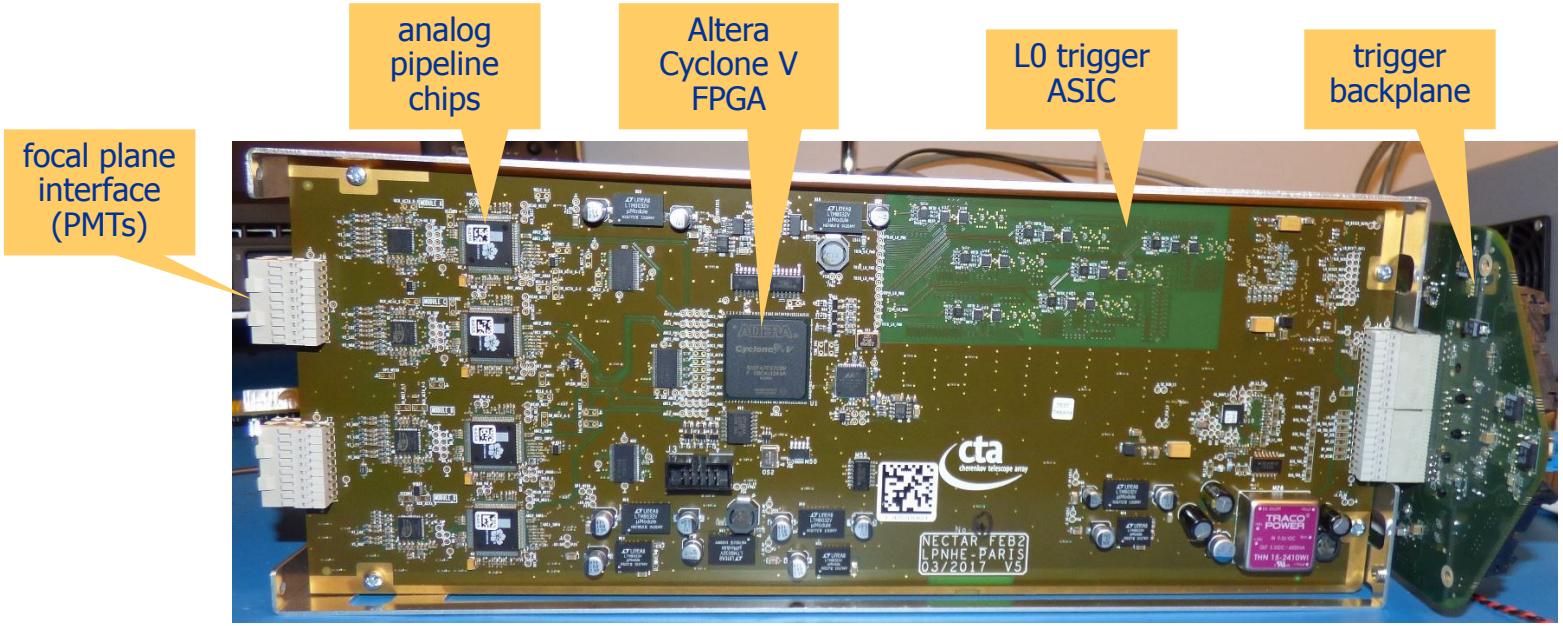
Focal Plane, 265 Cluster, 1855 Pixel



NectarCam Frontend Board



- design by Patrick Nayman & colleagues, LPNHE Paris
  - based on custom analog pipeline chips „Nectar"
- trigger options, analog (sum trigger, Spain) or digital (DESY)



Trigger down select

- parallel development of two trigger systems for years, analog and digital trigger
- analog trigger, designed by Spanish colleagues
  - based on analog sums of up to 21 pixel
  - theoretically better for weak and noisy signals (LST)
  - custom ASICs
  - less cabling, but sophisticated calibration procedures needed
  - will be used at LST

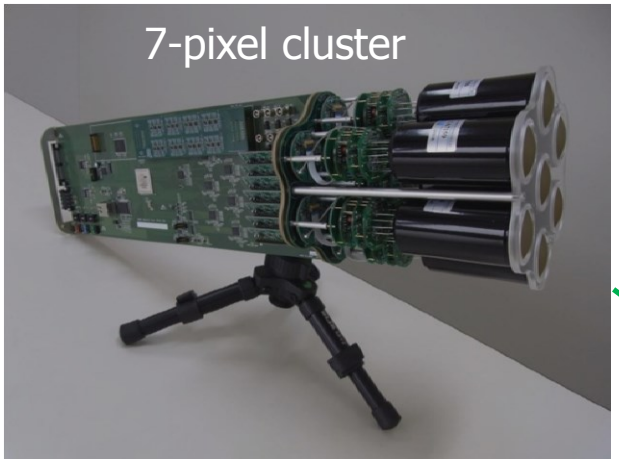
Trigger down select, cont.

- digital trigger
  - based on processing of TOT (timer over threshold) signals by a FPGA (Field Programmable Gate Array)
  - flexible, trigger alghorithm programmable
  - all parts are off the shelf
  - turnkey operation
  - includes individul FEB (frontend board) power management
  - **finally chosen for MST - NectarCam**

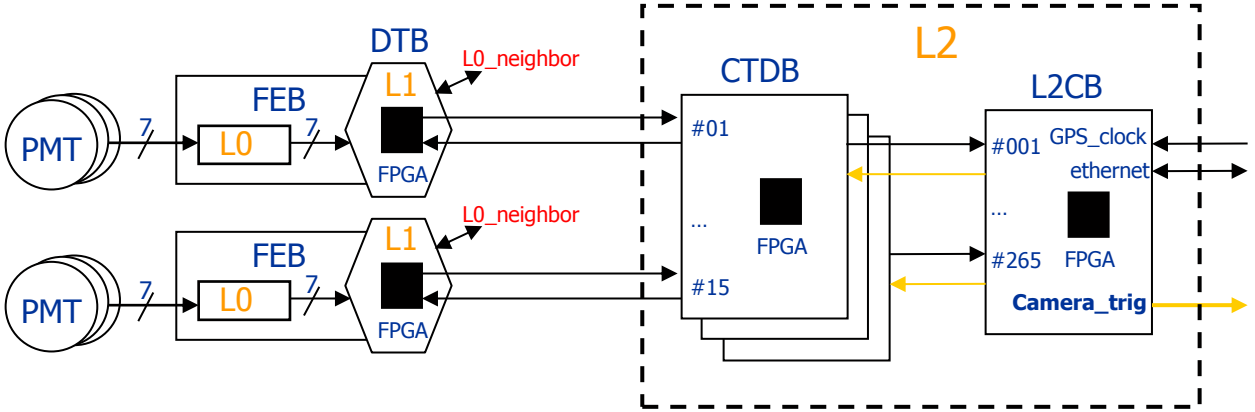
Main Features of the DT System

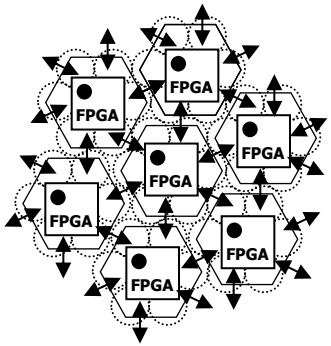
- generating camera triggers
  - processing overlapping 37 pixel areas
  - programmable trigger alghorithm
  - 1ns time resolution
- 1PPS distribution, fanout 1 to 265
  - time stamping in the FEBs
- clock distribution, fanout 1 to 265
  - not used by the NectarCam FEBs, (for some strange reason)
- FEB-busy propagation
- power distribution
  - individual FEBs power on / off cycling
  - current monitoring

37 Pixel Trigger Region



The Trigger Schema

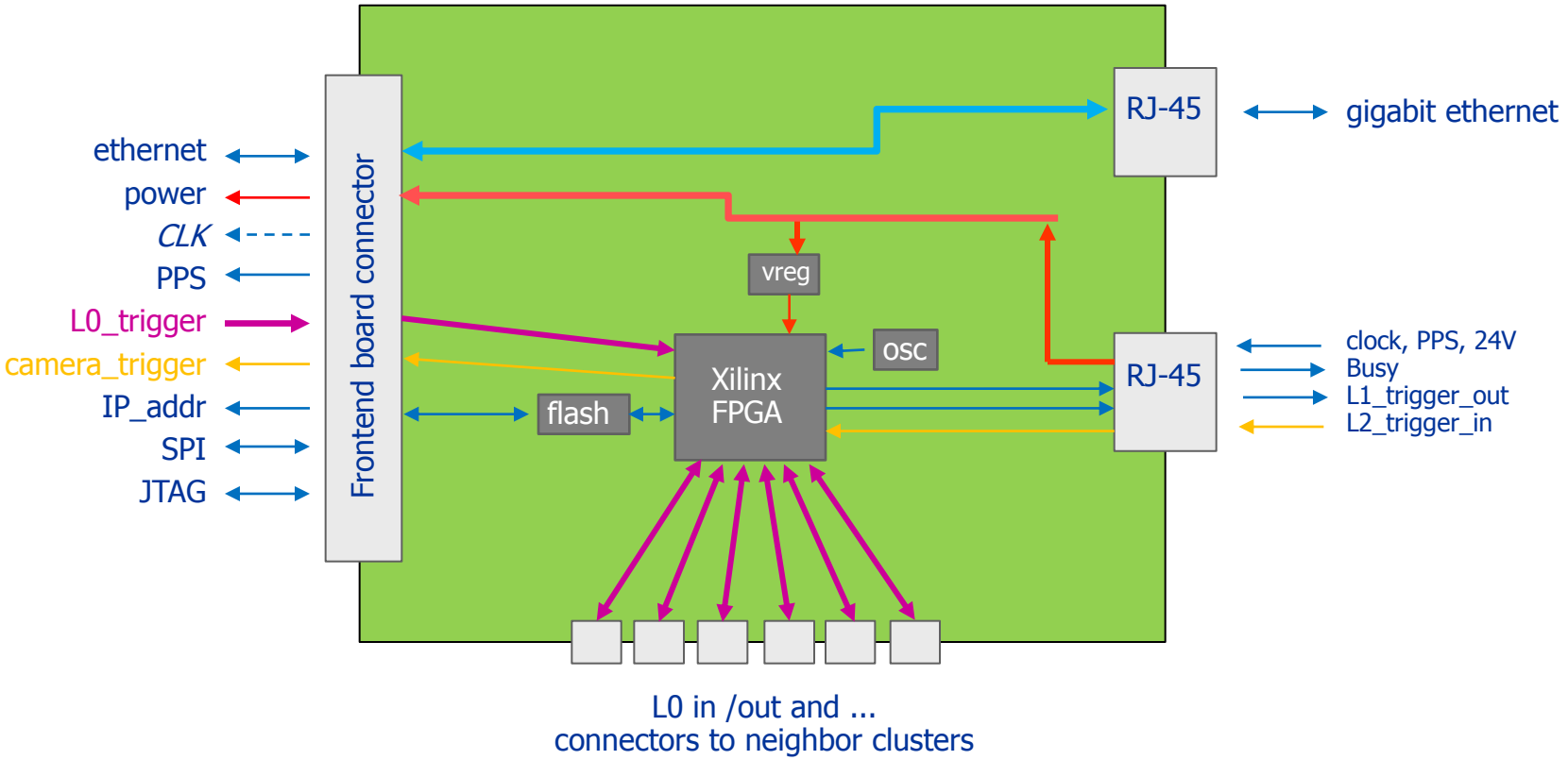




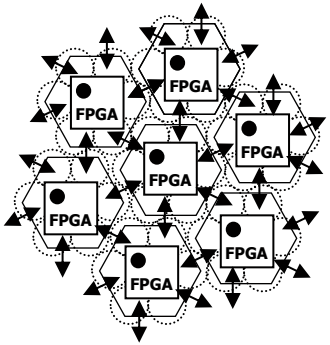
L1 (DTB) connections

PMT = Photomultiplier Tube
FEB = Frontend Board
DTB = Digital Trigger Backplane
CTDB = Clock & Trigger Distribution Board
L2CB = L2 Controller Board

L1, Digital Trigger Backplane



The L1-FPGA's Functionality



Xilinx Spartan 6 FPGA

fanout

L0s to surrounding clusters

L0_[0][4..0]

L0s from center cluster

L0_[0][6..0]

progr. delays

trigger mask

37 pixel trigger fabric

L0s from surrounding clusters

L0_[1][4..0]

L0_[6][4..0]

delay

to CTDB

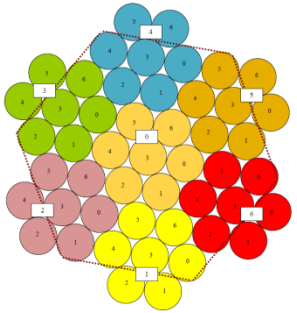
L1

SPI

register block

clock

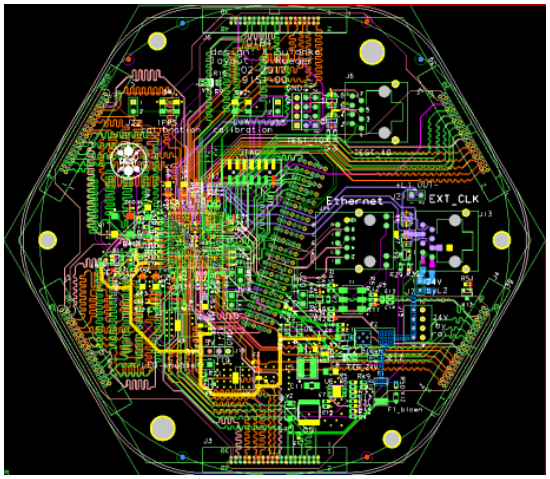
PLL

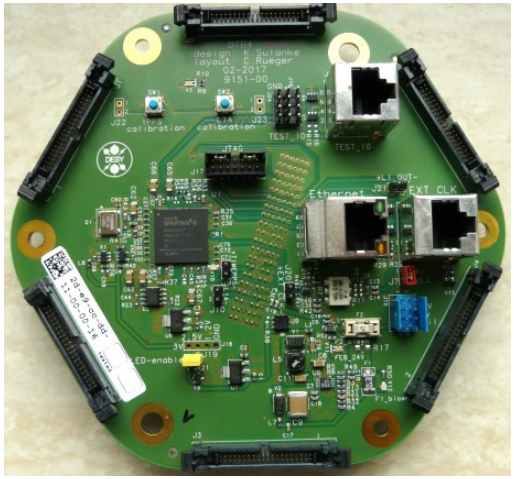


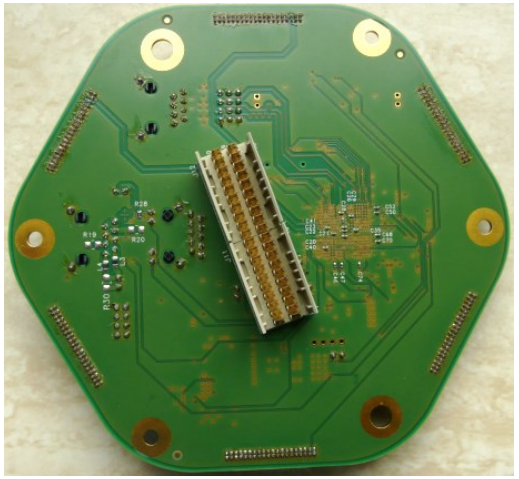
37 pixel map

L1, Digital Trigger Backplane, PCB

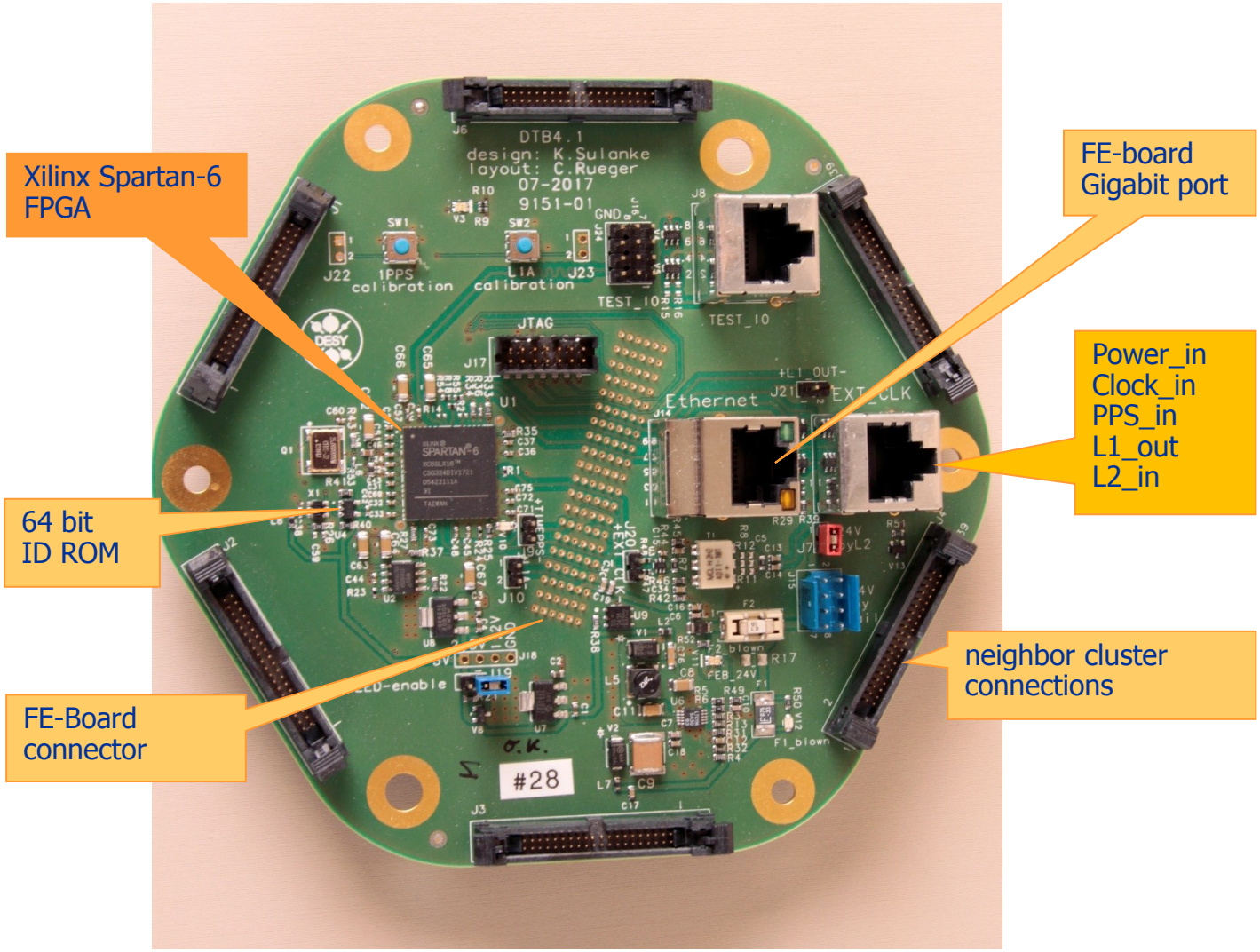
- 4 th revision
- PCB design by Carola Rueger, DESY Zeuthen
- 8 layer PCB, length & impedance matched diff. lines for precise timing
- 324 pin Spartan 6 FPGA
- prototypes assembled in-house
- mass production at DESY-HH workshop (ZE)







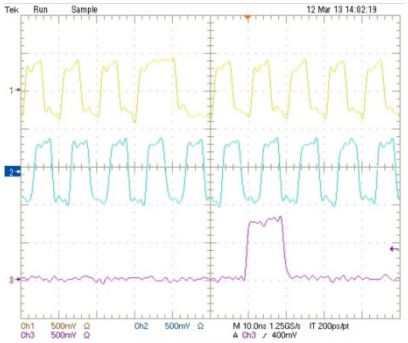
Digital Trigger Backplane, cont.

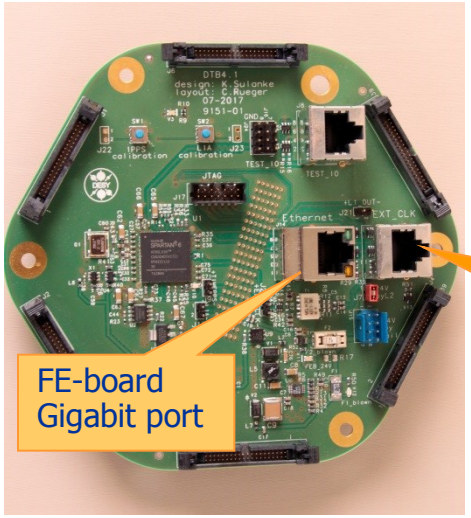


Combined Power and Clock Input

- 24V, clock, and PPS over a single wire pair
- requires a single cat5e..7 cable per cluster only (+ gigabit ethernet cable)
- Current spikes of 0.8 A did not influence the (recovered) clock quality

Cat5e - Wire Pair	usage
1	**Clock_in / PPS_in / 24V**
2	Busy_out
3	Trig_L1_out
4	Trig_L2_in





DTB Firmware Features

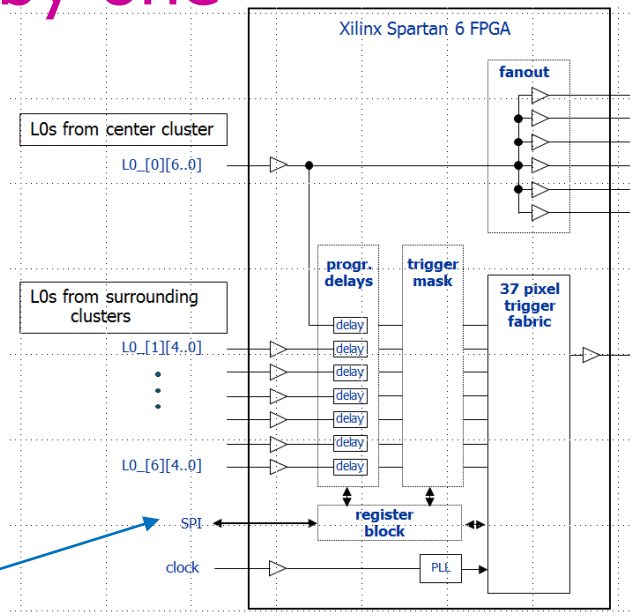
- Fully synchronous design
  - local oscillator (25 Mhz) or external clock (50 MHz)
- presently, 3NN (3 Next Neighbor) of 37 pixel
  - about 500 possible combinations
- Trigger latency ~100 ns
- Trigger time resolution 1 ns (1 GSPS L0-sampling rate)
- Trigger jitter +/- 1 ns
- Firmware automatically detects missing neighbor clusters (bit masking)
- L0 delay, PPS and L1A (L2) adjustment in 37 ps steps
- trigger masking
- programmable trigger window (1,3,5,.. ns)
- special trigger schemes (e.g. AND_2_of_37) for calibration and test
- L1 scaler

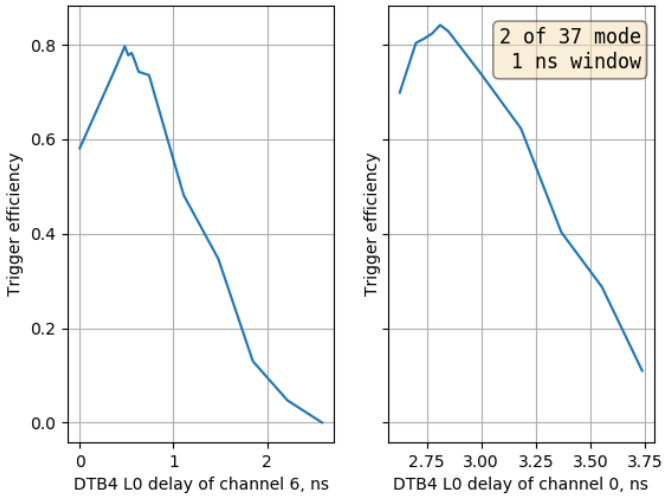
Calibration

- digital trigger works w/o calibration already („turnkey operation“)
- for improved performance, items to calibrate (in green delay diff., max – min, using 45 trigger channels)
  1. 1PPS / clock delay => max. skew = 140 ps
     - further adjustment in 37 ps steps possible
  2. L1 up delay => 0.84 ns, after correction, 4.9 ns w/o correction
     - mostly by the internal delay of the L2-FPGA (OR with 270 inputs)
     - will be improved with next firmware revisions
  3. L2 down delay => 0.57 ns, w/o correction
     - further adjustment in 37 ps steps possible
- L1 up delay has to be calibrated at the L2CB, all other at the DTB (via FEB access)

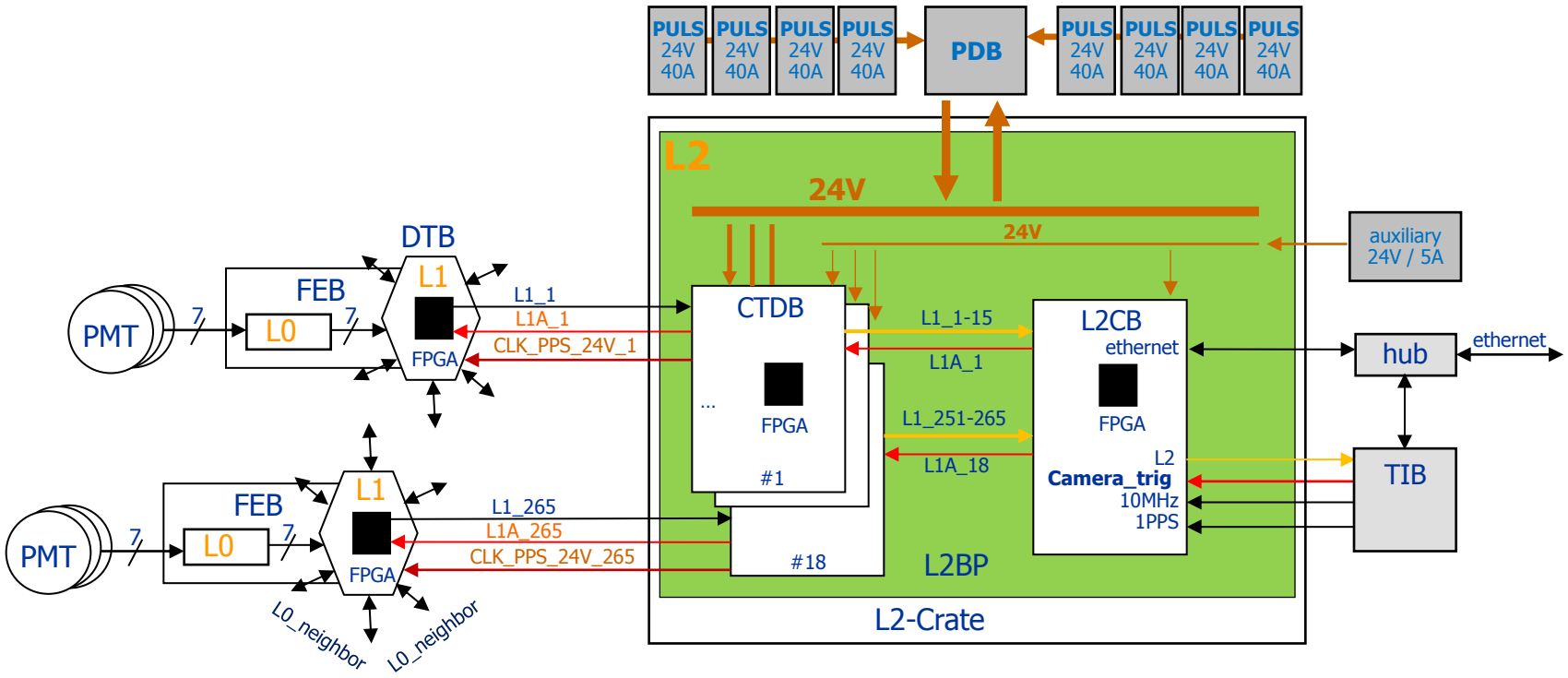
DTB, L0 Delay Calibration, one by one

- uniform LED / laser source with known flasher frequency, e.g. 1KHz
- trigger algorithm switched to AND_2_of_37 (ctrl-reg.)
  - triggers if the central pixel AND one of the selected surrounding are seeing light at the same time
- trigger window set to 1ns
- trigger mask set, to select the pixel to be calibrated, 1 of 36
- software adjusts the L0 delay in steps of 37ps for **max. trigger rate**
- for 1ns trigger window, 100 % trigger efficiency is not possible due to the asyncronous sampling of the L0 signals with 1GSPS
- examples see below, diagrams by Patrick Sizun, IRFU CEA Saclay



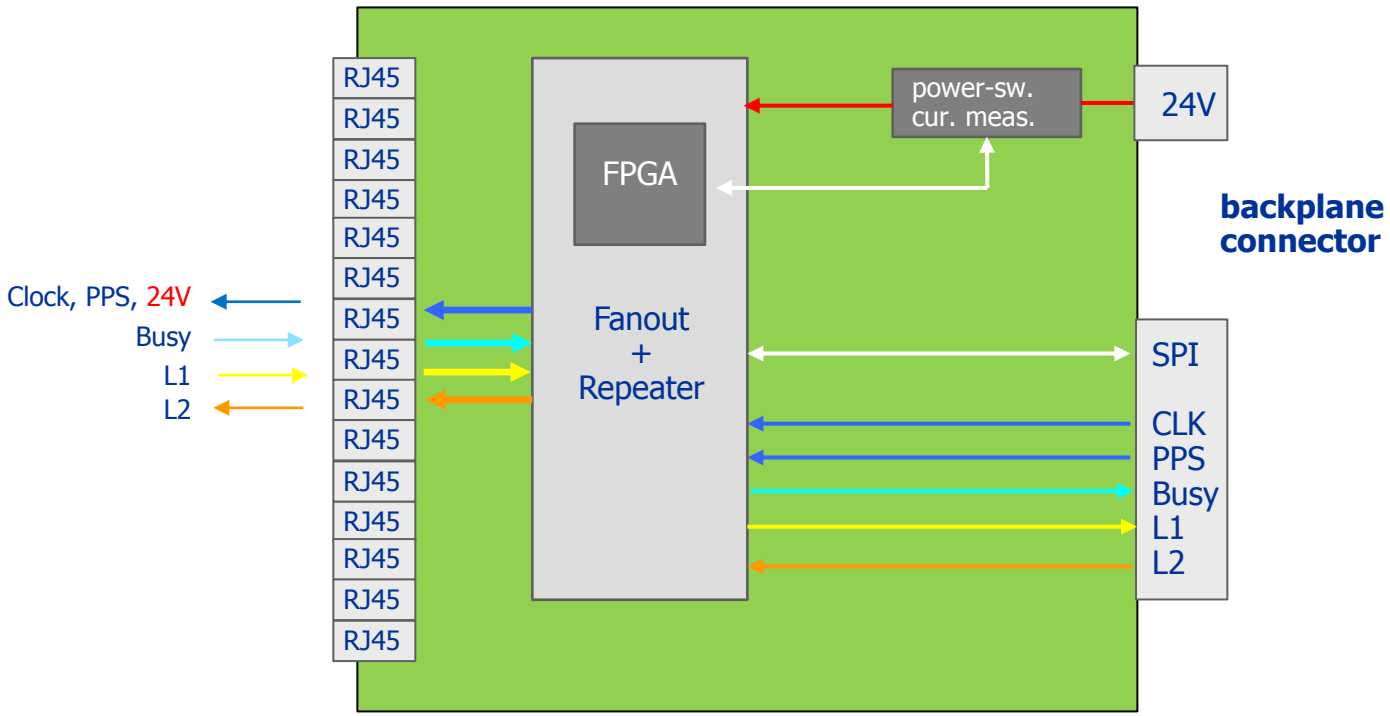


Trigger, Clock & Power Topology



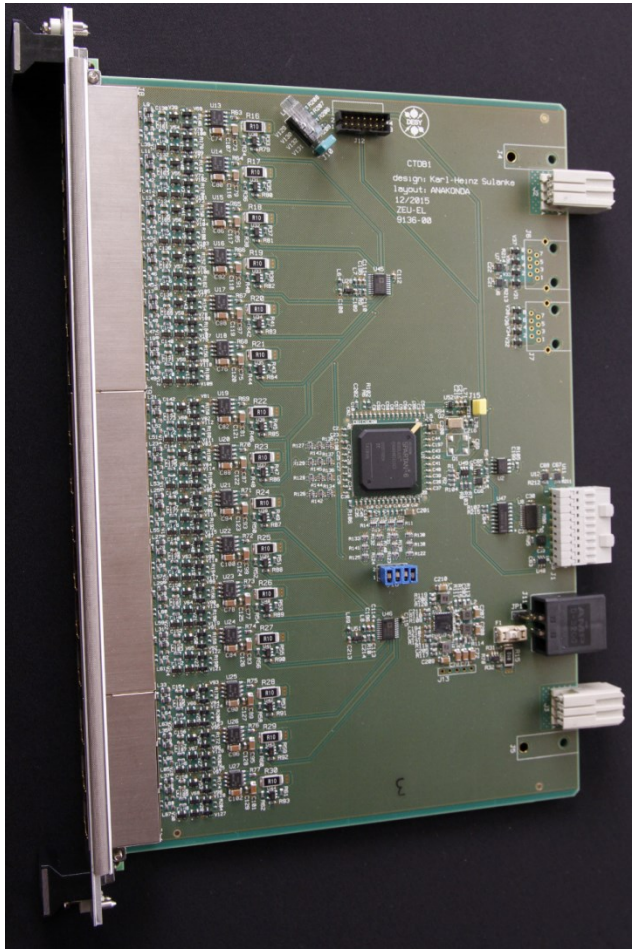
PMT	= Photomultiplier Tube
FEB	= Frontend Board
DTB	= Digital Trigger Backplane
CTDB	= Clock & Trigger Distribution Board
L2CB	= L2 Controller Board
TIB	= Trigger Interface Box (Spain)

CTDB, Clock & Trigger Distribution Board



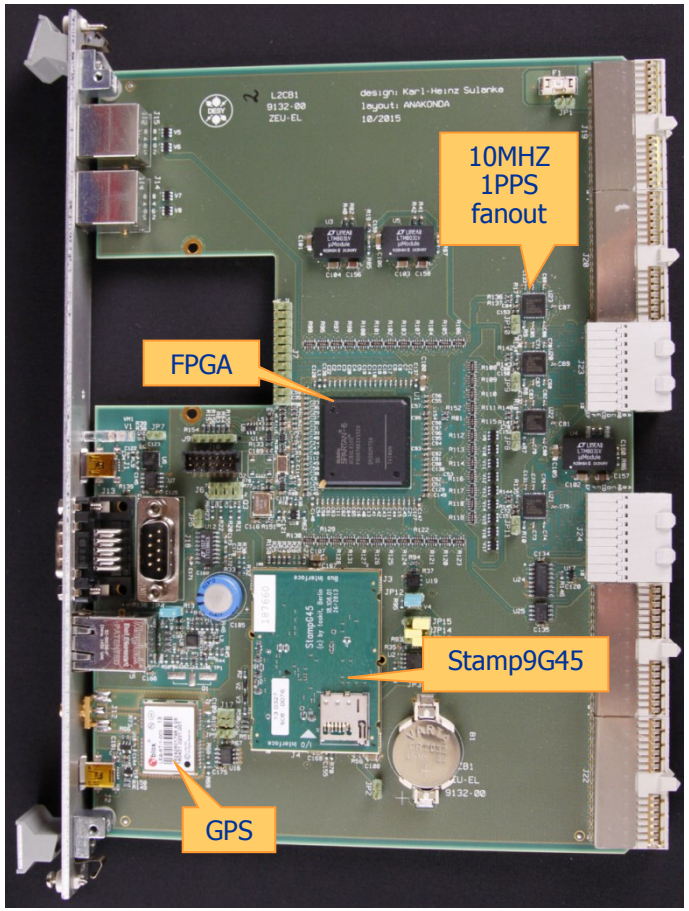
CTDB, Clock & Trigger Distribution Board, cont.

- PCB design by ANAKONDA GmbH Berlin
- 10 layer PCB, length & impedance matched diff.
- Spartan 6 FPGA
- SPI bus interface for slow control with L2CB as master
- **15 channels** (RJ45), each for
  - L1 and BUSY reception
  - clock & 1PPS fanout
  - camera trigger fanout
- FEB remote power control
  - 24V switch
  - current measurement
  - inrush current limitter



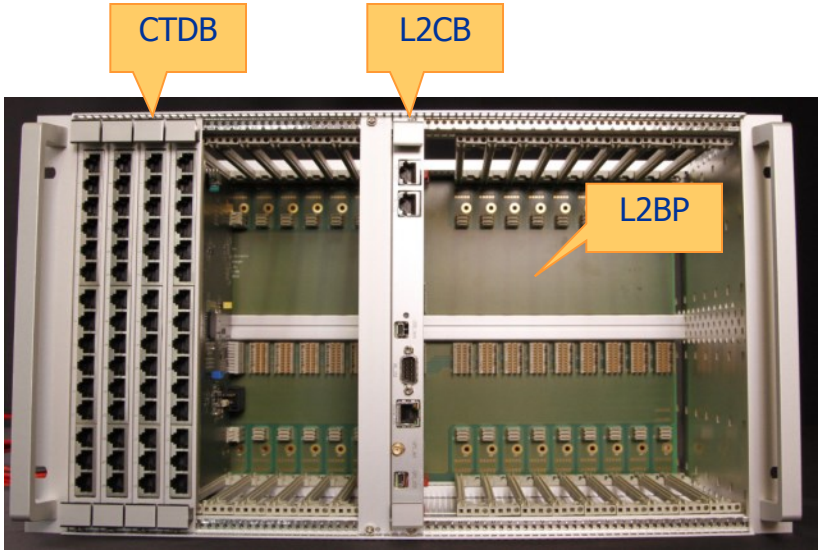
L2CB, L2 Controller Board

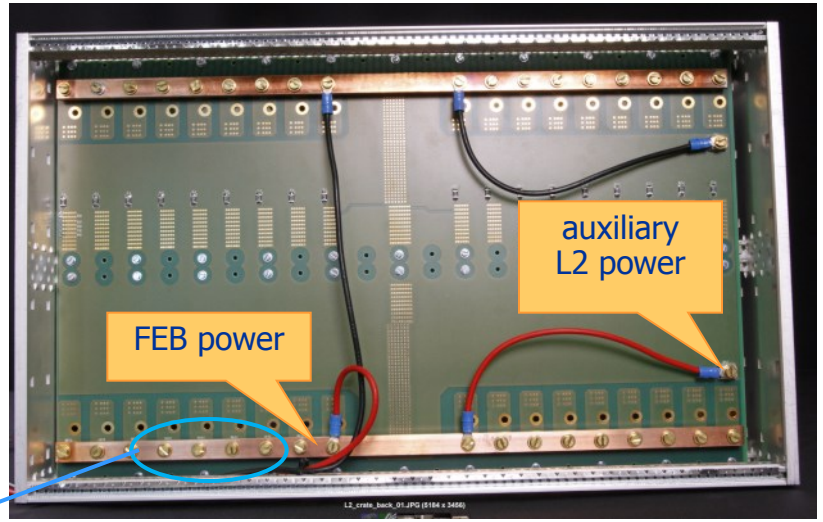
- PCB design by ANAKONDA GmbH Berlin
- 10 layer PCB
- 676 pin Spartan 6 FPGA, processes 265 (270) L1s
- TIB interface (Trigger Interface Box, Spain)
  (camera trigger, BUSY, 10MHz, 1PPS)
- 10MHz / 1PPS fanout 1:18
- ARM based microcontroller unit „Stamp9G45"
  - widely used at DESY Zeuthen
  - Linux
  - ethernet
  - high speed bus connection to the FPGA
  - FPGA, in system firmware update
  - HAL by Marek Penno, Marko Kossatz
  - OPCUA server by David Melkumyan
- SPI bus for CTDB slow control
- GPS (optional usage)
- extension slot



L2-Crate

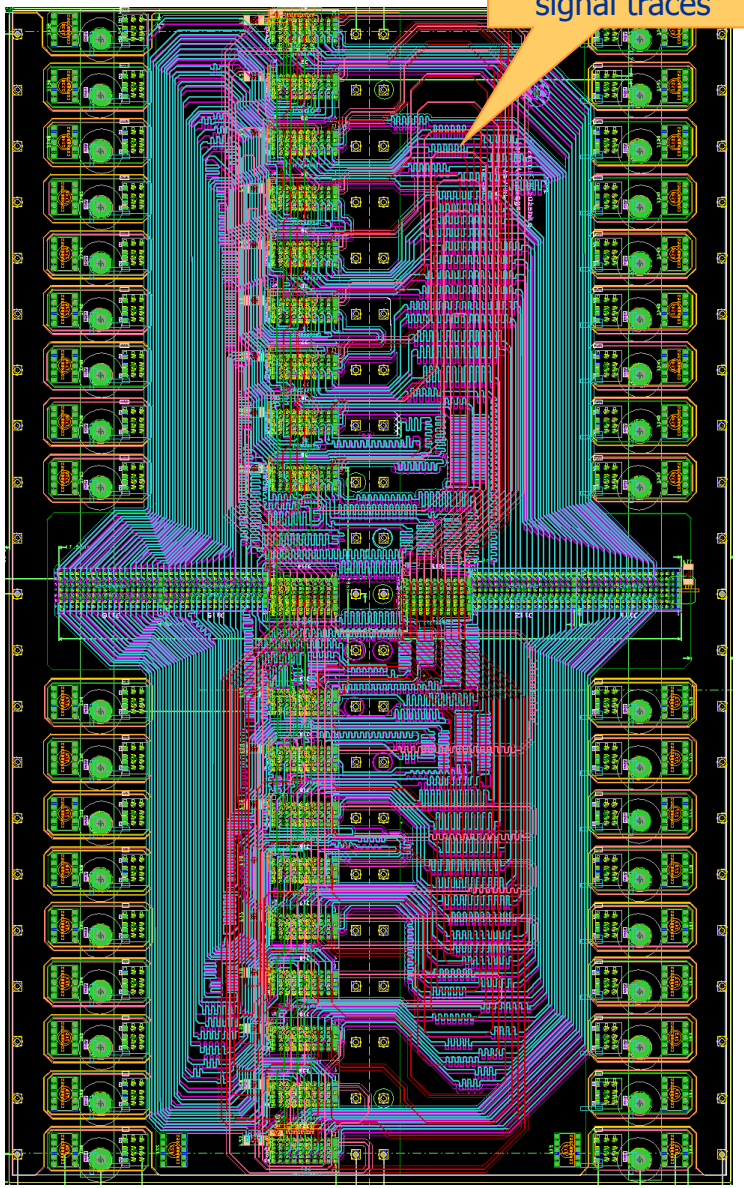
- off the shelf, Schroff 24563-442
- 6U, 84 HP (21 slots)
- Card size : 233 x 160 mm
- 18 x CTDB slots
- 1 x L2CB, pin count = 560 (!)
- 1 x L2BP (L2 Backplane)
- auxiliary power supply, comes up first
  - better for FPGA controlled power switches
- copper rails for the connection of the main 24V power
- overall, ~200 A are being passed thru





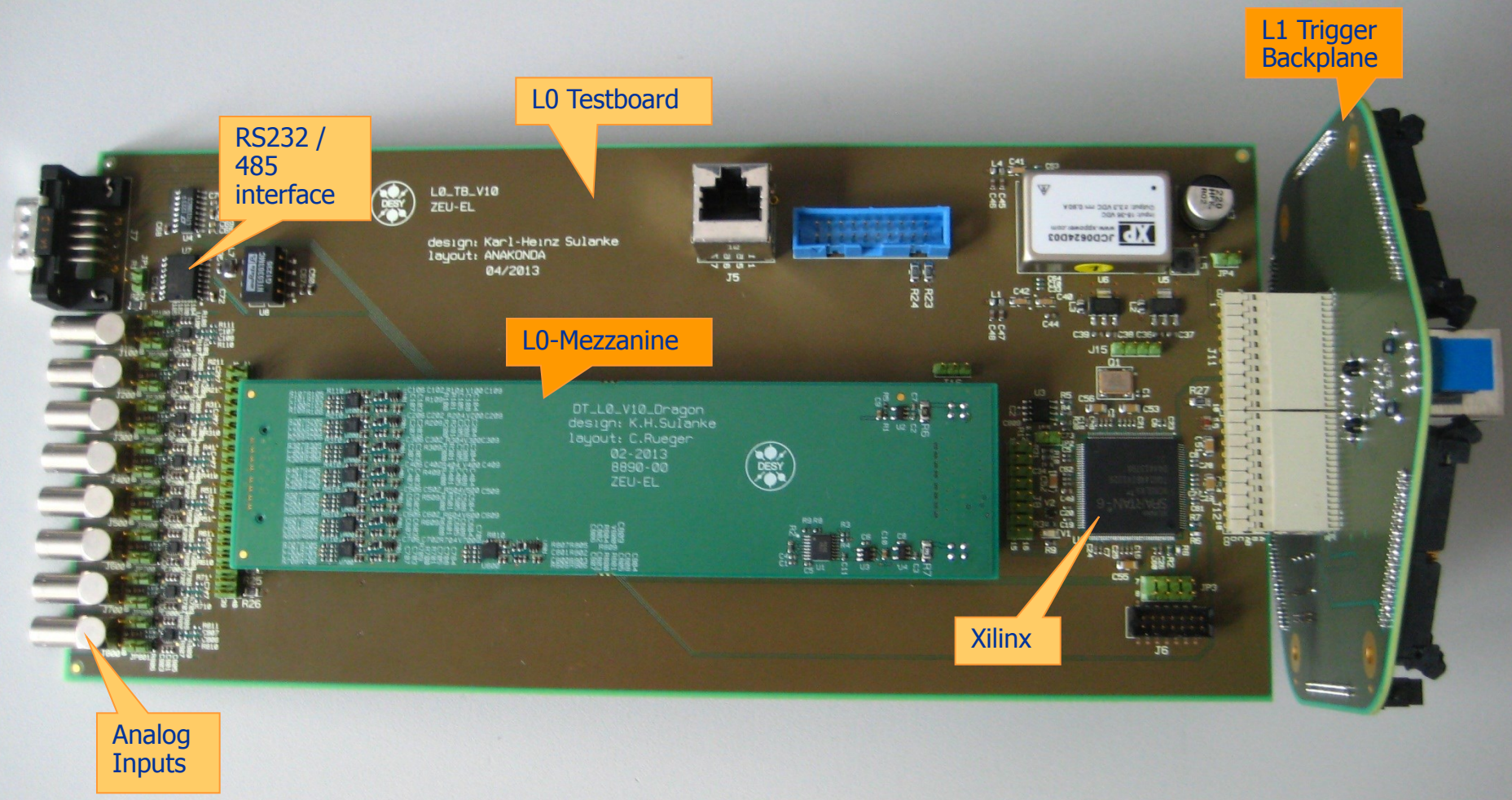
L2BP, L2 Backplane

- PCB design by Carola Rueger, DESY Zeuthen
- 10 layer PCB
- all connectors are of the pressfit type
- all connections between the CTDBs and the L2CB w/o vias
- impedance and length matched traces
- goal is, to get the same trigger and clock delay for each of the 18 CTDB slots
- CTDB slot address is hard wired in the backplane
- SPI bus for L2CB <-> CTDB communication

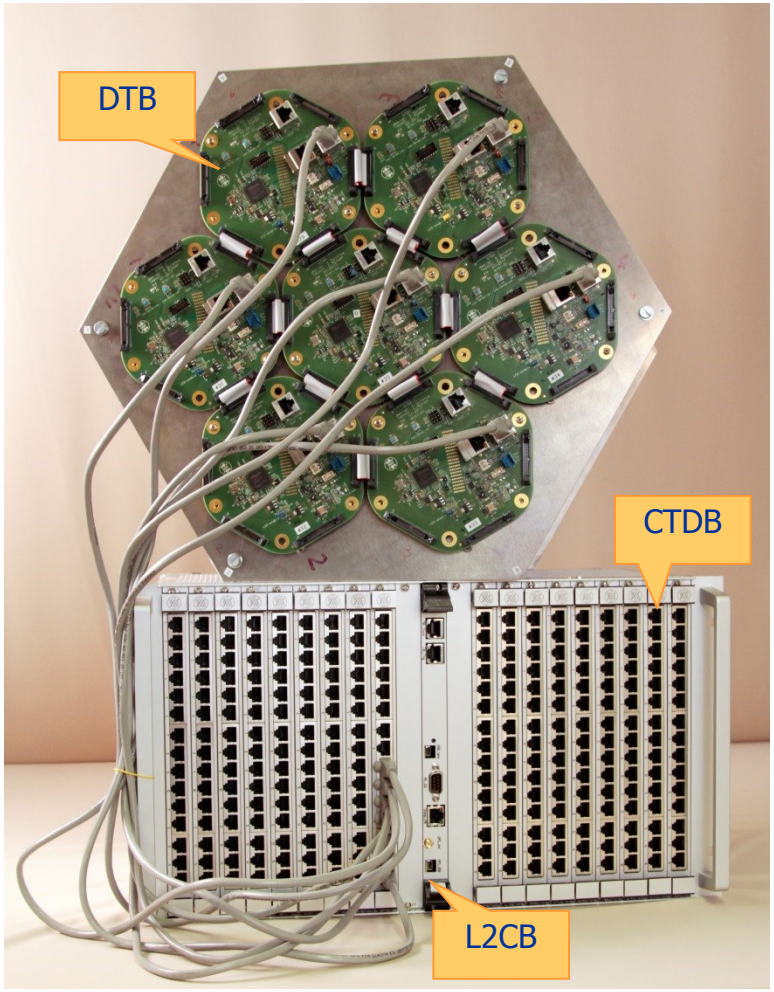


Digital Trigger Test Board

- to test the DTB hardware / firmware, FEBs are rare and more difficult to handle

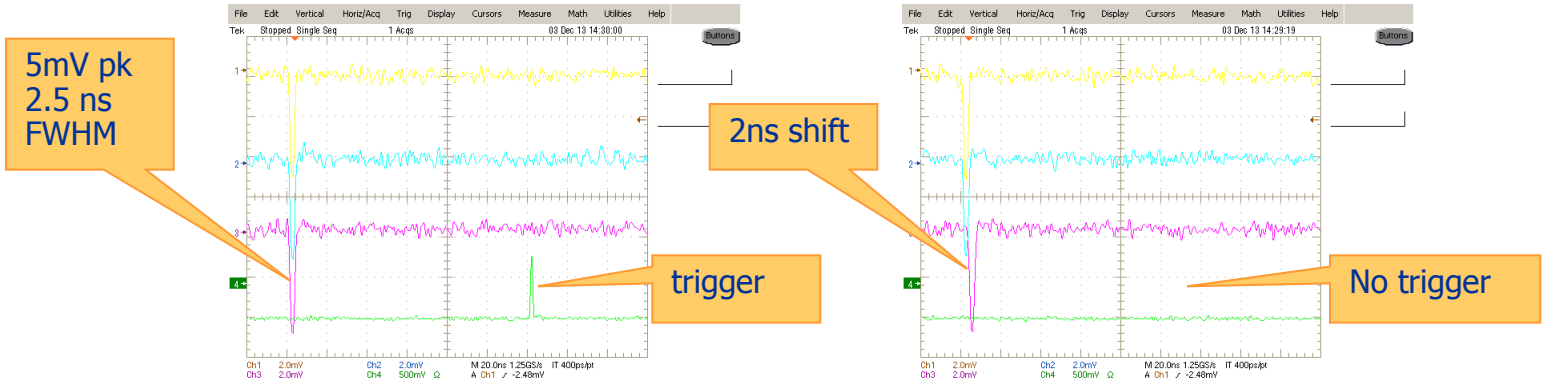


DESY Test Setup

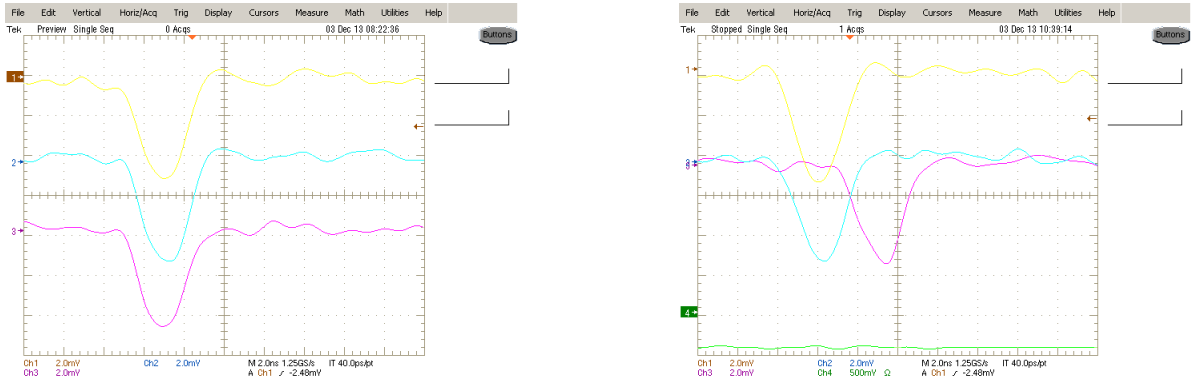


3NN Trigger Test

- 100% trigger and 0% trigger situation

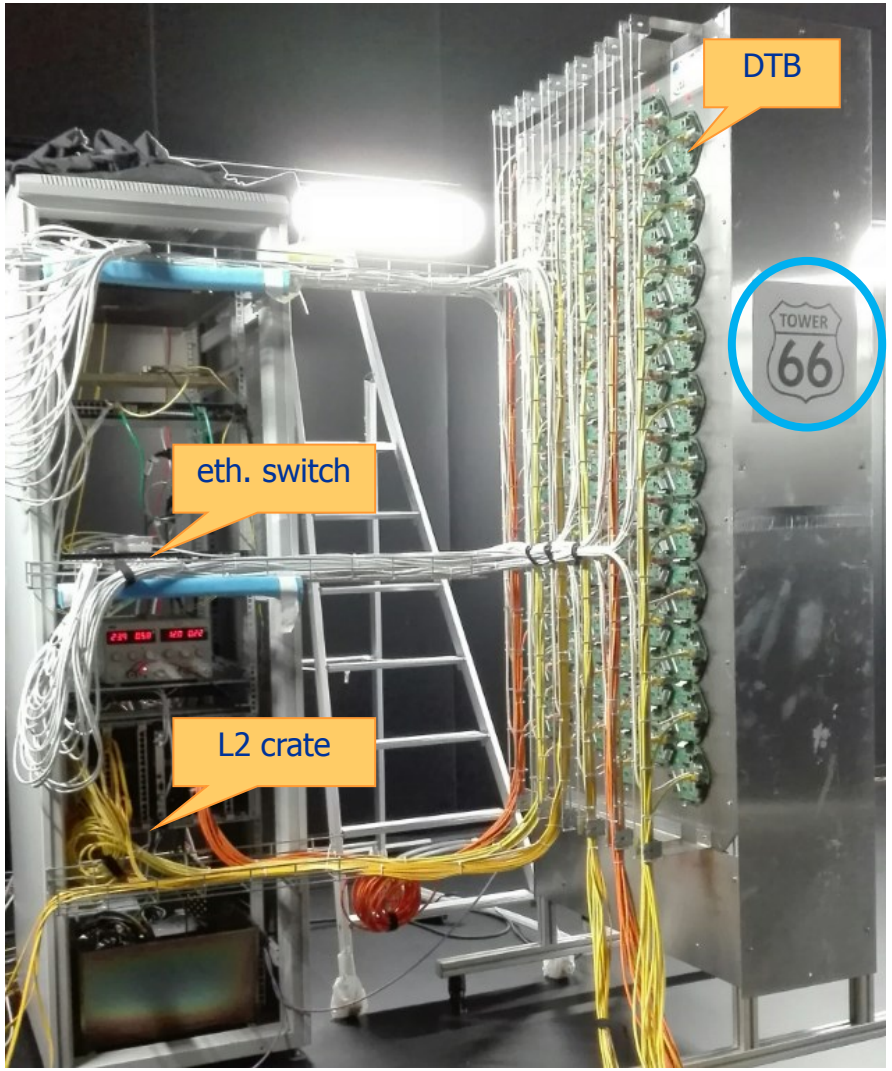


- Analog input signals, zoomed time scale



Test Setup at IRFU, Saclay

- camera test facility (dark room)
- driven by Frederic Louis and Patrick Sizun



Calibration of the NSB source (LED + Photodiode)

by Patrick Sizun

For these tests, we used the first version of the NSB source, soon to be replaced, equipped with a filter of density 2. To choose the current of the LED power supply, we moved a photo-diode to position 275 of the XY table grid, in front of the FPM of interest, and measured the pA-meter current. Given that a current of 934 pA corresponds to a NSB of 1 ph cm^{-2} ns^{-1} sr^{-1} [2], we chose the four current limits indicated in table 1 roughly corresponding to the desired NSB levels.

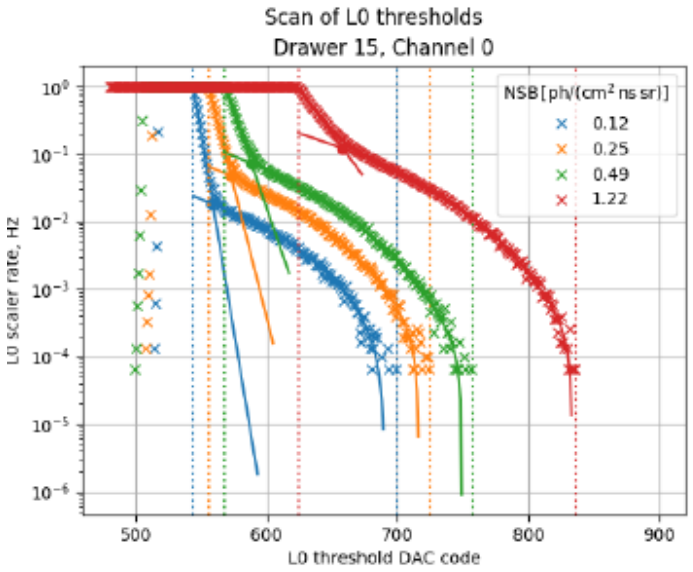
Current limit	NSB [ph cm^{-2} ns^{-1} sr^{-1}]	NSB [MHz]
11 mA	0.12	142
25 mA	0.25	296
50 mA	0.49	580
140 mA	1.22	1445

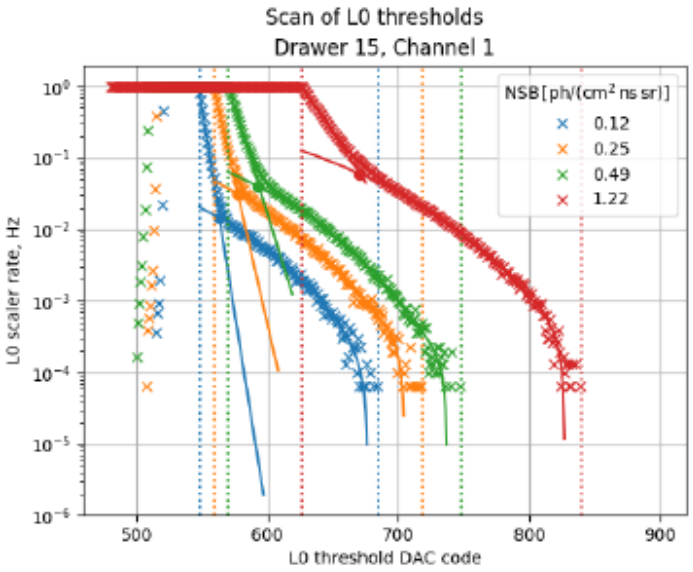
Table 1: Look-up table indicating the power supply current limit used to obtain a given intensity of the night sky background.

Choice of L0 Discriminator Thresholds

by Patrick Sizun

For each NSB level, we scanned the L0 discriminator thresholds (without pulsed light source) and measured the trigger rate at the output of the discriminator using the L0 scaler. The resulting curves are show in Fig. 1. To determine the threshold value where the curve "breaks", the left part was fit with a function $\log y = a\,x + b$ and the right part with a cubic spline. The threshold at the intersection point of the two functions was chosen.

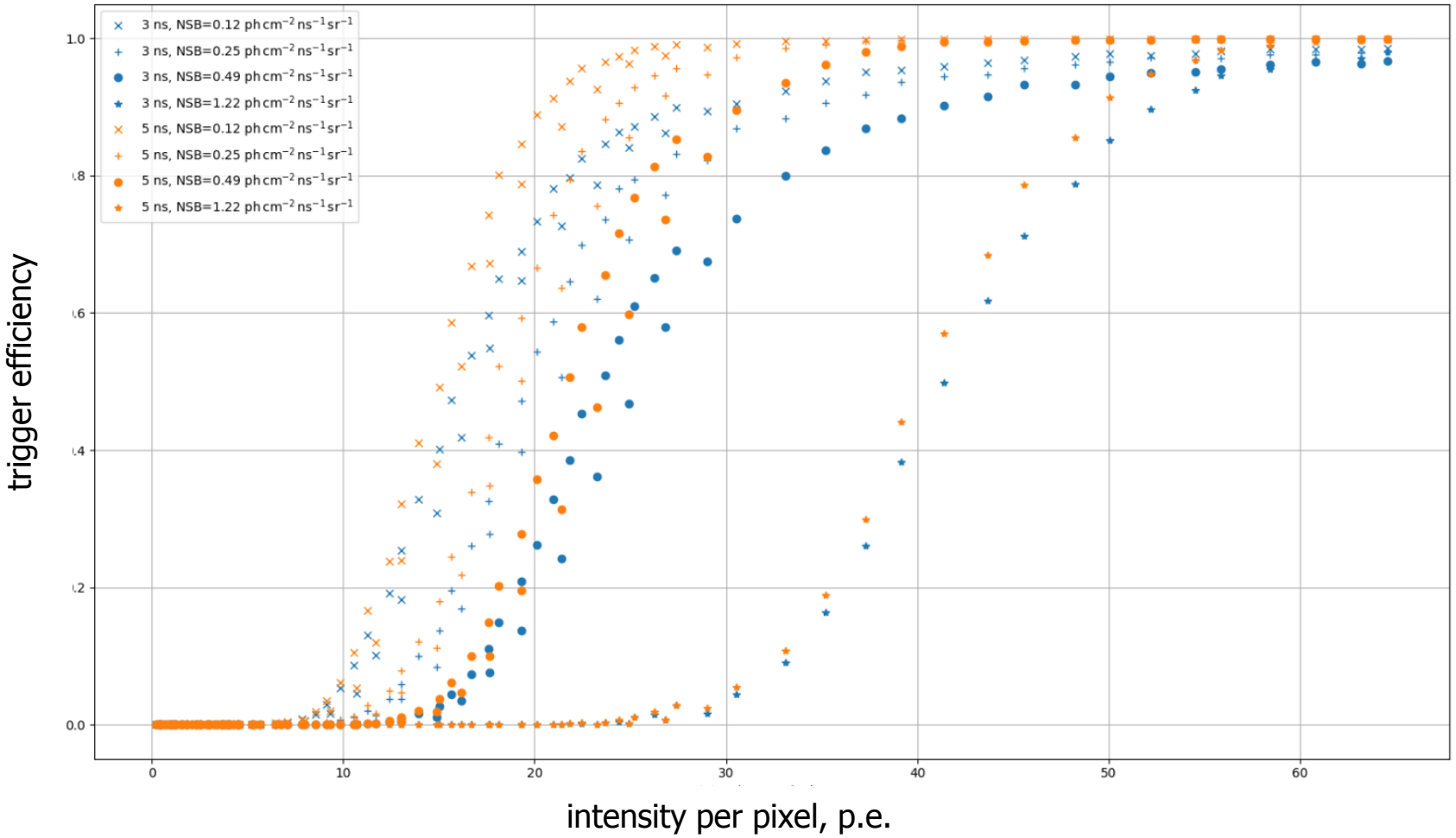




3NN trigger rate vs. NSB and pulsed source intensities

by Patrick Sizun

trigger window, 3 ns (blue) vs. 5 ns (orange)



Summary and next Steps

- Main advantage of the digital trigger is its flexibility concerning the trigger algorithm and the simplicity of the overall scheme
- it can be used both for MST-NectarCam and for LST-DragonCam
- all elements are fully tested, ready for the „mass production" towards 15 NectarCams
- firmware almost complete, some optimization of the L2CB firmware still needed
- in spring (?) 2019 installation and test of a 70-cluster NectarCam at Berlin-Adlershof planned
- end of 2019 (?), first fully equipped camera including 265 DTBs, produced at DESY HH

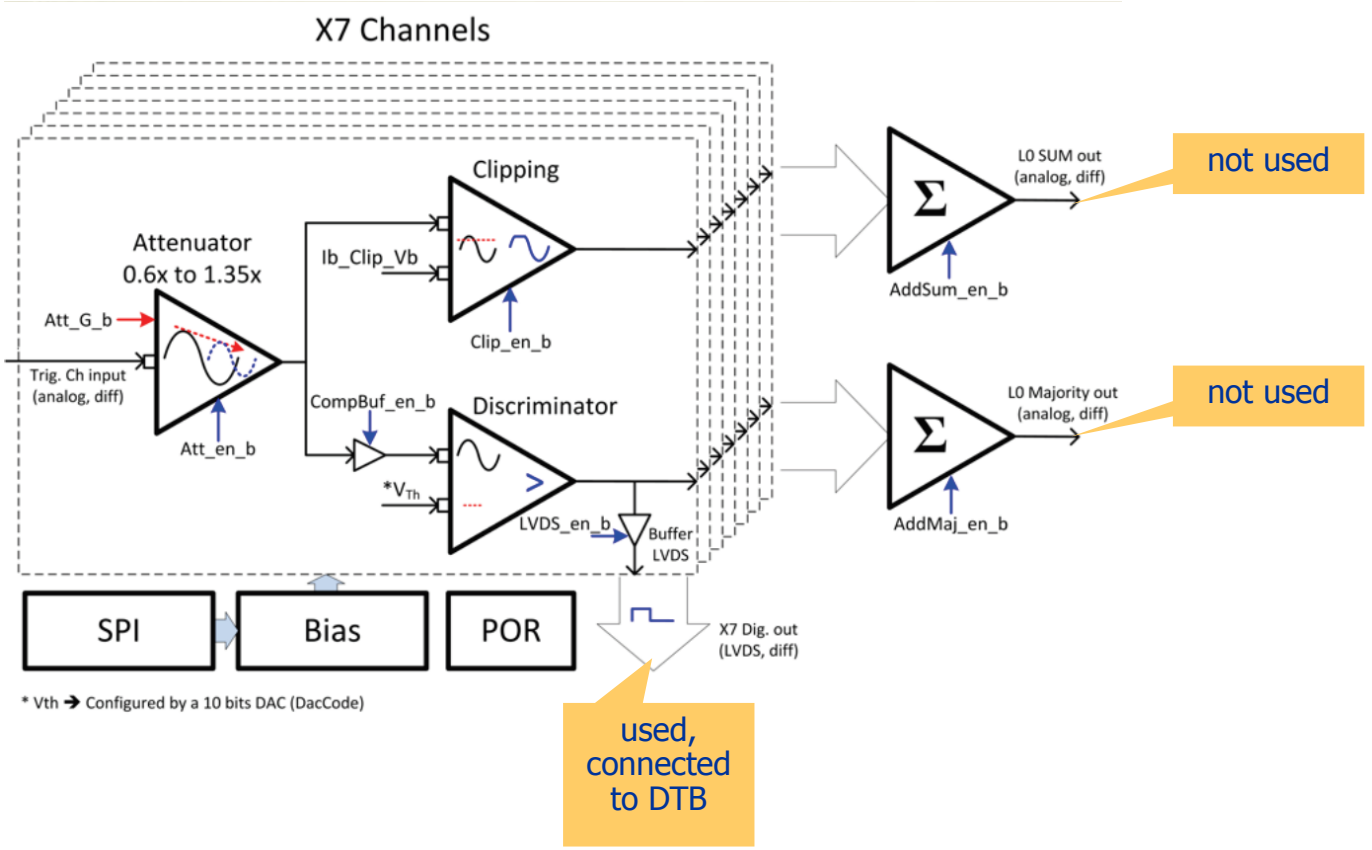
Waiting for the NectarCam ...

Thanks !

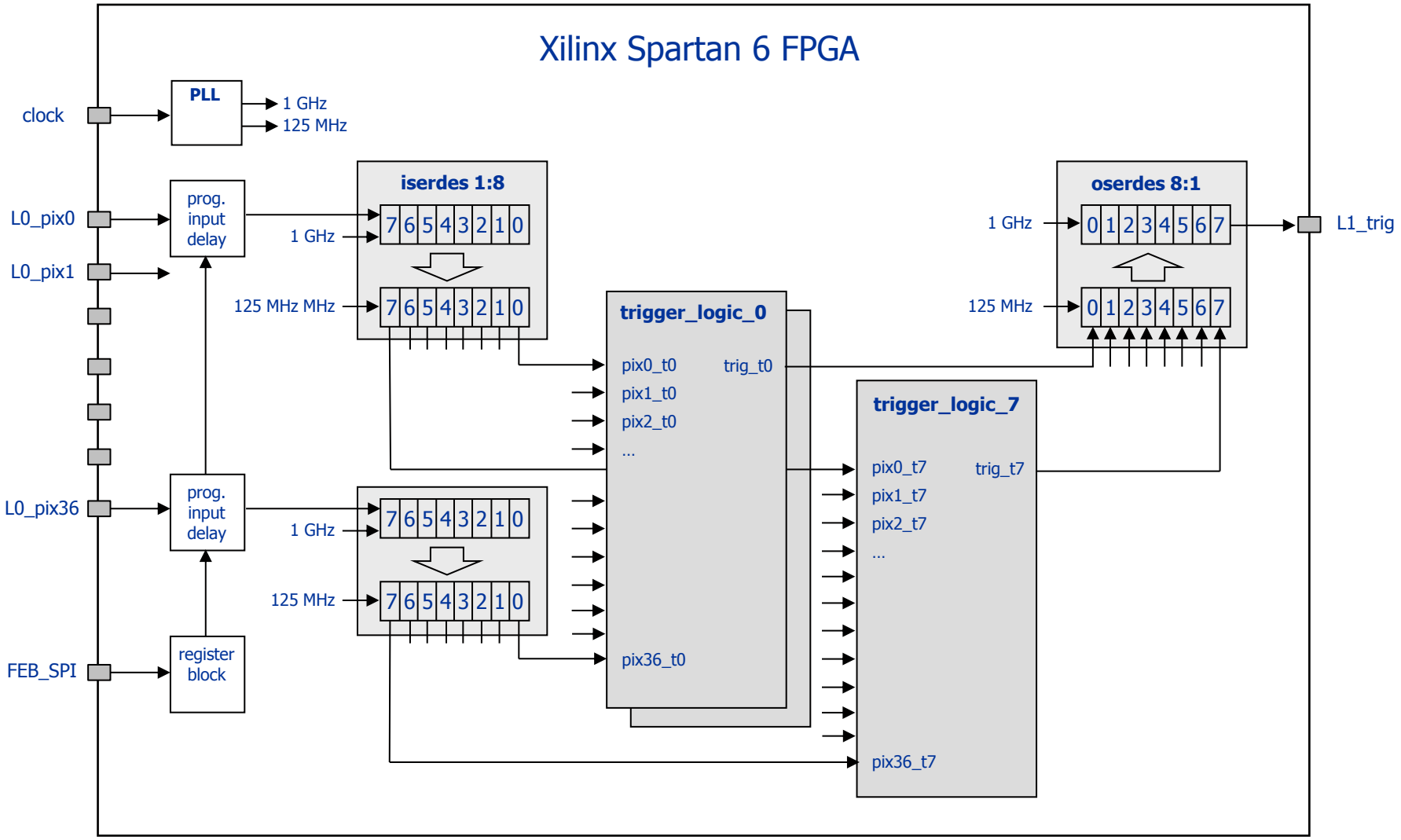
Back Up Slides

L0 Trigger ASIC

- design by Andreu Sanuy, David Gascon, Universidad de Barcelona
- analog outputs not used



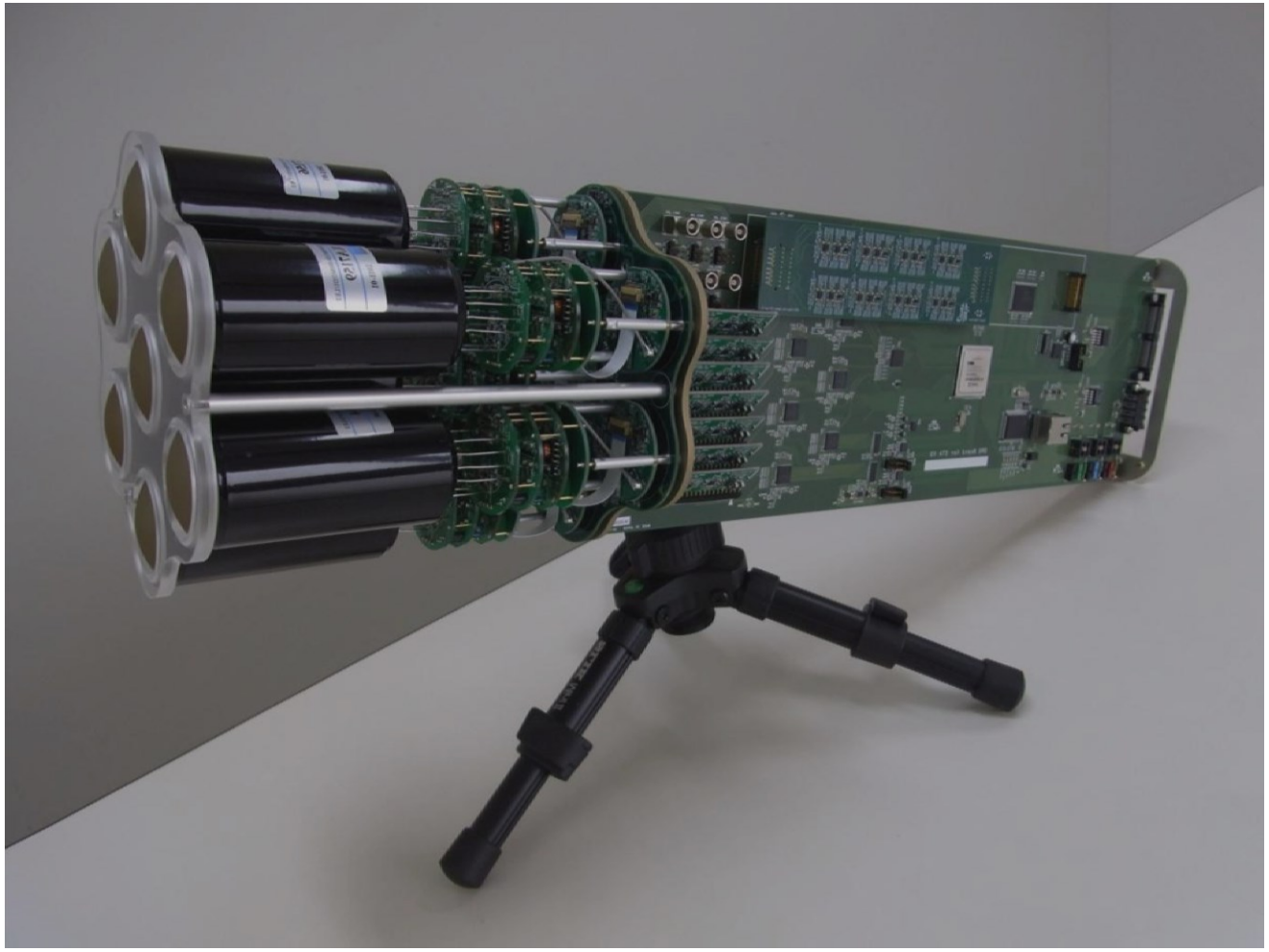
The L1-FPGA's Functionality, cont.



Digital Trigger Backplane, List of Key Hardware Features

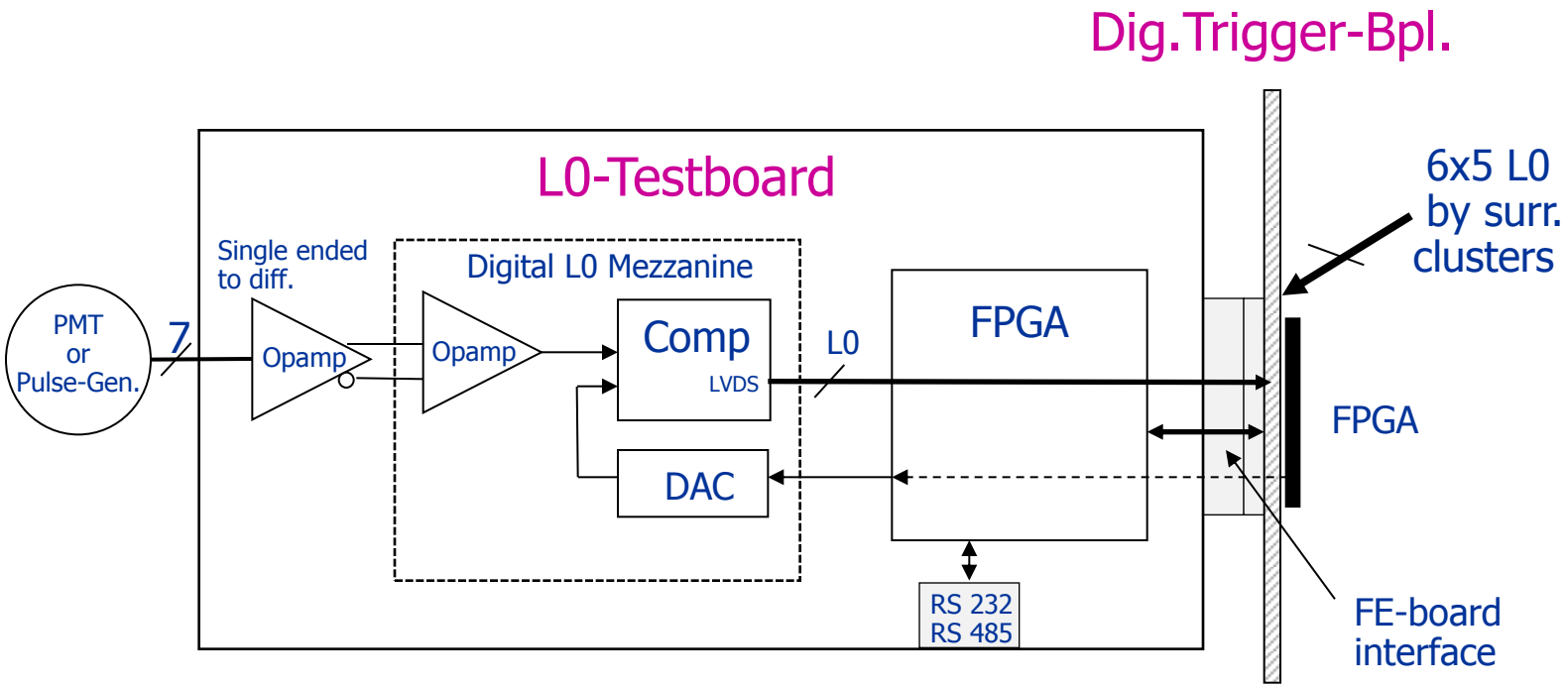
- Nominal power consumption: 1.5 W
- Weight : 95 g + 10 g cabling to neighbor clusters -> 28 kg for MST
- Automatic neighbor cluster recognition (border zone)
- Synchronous DC-DC converter (24 V to 3.0 V …)
- Local clock and external clock input (any diff. > 0.1V pk-pk)
- FPGA load by JTAG cable or PROM or remote (by FE board)
- 6 x bidirectional L0 signal connection with neighbor cluster
- Temperature sensor (allows automatic delay correction, if needed)
- Gigabit ethernet pass through connection to FE-board
- RJ 45 connector as combined power and clock input (single cat5e cable)

7-PMT-Cluster “DragonCam”



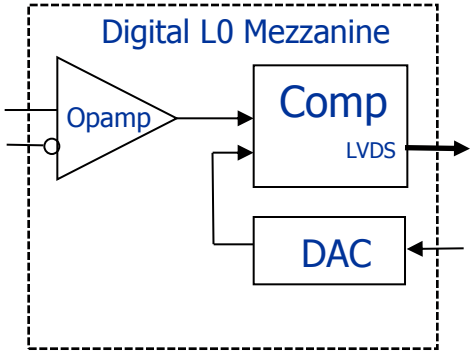
Digital Trigger Test Board

- Testing the L0 boards AND the FE-board interface of the Dig. Trigger Backplane
- Xilinx with RS232 / RS485 interface, to set the discriminator thresholds etc.



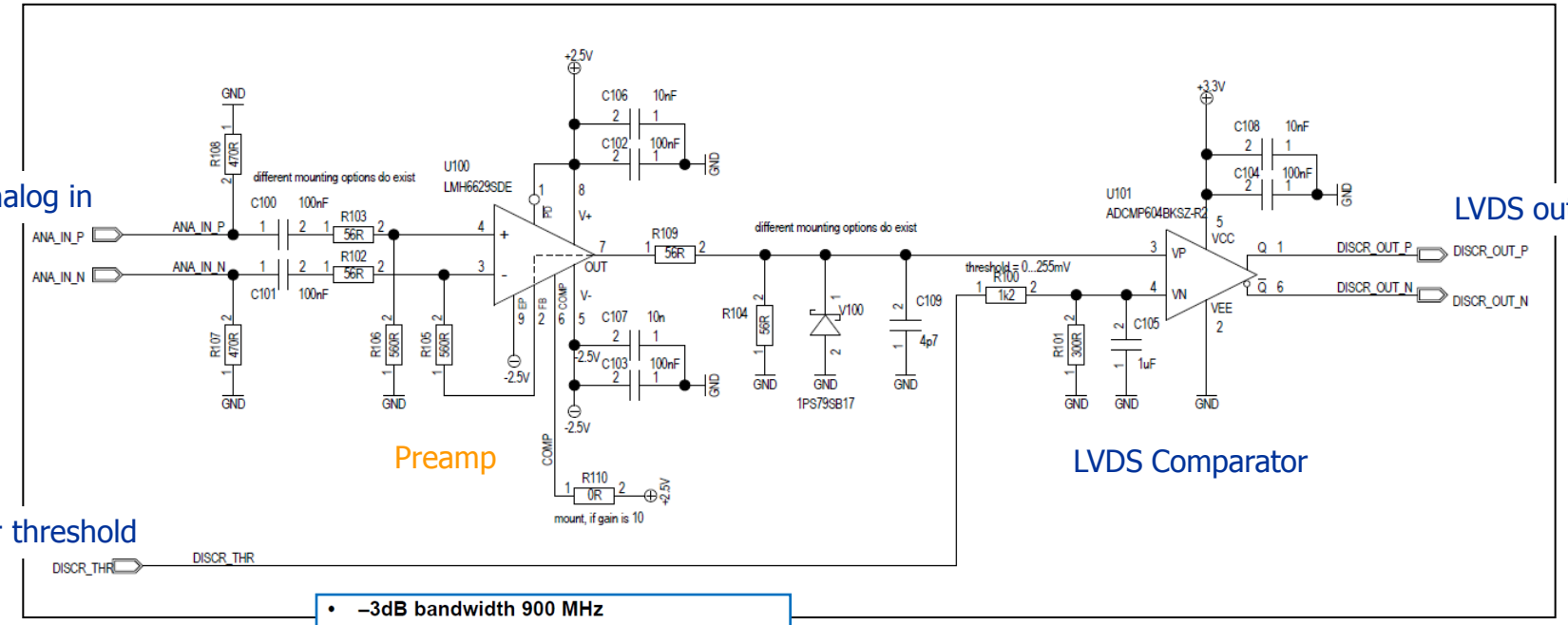
Digital Trigger L0 Mezzanine Board

- 7 channels
- Schematic simulated
- LMH6629, very low noise, low offset preamplifier



Diff. Analog in

Trigger threshold

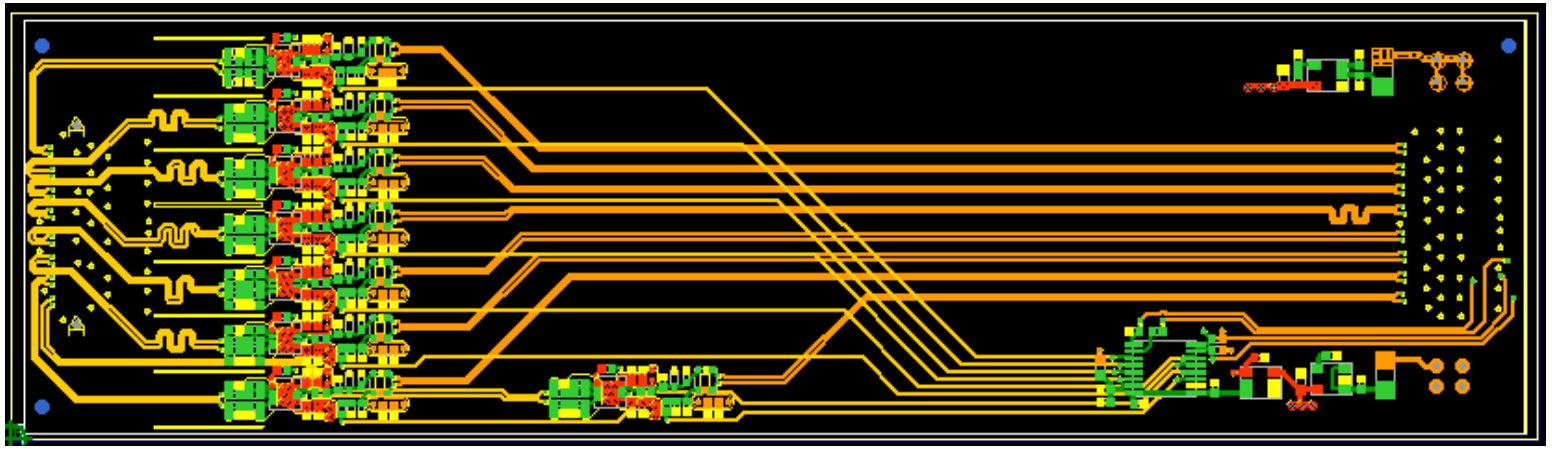


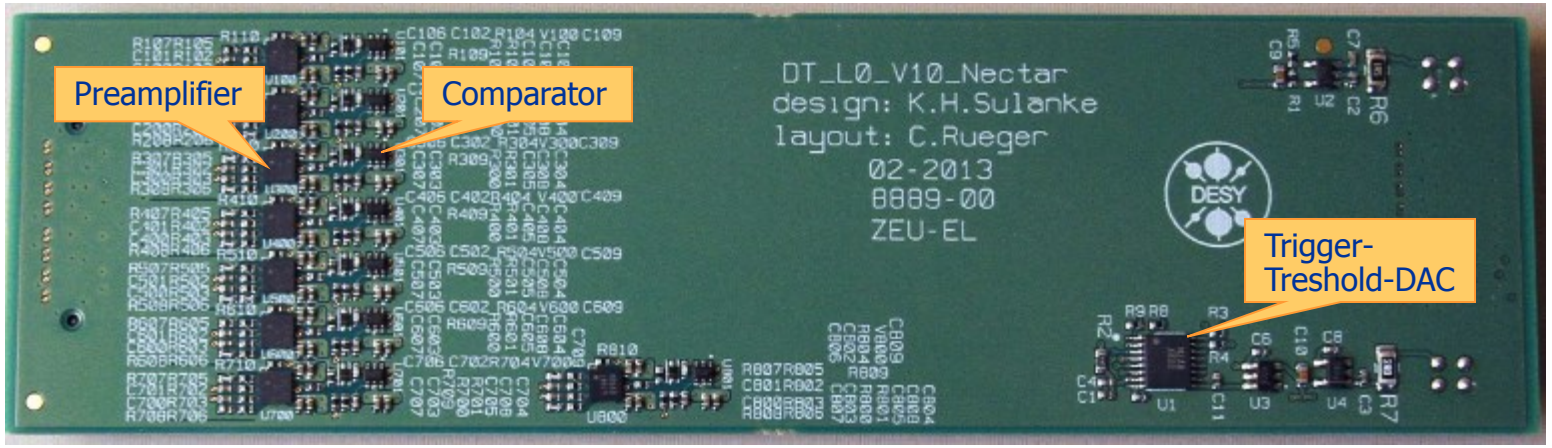
LVDS out

- **–3dB bandwidth 900 MHz**
- **Input voltage noise 0.69 nV/√Hz**
- **Input offset voltage max. over temperature ±0.8 mV**
- **Slew rate 1600 V/ µs**

Digital Trigger L0 Mezzanine Board

- 6 layer PCB with length-tuned signal lines



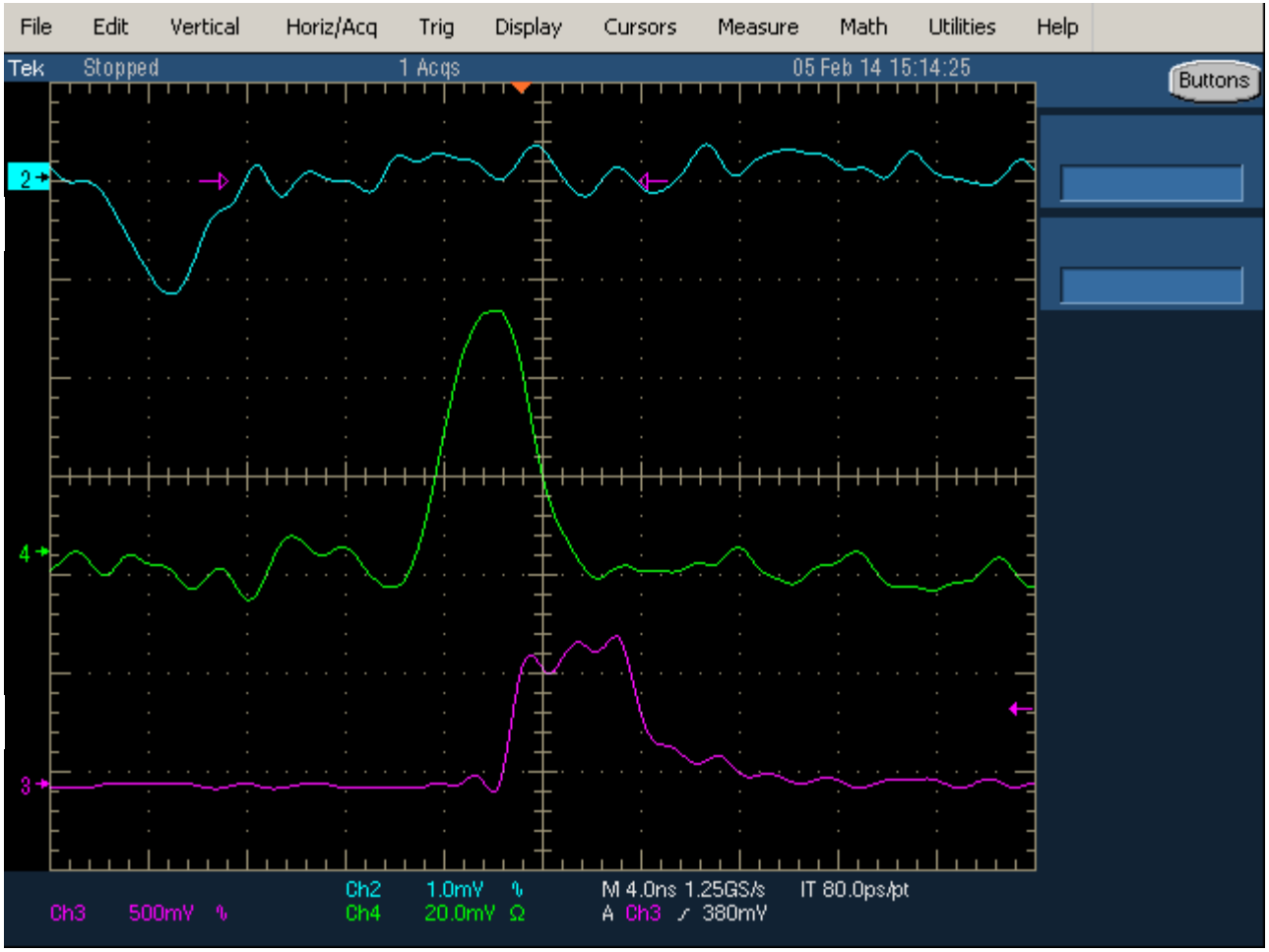


L0, minimum analog input Level

Analog_in, 1mV pk

Comp_in, gain = 27

Comp_out, thr=12mV



L2 Trigger Sectors, MST, Example

- 271 cluster shown (1897 pixel)
- Each sector comprises 14..16 clusters and is connected to a certain CTDB board (L2 crate)