Digital Trigger, Status

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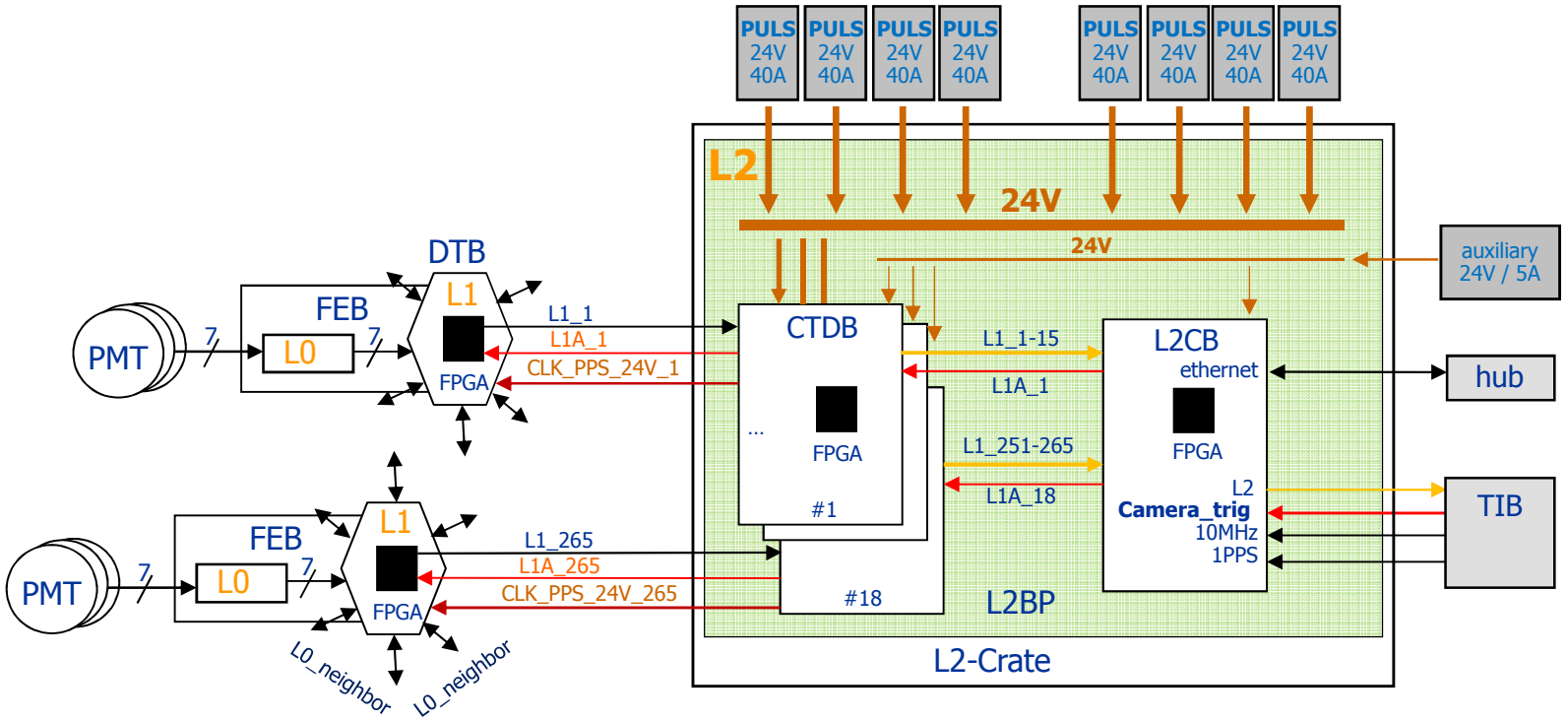
DESY

Contents

- Current / power management, L2 crate
- Cat6 cabling for power, clock, trigger and busy signals
- Calibration
- Firmware status
- DTB3
- Costs
- Trigger down selection
- Conclusions

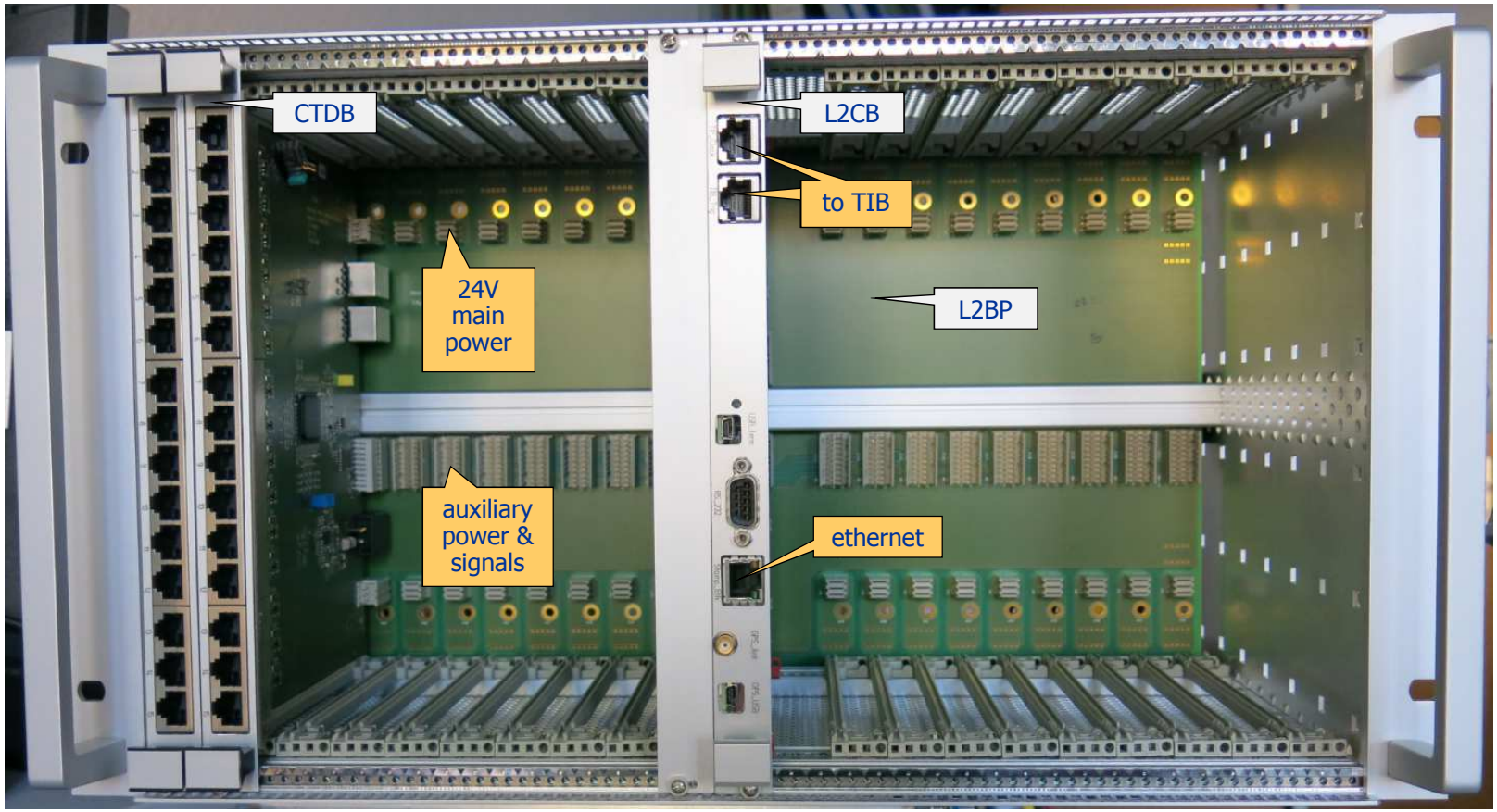
Trigger & Power Topology



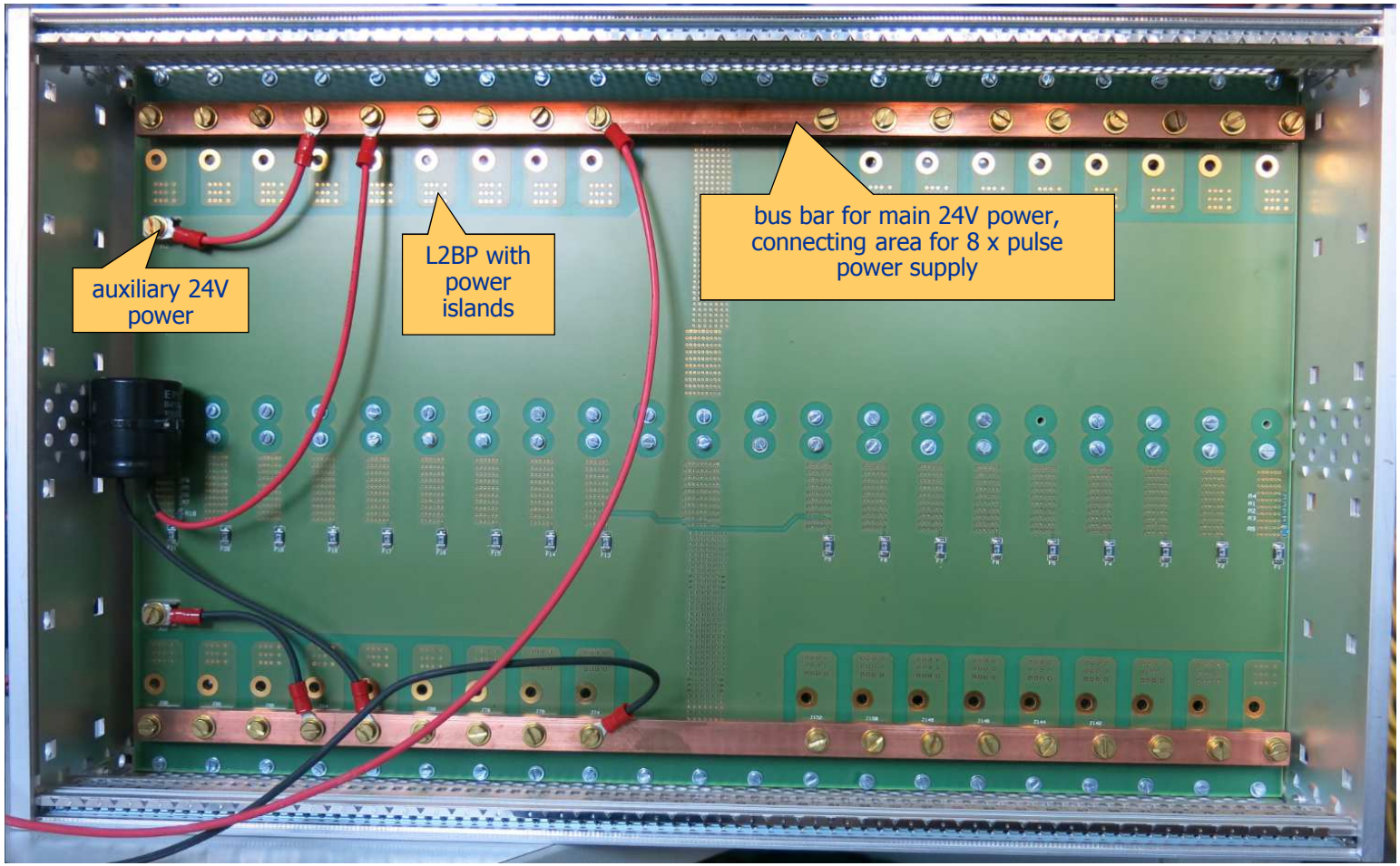
- 265 mezzanines (L0) + 265 DTBs (L1)

PMT = Photomultiplier Tube
FEB = Frontend Board
DTB = Digital Trigger Backplane
L2BP = L2 Backplane
CTDB = Clock & Trigger Distribution Board
L2CB = L2 Controller Board

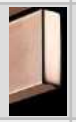
L2Crate with L2 Backplane, Lab Setup, Front View



L2Crate with L2 Backplane (L2BP1), Lab Setup, Back View



Checking the whole Current Path

#	item	cur. max	remark
1	stranded cable, 16mm2 Cu	82A	in bundle, up to 60° ambient temp., PVC or better isolation
2	tubular lug, M6 (eyelet), 6 AWG	95A	e.g. Multicomp MC000763 
3	bus bar 	427A 250A	e.g. 20x10 mm, overkill …, due to 8 x current distribution ->12x5 mm o.k.
4	power tap, 10 pin	40A	18, one per slot, Erni 214782 
5	L2BP PCB, copper island	60A	6 layer 18µ x 15mm parallel
6	vert. power conn., L2BP	48A	TE 5-223955-2 
7	hor. power conn., CTDB	48A	TE 5-5223961-1 
8	CTDB PCB	50A	47 vias, 0.3mm, 2 layers, 18 µ x 100mm
9	RJ45 port, CTDB 	3A	1.5A / 125V AC per contact, HARTING 09 45 551 1123
10	cable, Cat6a, AWG 26, 1 pair	2.1A 3.2A	at 50° ambient temp., at 35° ambient temp., 
11	RJ45 conn., DTB 	3A	1.5A / 125V AC per contact, MOLEX 85508-5001

- assuming a max. continuous current for DTB+FEB of 1A
- => connectors, PCB and cabling are sufficient, even at:
  - 100% overload (2A)
  - ambient temperature of 50°C

Maximum Current, Copper Wires

- absolute values do not exist, one has to consider:
  - ambient temperature
  - max. allowed temperature (warm up) of the wire
  - material, used for the insulation
  - way, the cables are arranged, e.g. in bundles, tubes
  - etc…
- standards do exist, e.g. DIN VDE 0891 T.1 und VDE 0100 T.523, 1981-06 Gruppe 2

  -> max. current density 10..15 A/mm2 at d= 2 to 0,5 mm

Einzelader Durchmesser [mm]	Querschnitt [mm²]	Oberfläche pro 1 m Länge [mm²]	Widerstand*) pro 1 m Länge [Ohm]	Adern	Ges. Querschnitt [mm²]	Ges. Oberfläche pro 1 m Länge [mm²]	Ges. Widerstand pro 1 m Länge [Ohm]	max. zulässig (max. Strom)*) [A]	Kupfer-Masse pro 1 m Länge [g]
0,020 *(= 20 µm)*	0,00031	63	55	320	0,101	20.000	0,17	*1,7 (0,36)*	0,90
0,020 *(= 20 µm)*	0,00031	63	55	460	0,145	29.000	0,12	*2,3 (0,52)*	1,3
0,030 *(= 30 µm)*	0,00071	94	24	36	0,025	3.400	0,68	*0,5 (0,09)*	0,23
0,030 *(= 30 µm)*	0,00071	94	24	200	0,141	19.000	0,12	*2,3 (0,51)*	1,3
0,040 *(= 40 µm)*	0,00126	126	14	35	0,044	4.400	0,39	*0,8 (0,16)*	0,39
0,050 *(= 50 µm)*	0,00196	157	8,8	10	0,020	1.600	0,88	*0,4 (0,07)*	0,18
0,070 *(= 70 µm)*	0,00385	220	4,5	45	0,173	9.900	0,10	*2,8 (0,62)*	1,5
0,071 *(= 71 µm)*	0,00396	223	4,3	20	0,079	4.500	0,22	*1,3 (0,28)*	0,71
0,10 *(= 100 µm)*	0,00785	314	2,2	30	0,236	9.400	0,073	3,7 (0,84)	2,1
0,10 *(= 100 µm)*	0,00785	314	2,2	60	0,471	19.000	0,037	7,1 (1,7)	4,2
0,10 *(= 100 µm)*	0,00785	314	2,2	90	0,707	28.000	0,024	10 (2,5)	6,3
0,10 *(= 100 µm)*	0,00785	314	2,2	120	0,942	38.000	0,018	14 (3,4)	8,4
0,15	0,0177	471	0,97	1	0,0177	471	0,97	0,3 (--)	0,16
0,20	0,0314	628	0,55	1	0,0314	628	0,55	0,6 (--)	0,28
0,30	0,0707	942	0,24	1	0,0707	942	0,24	1,2 (--)	0,62
0,40	0,126	1260	0,14	1	0,126	1.260	0,14	2,0 (--)	1,1

Cat.6a
AWG 26/7
=> ~ 2 A

Shielded Cat.x Cables, Comparison

calculated values based on:

cable length = 3 m

E-Cu, spec. resistance = 0.0172 Ω/mm2 x m

max. current density = 10 A / mm2

	Cat.5e	**Cat.6a**	**Cat.6a**	**Cat.7 - flat**	remark
Order-Nr.	PS5.030.GE	PP6.030.GE	PH6.030.GE	PF7.030.GE	KabelScheune
type	SF/UTP, 4x2xAWG26/7 (7 x 0.16 mm)	S/FTP PIMF, 4x2xAWG26/7 (7 x 0.16 mm)	S/FTP PIMF, 4x2xAWG27/7 (7 x 0.143 mm)	U/FTP, 4x2xAWG30/7 (7 x 0.1 mm)	
weight	81 g	114 g	127 g	103 g	
diameter	5.4 mm	6.5 mm	6.2 mm	7.8 x 2.7 mm	
cross section	22 mm2	33.2 mm2	30.2 mm2	21,1 mm2	
price	1,19 €	4,19 €	6,79 €	4,89 €	
Cu, cross section	0.14 mm2	0.14 mm2	0.112 mm2	0.055 mm2	one wire
resistance	0.184 Ω	0.184 Ω	0.23 Ω	0.47 Ω	one pair
max. cont. current	2.8 A	2.8 A	2.2 A	0.94 A	one pair
power loss	0.12 W	0.12 W	0.15 W	0.3 W	0.8 A
remark		halogen free	halogen free, 3.5 m avail.	gold plated connector shield	

CTDB, Power Switch

- R16 (0.1Ω) for current sensing
- power switch U13 (FPF2702MX)
  - TTL-level on/off input (control by FPGA)
  - short circuit proof
  - power ramping (7.5 ms min), switching to current mode if overcurrent
- R63 for **max. current**, see Table 1.
  - two values tried (120K and 270K)
  - see measurements on next slide

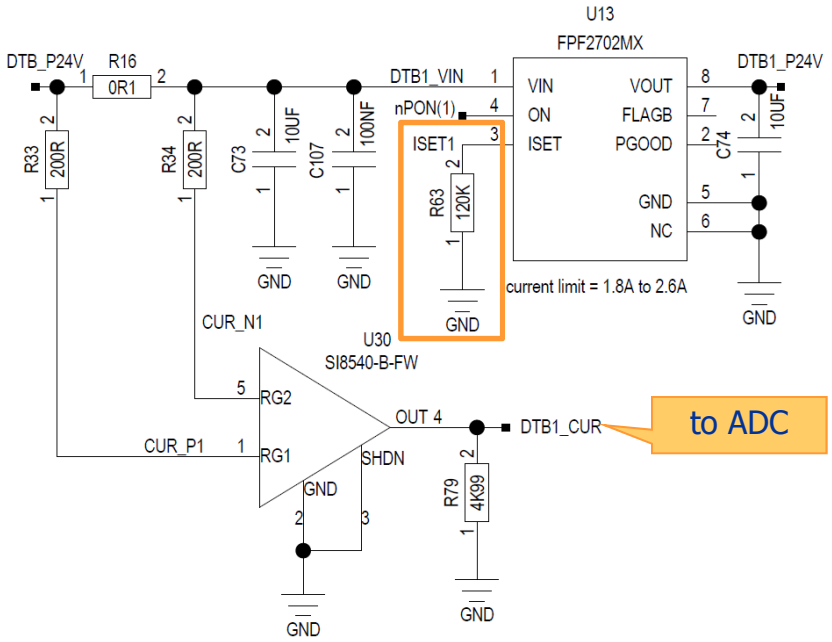
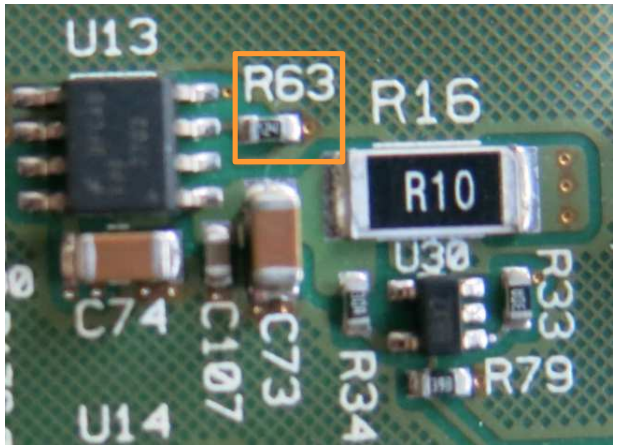


Table 1. R_{SET} Selection Guide

R_{SET} (kΩ)	Current Limit [A]			Tol. (%)
	Min.	Typ.	Max.	
111	2.00	2.50	3.00	20
124	1.79	2.24	2.69	20
147	1.51	1.89	2.27	20
182	1.22	1.52	1.83	20
220	1.01	1.26	1.51	20
274	0.81	1.01	1.22	20
374	0.59	0.74	0.89	20
549	0.40	0.51	0.61	20



CTDB, Power Switch Circuit FPF270x

FPF2700 / FPF2701 / FPF2702 — AccuPower™ 0.4~2A Adjustable Over-Current Protection Load Switches

Features

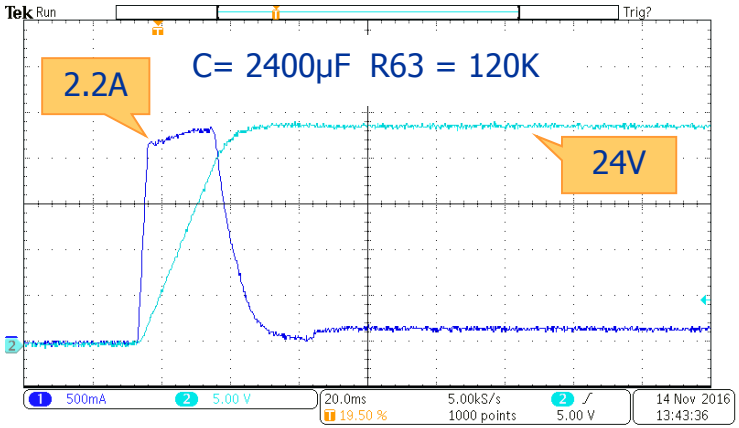
- 2.8V to 36V Input Voltage Range
- Typical $R_{DS(ON)}$=88mΩ
- 0.4A to 2A Adjustable Current Limit (Min.)
- Slew Rate Controlled
- ESD Protected, above 2000V HBM
- Thermal Shutdown
- Active LOW Enable
- UVLO Protection
- Power-Good Output

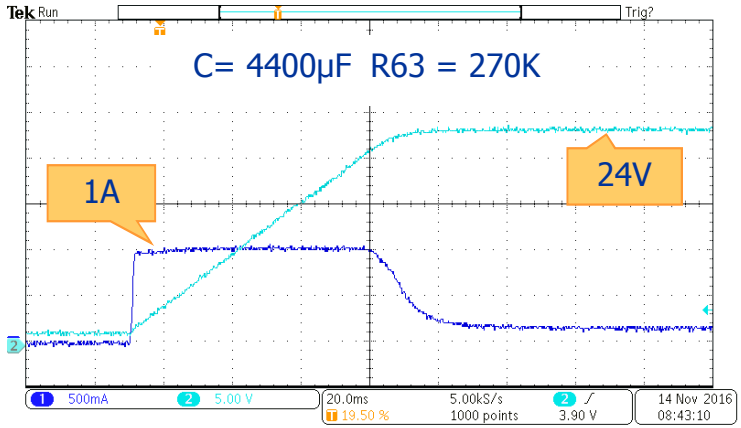
Applications

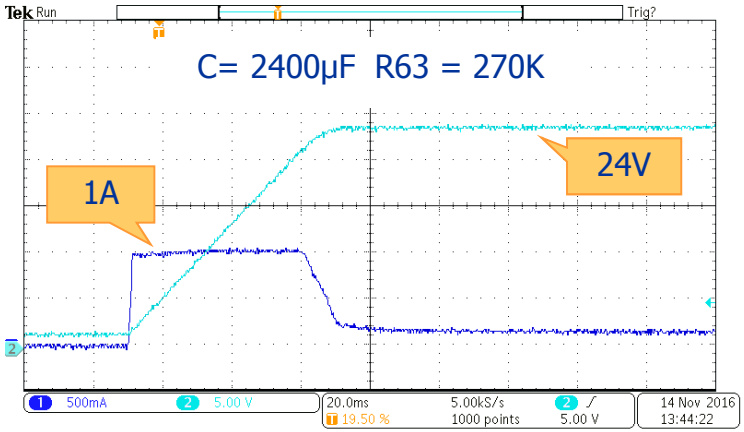
- Motor Drives
- Digital Cameras
- Consumer Electronics
- Industrial
- Computing
- Hard Disk Drives
- Telecom Equipment

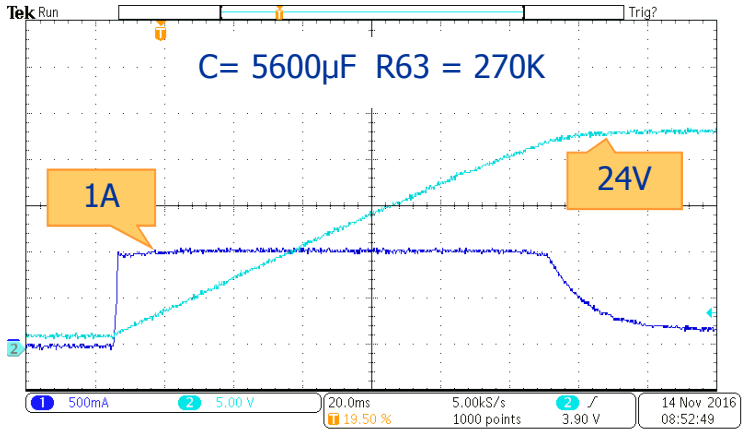
CTDB, Power Switch, Power Ramping

- current values taken with Tektronix current probe TCP0030 (120MHz BW)
- used two current limits, 2.2 A and 1 A, different capacitve loads attached to the L0 test board
- t_on = 30ms … 160ms, needs to be repeated using the real FEB as load





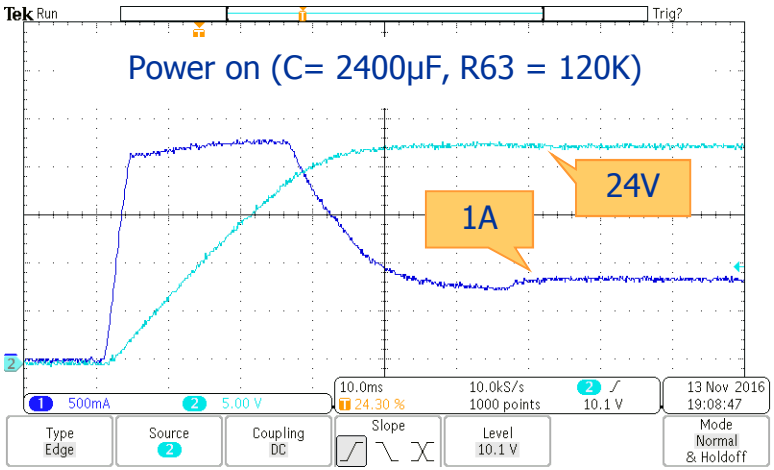


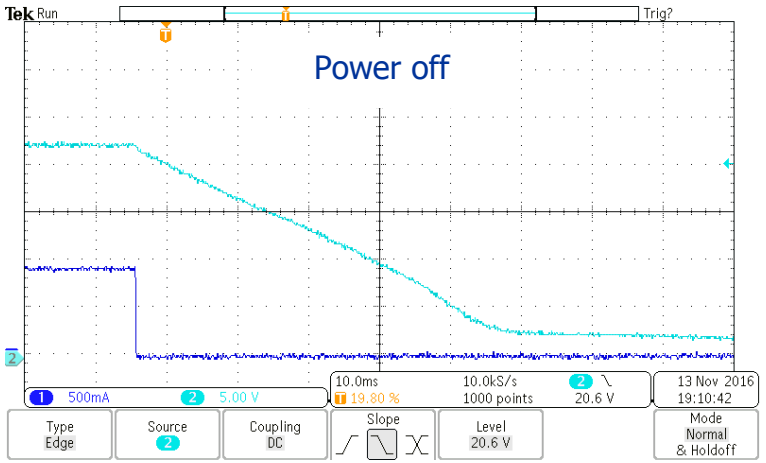


Voltage Loss by Cat.x Cable (3m) and Parts

- overall voltage loss measured from PULS psupply to „FEB" (L0_TB)
- 34 Ω resistor connected to L0_TB to get ~1A load current
- part related loss ~0.5 V @ 1A

	Cat.5e	**Cat.6a**	**Cat.6a**	**Cat.7 - flat**	remark
Order-Nr.	PS5.030.GE	PP6.030.GE	PH6.030.GE	PF7.030.GE	KabelScheune
type	SF/UTP, 4x2xAWG26/7 (7 x 0.16 mm)	S/FTP PIMF, 4x2xAWG26/7 (7 x 0.16 mm)	S/FTP PIMF, 4x2xAWG27/7 (7 x 0.143 mm)	U/FTP, 4x2xAWG30/7 (7 x 0.1 mm)	
cable loss	0.8 V	0.6 V	0.6 V	0.8 V	
overall loss	1.3 V	1.1 V	1.1 V	1.3 V	
remark			length = 3.5 m		





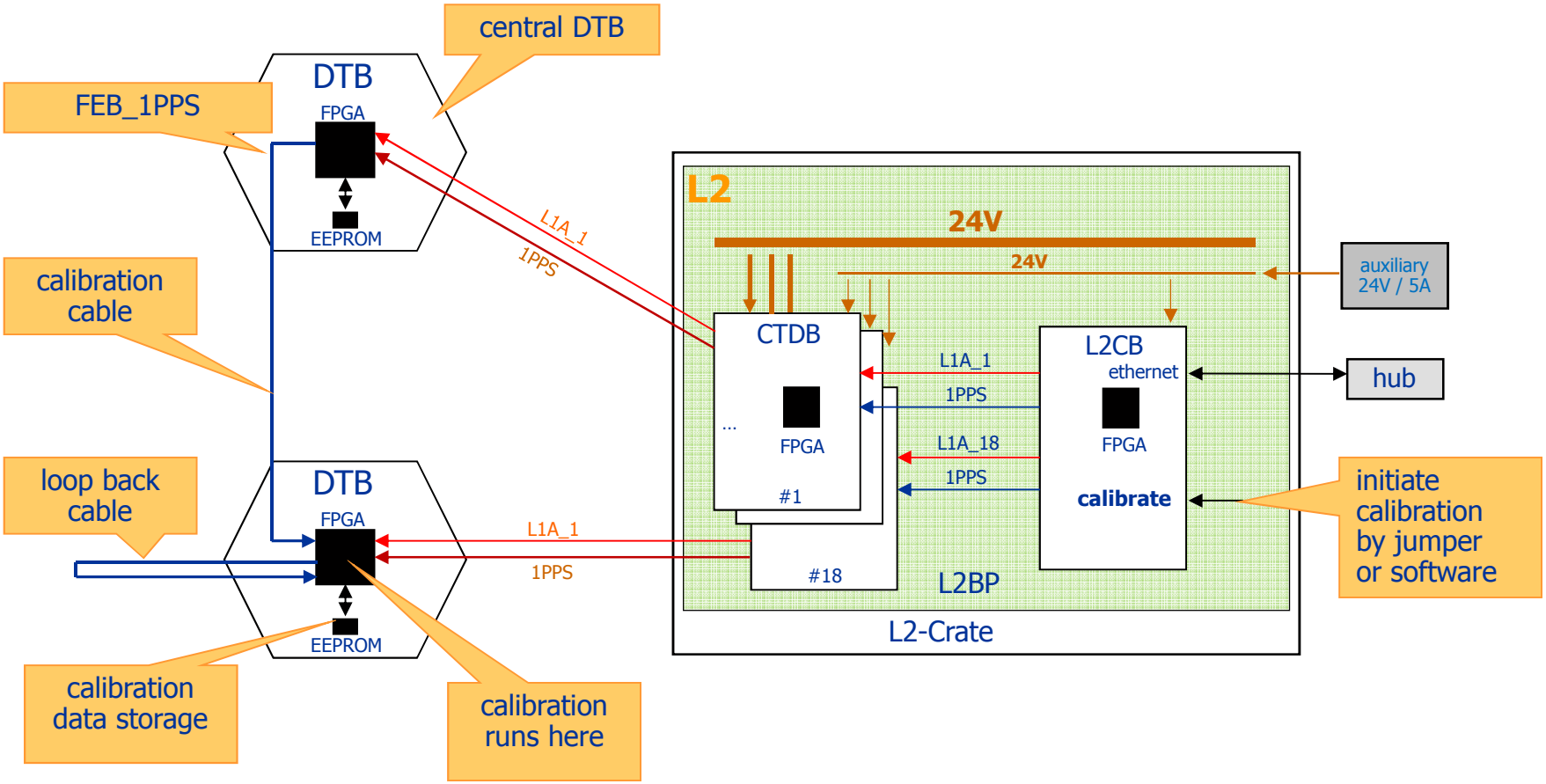
Delay Calibration, 1PPS, L1A, L0

- question: what reference to be used for 1PPS and L1A delay calibration?
- Laser pulser, synchronized by 1PPS ? not possible, because of analog signal delay variation
- easiest is to use the signal arriving at the center cluster for reference
  - after installing all 265 DTBs, do a phase comparison using dedicated calibration inputs on the DTB and the same cable for all, one by one
  - gained calibration values will be stored on each DTB in an EEPROM, to be reloaded after power on
  - can be done by „push button until green light" w/o software interaction
  - can get read back / altered by software as well
- L0, fine delay tuning by firmware or software, if laser available
  - Add a medium delay to one (e.g. central) pixel, AND the L0 with any of the other pixels, tune (in 37 ps steps) until all 37 pixel are in phase
  - also to be stored locally in the EEPROM for power on reload
  - good results (3NN, trigger window set to 2ns) w/o calibration already (FPGA compiler, timing settings are optimized)

=> after power on, the camera is functional immediately

Delay Calibration Procedure, cont.

Using two cables of the same length, L2CB acts as signal generator.



DTB2a, Firmware Status

- Rev. 017, to be tested at Saclay
  - clocked by L2-crate
  - **SPI bus slave**
  - NectarCam pixel numbering schema
  - DTB user manual for DTB register def.
    - two trigger modes, single pixel or 3NN
    - pixel masking
    - trigger window size adjustment down to 1ns
    - all required delay adjustments
- Rev. 018 for standalone tests
  - clocked by local 25 MHz oscillator
  - for more realistic tests with external clock and power via clock line, a single CTDB1 could get set up instead, as „L2" stage (15 ports)

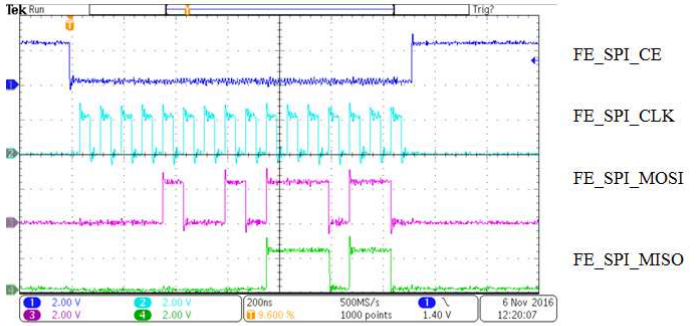


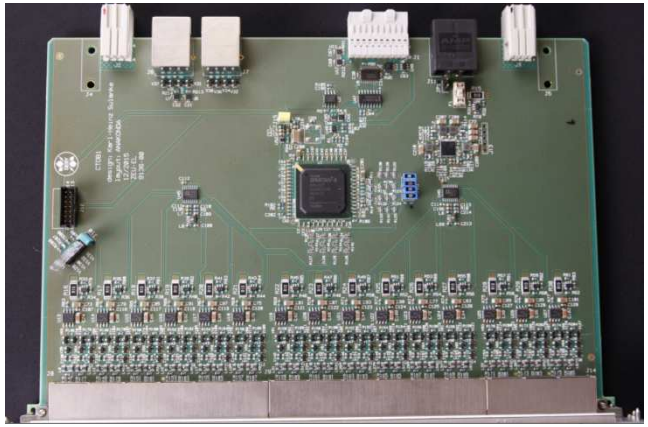
Figure 4: FEB signals, reading data 76h from address 09h at a SPI clock frequency of 12,5 MHz

Address	hex addr.	Name	Usage
0	00	CTRL	Control register
1	01	STAT	Status register
2	02	TRIG_MASK_C	trigger mask for the central clusters
3	03	TRIG_MASK_N	trigger mask for the neighbor cluster
4	04	TRIG_PULS	pulse width for up going (to CTDB) trigger pulse
5	05	TRIG_DTIM	trigger dead time
6	06	TRIG_WIN	trigger window using the leading L0-edges
7	07	PPS_DEL	1PPS input delay fine tuning in steps of 37 ps
8	08	L1A_DEL	L1A trigger (L2) input delay fine tuning in steps of 37 ps
9	09	L0_DEL_SEL	L0 delay select register
10	0A	L0_DEL	L0 delay for the pixel selected by the reg. L0_DEL_SEL
11	0B		Not used (reserved)
..			
125	7D		
126	7E	FW_REVL	Firmware Revision, bits 7..0
127	7F	FW_REVH	Firmware Revision, bits 15..8

Firmware Status, L2CB1, CTDB1

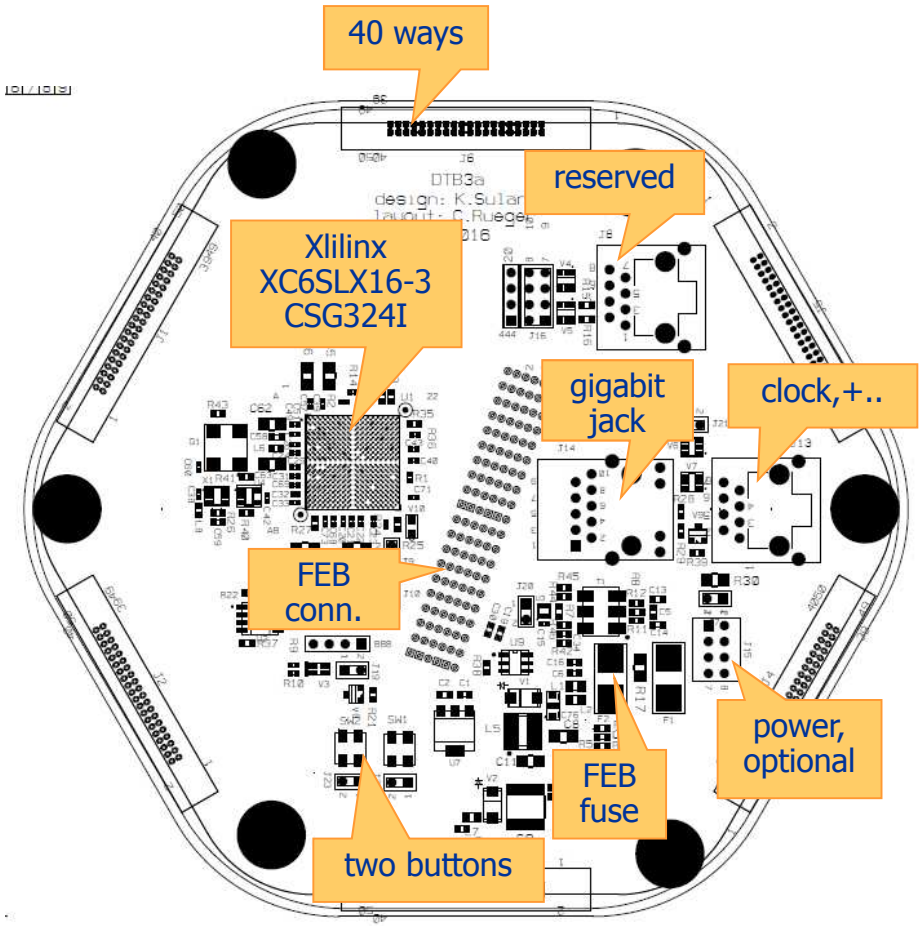
- L2CB1, firmware Rev. 002
  - clock generation from 10 Mhz (TIB)
  - clock and 1PPS distribution
  - L2 trigger generation from 265 L1s
  - camera trigger distribution
  - **SPI master control**
  - preliminary user manual written (includes CTDB1 registers)
- CTDB1, firmware Rev. 002
  - clock and trigger distribution
  - **SPI slave control**
  - SPI address by slot position (no jumper setting needed)
  - power on / off by register write (or jumper)
  - FEB current measurement not yet available
    - almost done

=> remote FEB power on / off via L2CB1-RS232 (or ethernet) has been successfully tested



DTB2a -> DTB3

- presently in PCB design phase
- FEB connector rotated
- FPGA changed to smaller package
  - 324 pin 0.8 mm pitch BGA
  - 37 pixel (was up to 49 before)
- FPGA, two mounting options
  - XC6SLX16 or XC6SLX25
- 50 way connector -> 40 way
- two push buttons / connectors for calibration
- separate EEPROM for calibration data
- second fuse, for the FEB
- global LED-disable per jumper or register
- most critical part delivered already
  - vertical gigabit ethernet conn.
- DTB3 will be available January 2017



DT Costs

- 1000 DTBs assumed
- driven by the DTB
- L1 (DTB) ~ 200 €
- L2 ~5000 €
- Sum = 58000 €
- per pixel ~ 31 €

	A	B	C	D	E	F	G	H
1	Baut Posit	Benennung / Type / W	Hersteller	Hersteller-Nr.	Einze stüc	Menge /VE	Price if 1000 pcs.	Colu
2	C62,C63, C64,C65, C66,C67, C8	Capacitor 1206 47uF 10V 20%	MURATA	GRM31CR61A476ME15	0,26	7	1,82	
3	C9	Capacitor 2220 10uF 50V 10%	KEMET	C2220X106K5RAC	1,10	1	1,10	
4	F1	Misc SERIE 453 T-1A 1A	LITTELFUSE	0154001.DR	1,53	1	1,53	
5	J1,J2,J3,J4 ,J5,J6	Connector EHF-120-01-L-D Gold-Plated 1.27 mm Terminale block 0°	Harwin	M50-3552042	1,92	6	11,52	
6	J11,J12	Connector 6469025-1 Gold-Plated Header Shielded z-pack Bus-Kontaktblock High Speed	TE CONNECTIVITY	6469025-1	5,60	2	11,20	
7	J13	Connector CAT5 Gold-Plated Female Shielded Straight	MOLEX	85508-5001	2,24	1	2,24	
8	J14	Connector 1840417-4 Gold-Plated Phosphor Bronze vertical	TE CONNECTIVITY	1840417-4	5,00	1	5,00	
9	J17	Connector 87832-1420 2 mm Male Straight Zweireihig	MOLEX	87832-1420	0,82	1	0,82	
10	L2	Inductor 10uH Ferrite Inductor Power Magnetic Shielded	WUERTH ELEKTRONIK	74488430100	1,44	1	1,44	
11	L5	Inductor 74408943022 High Q factor Inductor High Current Low DC Resistance Power 2,2uH	WUERTH ELEKTRONIK	74408943022	1,60	1	1,60	
12	L1,L2,L3, L4,L7	ferrite 0805, 1A, 0R3, 1K	WUERTH ELEKTRONIK	742792096	0,14	5	0,70	
13	U1	IC XC6SLX16-3CSG324I FPGA	XILINX	XC6SLX16-3CSG324I	**37,17**	1	37,17	
14	U2	IC AT45DB081D-SU Flash Memory FLASH Serial	ATMEL	AT45DB081D-SSU	1,60	1	1,60	
15	U3	IC ADCMP604BKSZ-R2 Comparator LVDS Fast	ANALOG DEVICES	ADCMP604BKSZ-R2	2,65	1	2,65	
16	U5	IC TMP05BRTZ Temperature Sensor	ANALOG DEVICES	TMP05BRTZ	1,17	1	1,17	
17	U6	IC LT3680EMSE#PBF Regulator Supply Positive	LINEAR TECHNOLOGY	LT3680EMSE#PBF	5,06	1	5,06	
18	U7	IC MCP1826S LDO Regulator Voltage Regulator, Positive, 2.5V	MICROCHIP	MCP1826S-2502E/DB	0,52	1	0,52	
19	U8	IC MCP1826S LDO Regulator Voltage Regulator, Positive, 1.2V	MICROCHIP	MCP1826S-1202E/DB	0,52	1	0,52	
20	V1,V2	Diode DO-214AC MBRA340T3G 40V	ON SEMICONDUCTOR	MBRA340T3G	0,16	2	0,32	
21	V3,V4,V5, V6,V7,V8, V9	Diode SOT323 BAT54SW 30V	NXP Semiconductors	BAT54SW	0,33	7	2,31	
22	U9	IC DS2431P+ EEPROM ,1KB,1-WIRE,TSOC6	MAXIM	DS2431P+	0,70	1	0,70	
23	C76	EMI filter, 1206, 22nF, 2A, 50V	MURATA	NFM3DPC223R1H3L	0,23	1	0,23	
24	SW1,SW2	push button switch, SMD	Bourns	7914J-1-000E	0,40	2	0,80	
25	J1..J6, cable connector	socket, IDC, 1.27MM, 40 Way	Harwin	M50-3302042	1,94	6	11,64	
26	cable	flat cable, 30 AWG, 7x0.1mm, 50 way, 122 ohm, 0.635mm, PVC	3M	3754-40	0,21	3	0,63	
27	J15, cable connector	socket, 2x4 way, crimp, HE14 series	TE CONNECTIVITY	281839-4	0,27	1	0,27	
28	J15, crimp contacts	crimp contacts, AWG 24-28, 0.8...1.5mm,	TE CONNECTIVITY	182734-2	0,14	4	0,56	
29		cable Cat.6a, 3m	KabelScheune	PP6.030.GE	4,19	1	4,19	
30	PCB	PCB, 8 layers	Contag	8884-00	**66,00**	1	66,00	
31	assembly				**20,00**	1	20,00	
32					L1	sum	**195,31**	
33					L2	sum	**4800,00**	
34						**overall sum**	**56557,15**	
35						**sum / pixel**	**30,49**	

Digital Trigger, Pros and Cons

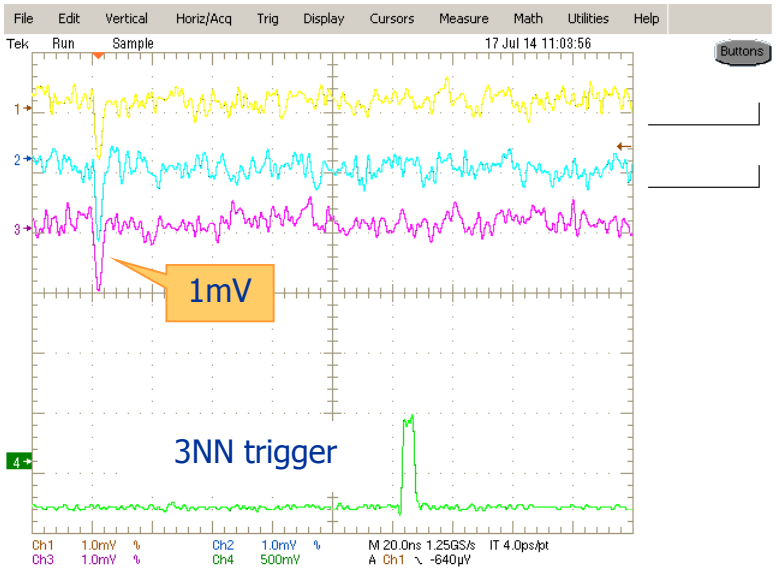
- Cons:
  - more cabling + L2 Crate required
  - more weight (~36 Kg)
  - ~1V loss, if powered via L2 crate
- Pros:
  - overall structure, on the FEB only a very short (noise sensitive) analog path needed, digital signals routing directly after analog frontend
  - can be completely build up (including L0 stage) by off the shelf parts
  - flexible, L1 and L2 based on FPGAs, all 265 L1s handled by a single powerful L2-FPGA (topological trigger)
  - small calibration effort, local storage of calibration data (still has to be demonstrated)
  - trigger functional after power on , „turn key operation"
  - L1, L2 remote firmware update capability
  - adjustable trigger window, minimum is 1ns
  - time distributed trigger (still has to be demonstrated)
  - FEB current (health~) monitoring
  - dedicated FEB power on / off / reset, power ramping
  - copper bars + power wires and solid state relays not needed in the camera back

Analog vs. Digital Trigger, Down Selection

- there seem to be no big differences in price and power consumption
- choice by performance NOT by simulation
- MiniCam or QM, if both passing the tests, then the real Cam should be used
- Estimated effort to rearrange the camera trigger from analog to digital is ~ 1..2 days (1 technician or engineer, 1 physicist)
- existing projects, e.g. MAGIC, HESS are showing, it takes a while to optimize the trigger performance
- while the hardware is fixed, more or less, there is a lot of headroom for firmware and software improvements

Analog vs. Digital Trigger, Performance Test, e.g.

- Start with the digital trigger, use 3 very weak signals by pulsgenerator (or light)
- Find the minimum amplitude, where each is still clearly detectable (L0 discriminator)
- Check the 3NN for 100 % trigger rate for different pixel combinations of 3 clusters
- Shift the signal and record the trigger rate
- Keep the signals amplitude and do the same with the analog trigger for comparison



Conclusions

- basic tests did show, all elements of the Digital Trigger perform like expected so far …
- still, a lot of more testing required, using real FEBs + focal planes
- provided, no show stopper being revealed, while testing at Saclay

=> final trigger decision should be driven by the camera performance

Thanks !

Backup Slides

Max. Current over Copper Wires

Strombelastbarkeit (allgemein) für flexible Leitungen die in den vorhergehenden Tabellen nicht vorhanden sind

Die in den nachfolgenden Tabellen angegebenen Werte sind Richtwerte und in vereinfachter Form der DIN VDE 0298 Teil 4 und DIN VDE 0100 Teil 430 entnommen. In Grenzfällen sind die DIN VDE-Bestimmungen zu berücksichtigen.
Es gelten für Industriemaschinen VDE 0113, Teil 1 (EN 60204 Teil 1/IEC 204-1); für Fernmelde- und Informations-Anlagen DIN VDE 0891 Teil 1; für Fernmelde-Luftkabel DIN VDE 0891 Teil 8; für Flachleitungen DIN VDE 0891 Teil 10. Allgemeine Bestimmungen und Empfehlungs-Werte finden Sie in DIN VDE 0298 Teil 2 und Teil 4.

Strombelastbarkeit, ab 1,5 – 120 mm² (bei Gruppe 3 bis 35 mm²) nach DIN VDE 0100 Teil 430 bei

Umgebungs-Temperatur bis 30°C

Nenn-quer-schnitt	Gruppe 1		Gruppe 2		Gruppe 3	
	Cu-Leiter	Absicherung	Cu-Leiter	Absicherung	Cu-Leiter	Absicherung
mm²	A	A	A	A	A	A
0,05	1	–	1	–	2	–
0,14	2	–	2	–	3,5	–
0,25	4	–	4,5	–	6	–
0,34	6	–	6	–	9	–
0,5	9	–	9	–	12	–
0,75	12	–	12	10	15	10
1	15	10	15	10	19	16
1,5	18	16	18	16	24	20
2,5	26	25	26	25	32	25
4	34	25	34	25	42	35
6	44	35	44	35	54	50
10	61	50	61	50	73	63
16	82	80	82	63	98	80
25	108	100	108	80	129	100
35	135	125	135	100	158	125
50	168	160	168	125	198	160

Gruppe 1 Eine oder mehrere in Rohr verlegte einadrige Leitungen, z.B. PVC-Aderleitungen H 03V../H 05V../H 07V.. nach DIN VDE 0281.

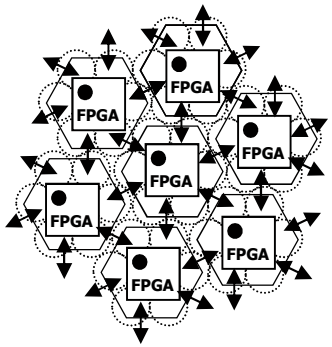
Gruppe 2 Mehraderleitungen, z.B. Mantelleitungen, bewegliche Leitungen, Rohrdrähte in offenen oder belüfteten Kanälen.

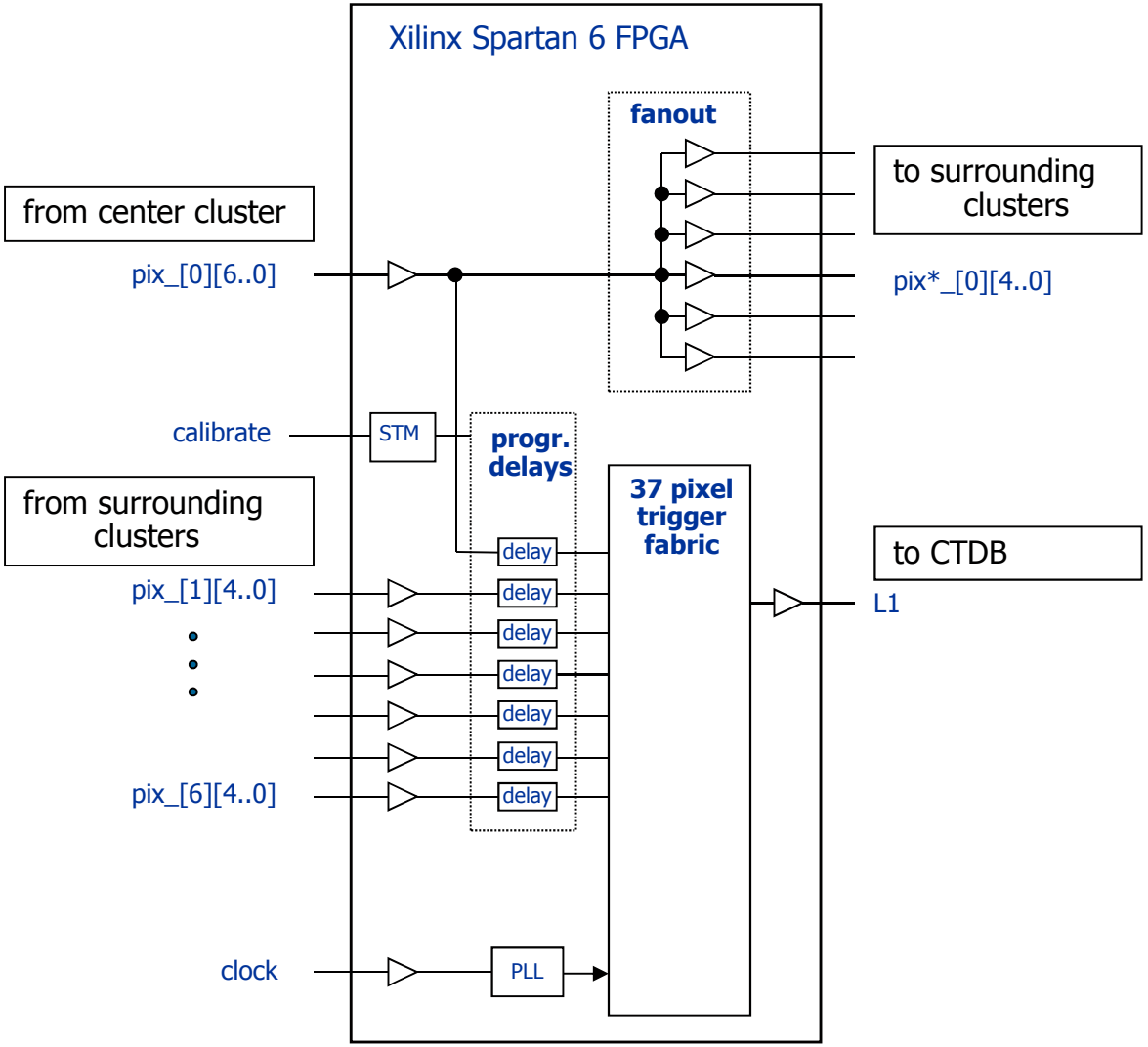
Max. Current over PCBs

Trace width (mm)	Max. current at bei 17,5 µm in (A)	Max. current at bei 35 µm in (A)
0,1	0,25	0,5
0,2	0,5	1
0,5	1,2	2
1	2	4
1,5	3	5
2	3,3	6
4	6	10
6	8,3	14
10	12	21

Drill (via) diameter	Max. current
0,2	1
0,3	2
0,4	2,5
0,5	3,0
0,6	3,5
0,7	4
0,8	5

L1, DTB-FPGA's Functionality

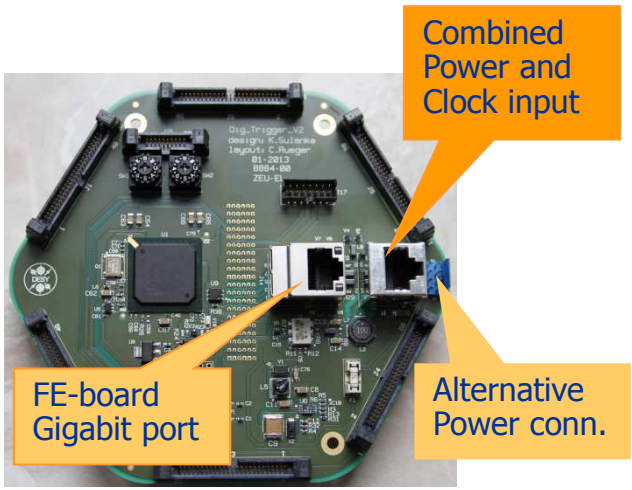


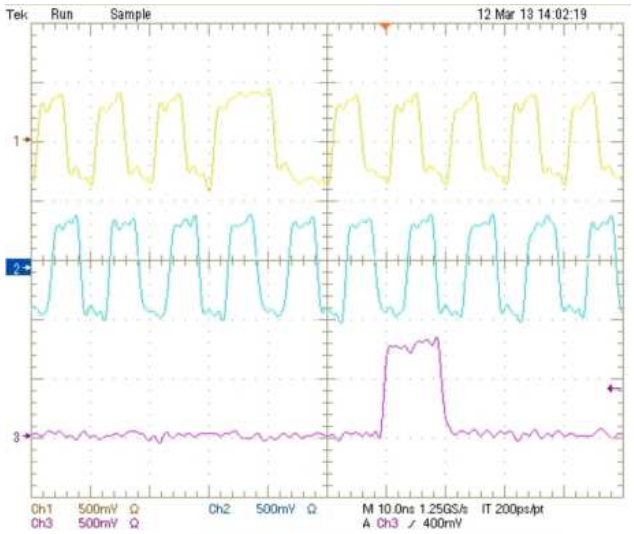


Combined Power and Clock Input

- 24V, clock, and PPS over a single wire pair
- requires a single cat6 cable per cluster only (+ gigabit ethernet cable)
- Current spikes of 0.8 A did not influence the (recovered) clock quality

Cat6 - Wire Pair	signal
1	1PPS_CLK_24V
2	BUSY
3	Trig_L1_out
4	Trig_L2_in





Cabling, Power Consumption and Cooling

- Cat6 Cabling
  - DTBs <-> CTDB (L2-crate), standard round (d=6mm) or flat, 265 x shielded CAT6
    - Same Length up to 5 m, but as short as possible preferred. 3 m is o.k. ?
    - Cabling splitted into 2 branches, left / right with L2-crate on top or bottom ?
    - If two branches, cable duct width ~ 40 cm2
  - L2CB (L2-crate) <-> TIB, standard round (d=6mm) 2 x shielded CAT6, .. 5m
  - L2CB (L2-crate) <-> central cluster, standard round (d=6mm) 1 x shielded CAT6, .. 5m
  - L2CB (L2-crate) <-> ethernet hub, standard round (d=6mm) 1 x shielded CAT6, .. 5m
- 24V Power cabling
  - DTBs, same like for the ATBs, or the CAT6 cable, used for clock, pps, trigger,...
  - L2-crate, 2 x copper, 0.5 ... 1 mm2, like used for other peripherals
- Max. L2-crate Power consumption
  - 60 W estimated (~3 W per CTDB)
- Cooling, L2-Crate
  - Additional cooling not required
  - Convection must be possible