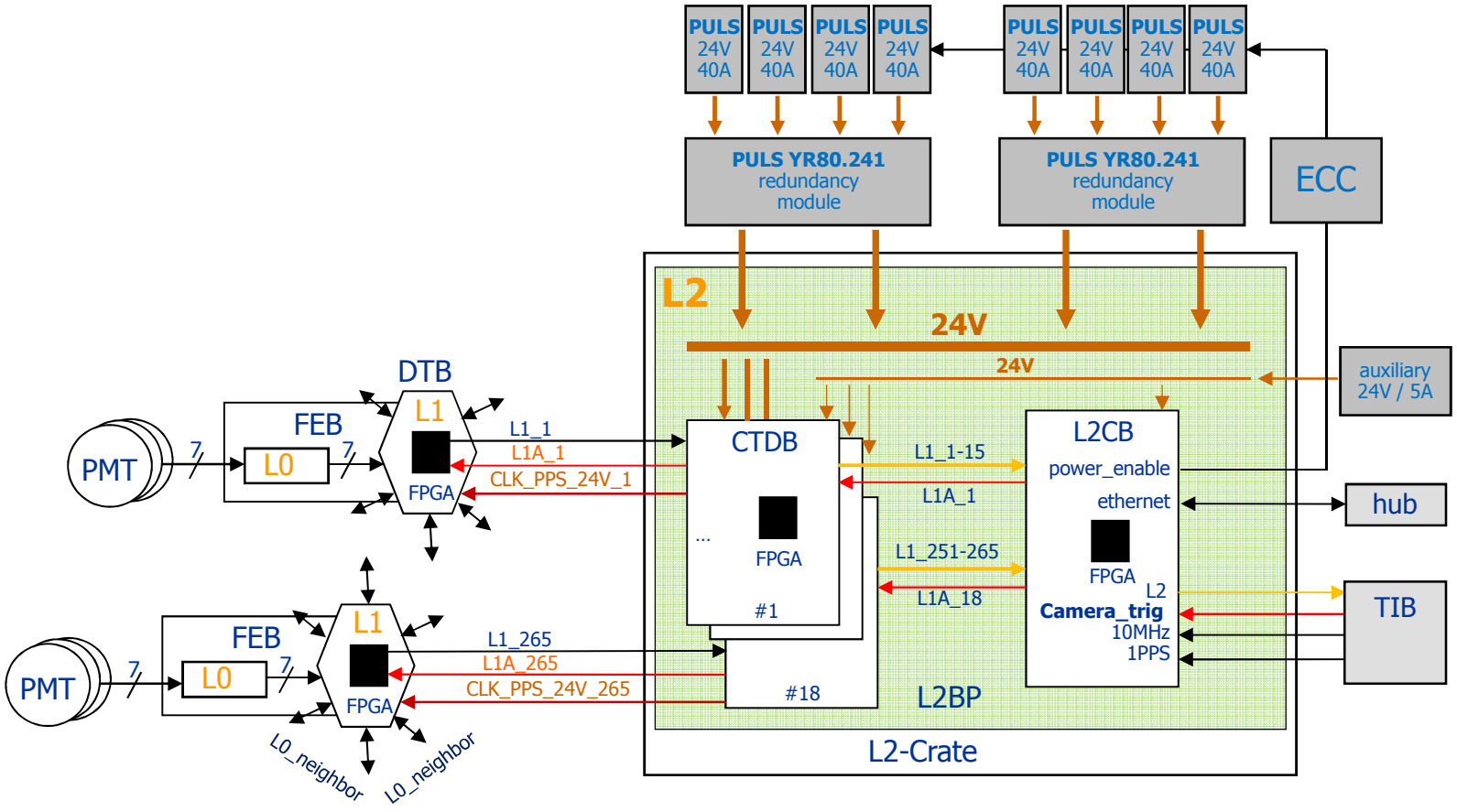
Digital Trigger Calibration & Next Steps, August 2017

- trigger and time calibration
- planned DTB4 firmware extensions
- digital trigger crate using OPCUA protocol
- power supply and choice of cables
- mechanics
- DTB4 production status

Trigger & Power Topology



Calibration

- digital trigger works w/o calibration already
- for improved performance, items to calibrate
  1. 1PPS / clock delay
  2. L0 delay
  3. L1 up delay
  4. L1 down delay
- upper shown calibration sequence should be used
  - digital trigger is a synchronous system
  - best performance, when all clocks are in phase
- L1 up delay has to be calibrated at the L2CB, all other at the DTB (via FEB access)

1PPS & Clock Accuracy w/o Calibration

- 1PPS & Clock L2-Crate Channel to Channel Skew measurement
- measured the 1PPS and clock deviation of 45 channels (3 CTDBs)
- used scope, the Tektronix MDO3104, 1Ghz, 5GS/s, not very accurate for such small skews
- two DTB4s, one with fixed connection to L2-crate slot 1, channel 1, the other plugged to the remaining channels
- signal TIMEPPS probed next to the FEB connector
- typical values, see left side
- maximum skew found was **140 ps**

slot1	0.00
	-30.00
	-25.00
	-15.00
	10.00
	-50.00
	0.00
	-50.00
	-85.00
	-80.00
	-50.00
	-70.00
	-90.00
	-80.00
	-80.00
slot2	-80.00
	-80.00
	-65.00
	0.00
	-60.00
	-85.00
	-70.00
	-100.00
	-70.00
	-95.00
	-70.00
	-80.00
	-95.00
	-130.00
	-140.00
slot3	-140.00
	-95.00
	-100.00

1PPS & Clock Calibration

- should be the first step of the calibration procedure, several methods possible
- delay is not significantly dependent on temperature and time
- Method 0, do nothing, rely on the built in accuracy of the 1PPS / clock distribution system
- Method 1, using the LED / laser source, triggered by 1PPS
  - using TDCs (DTB4 firmware, not yet implemented), take L0 time stamps
  - adjust the 1PPS delay accordingly by software
  - pros: fully automated procedure
  - contra: uncertainty of the L0 delay (PMT, L0-ASIC, …)
- Method 2, step by step, 1PPS phase comparison and delay adjustment by DTB4 firmware
  - one time calibration after Digital Trigger installation
  - central FEB as reference
  - needs 264 x plugging of a test cable and pressing a button on the DTB4
  - implemented in firmware, successfully simulated and tested
  - read back and storage of the gained delay value by software
    - local storage / power on reload (EEPROM) by firmware also possible
  - pros: accurate, half automated
  - contra: manual interaction needed

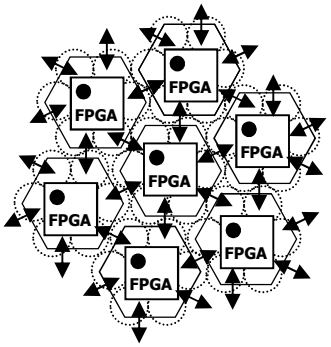
1PPS & Clock Calibration, cont.

- Method 3, step by step 1PPS scope based phase comparison and delay adjustment by software
  - one time calibration after Digital Trigger installation
  - central FEB as reference, using onboard test points + good scope with diff probes
  - read back and storage of the gained delay value by software
  - pros: very accurate
  - contra: manual interaction needed

➢ Method 1 (TDC based) will be the preferred one

- at the camera assembly phase method 2 or 3 could be used
- later, in field method 1 for verification

DTB4, L0 Delay Calibration



Xilinx Spartan 6 FPGA

fanout

L0s from center cluster

L0_[0][6..0]

L0s to surrounding clusters

L0_[0][4..0]

progr. delays

trigger mask

37 pixel trigger fabric

L0s from surrounding clusters

L0_[1][4..0]

delay

delay

delay

delay

delay

delay

L0_[6][4..0]

to CTDB

L1

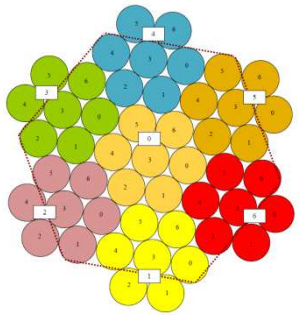
trigger = 2_of_37

SPI

register block

clock

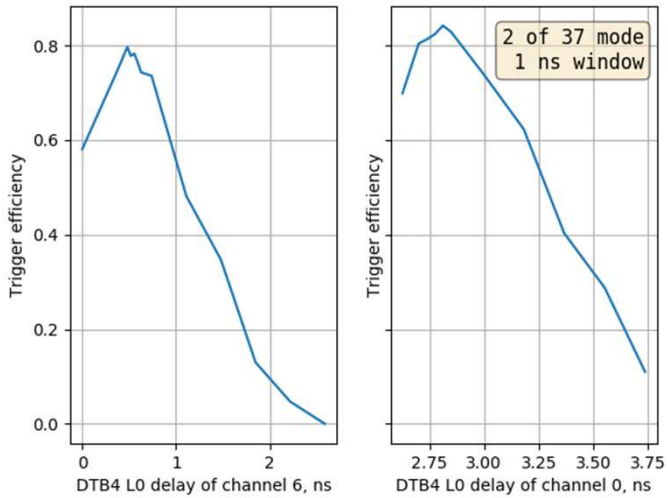
PLL



37 pixel map

DTB4, L0 Delay Calibration cont.

- trigger algorithm switched to AND_2_of_37 (ctrl-reg.)
  - triggers if the central pixel AND one of the selected surrounding are seeing light at the same time
- trigger window set to 1ns
- trigger mask set, to select the pixel to be calibrated, 1 of 36
- uniform LED / laser source with known flasher frequency, e.g. 1KHz
- software adjusts the L0 delay for **max. trigger rate**
- for 1ns trigger window, 100 % trigger efficiency is not possible due to the asyncronous sampling of the L0 signals with 1GSPS
- examples see below, diagrams by Patrick Sizun



L1 Delay Calibration

- up delay
  - main skew comes from the L2CB FPGA internal delays
  - compensation by setting 265 individual delays in steps of 37ps
  - possible with latest L2CB firmware
    - Xilinx compiler provides a delay table after timing analysis
    - can be used to compensate the delays by software
    - 90 channels measured, max-min = 0.84ns after correction
  - or, calibration using the LED / Laser source
    - trigger algorithm switched to AND_2_of_265
    - delay calibration for maximum trigger rate (like L0 delay calibration)
    - not yet implemented
- down delay
  - according to the latest measurements negligible
    - 90 channels measured, max-min = 0.57 ns (no correction)
  - if required, at DTB4 the L1A delay can be adjusted, as a second step
  - for automated procedure TDCs are needed
    - not yet implemented

Planned DTB4 Firmware Extensions

- L1 scaler
  - 16 bit binary counter (0 .. 65,535 KHz), updated every second (by 1PPS or local clock source)
  - when overflow, counter stays at max value (0xFFFF)
  - means two additional 8 bit registers, accessible by SPI
- additional trigger schema, 1_of_37
  - verification of the connection to neighbor clusters
- BUSY issue, observed by Patrick:

  „when using a TIB firmware which did not handle the BUSY signal, we noticed that the FEB did not take its own BUSY into account either but buffers the L1A and treats them later...”
  - implementation of L1A blocking when BUSY is active
  - can be programmable (CTRL-reg. bit)
- TDCs for L0 time stamping (e.g. central pixel)
  - useful for 1PPS delay calibration

Digital Trigger Crate using OPCUA protocol

- will be supported by DESY Zeuthen Computing Department and Electronics Group
- OPCUA implementation
  - by David Melkumyan (Computing Department)
  - support also by Marek Penno (EL-Group)
- due to vacations, details will be discussed on September 4th

Power Supply

- L2 crate, 24V auxiliary power supply
  - measured: max. continous current < 2.5A (fully populated crate)
  - power supply **CT5.241** would fit into the back of the L2-crate
    - 380-480V 2 phase input
    - negligible low inrush current
    - efficiency up to 90.4%
    - 24 V/DC 5 A output
    - WxHxD = 40 x 124 x117mm
    - weight = 500g

- L2CB will get a small piggy back board and a new front plate
  - relay to enable power on / off of the FEB power supplies by ECC
  - PULS power supply enable („Shut-Down") input could be used
  - can be available end of September
- possible power on sequence (power off vice versa)
  1. ECC switches L2 crates auxiliary power supply on
  2. L2CB FPGA, once loaded, enables ECC switching of the FEB power supplies
  3. ECC switches FEB power supplies on
- details to be discussed with Julie and Scott

Cabling, DTB4 to L2-Crate,

- any of the types or similar (see next slide) is fine with me
- the flat ones might be easier to handle
- the round ones provide more headroom for the max. current and seem to be more robust

➢ lets use the round ones

Shielded Cat.x Cables, Comparison

calculated values based on:

cable length = 3 m

E-Cu, spec. resistance = 0.0172 Ω/mm2 x m

max. current density = 10 A / mm2

	Cat.5e	**Cat.6a**	**Cat.6a**	**Cat.7 - flat**	remark
Order-Nr.	PS5.030.GE	PP6.030.GE	PH6.030.GE	PF7.030.GE	KabelScheune
type	SF/UTP, 4x2xAWG26/7 (7 x 0.16 mm)	S/FTP PIMF, 4x2xAWG26/7 (7 x 0.16 mm)	S/FTP PIMF, 4x2xAWG27/7 (7 x 0.143 mm)	U/FTP, 4x2xAWG30/7 (7 x 0.1 mm)	
weight	81 g	114 g	127 g	103 g	
diameter	5.4 mm	6.5 mm	6.2 mm	7.8 x 2.7 mm	
cross section	22 mm2	33.2 mm2	30.2 mm2	21,1 mm2	
price	1,19 €	4,19 €	6,79 €	4,89 €	
Cu, cross section	0.14 mm2	0.14 mm2	0.112 mm2	0.055 mm2	one wire
resistance	0.184 Ω	0.184 Ω	0.23 Ω	0.47 Ω	one pair
max. cont. current	2.8 A	2.8 A	2.2 A	0.94 A	one pair
power loss	0.12 W	0.12 W	0.15 W	0.3 W	0.8 A
remark		halogen free	halogen free, 3.5 m avail.	gold plated connector shield	

Mechanics

- issue, the vertically arranged L2 crate prevents access to the lowest backplanes
  - would be good to know, how big the overlap is
- theoretically, the depth of the L2 crate can be decreased
  - there is 4.5 cm spare room in the back
    - but then room for the auxiliary power supply is lost
  - more shrinking (..5 cm ?) by redesigning the L2CB (challenging) and the CTDB
- the last one
  - lot of effort and some risk

DTB4 Production Status

- 20 DTB4.1 will be ready this week (DESY Zeuthen workshop)
  - DTB4 -> DTB4.1 by improved soldering mask (outer connector region)
- parts for 60 more DTB4s are ordered and mostly delivered
- next production cycle after PCB / schematic review only

Last slide
Thanks for Your Patience !

Backup Slides

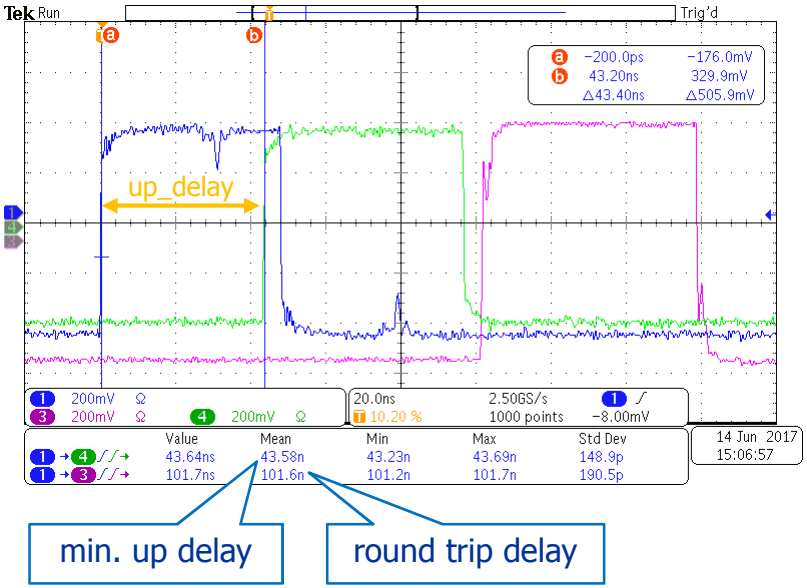
L2CB, Up Delay Measurement

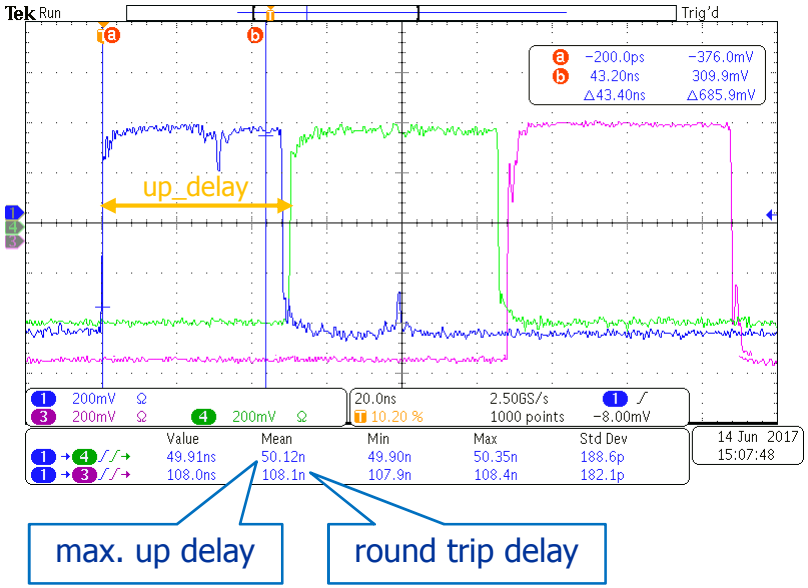
- up delay and round trip measurement with backlooped L2 trigger (instead of TIB), using min. and max. up delay values (software)
- done for **90** L1 trigger channels using the same CTDB, plugged to L2-crate slots 1, 2, 3, 9, 17, 21 (most left, .. middle, ..most right)
- scope channels:

  blue = L1 trigger measured at DTB

  green = L2 trigger measured at L2CB (usually connected to the TIB)

  purple = „L1A", camera trigger, received at the FEB
- up delay, see max-min, => adjustable delay range is 0 to 6.54 ns here





Up / Down Delay Measurement, 90 Channels, Results

- L1 channel to channel skew mainly caused by the L2 FPGA design, the 270 input trigger-OR
- uncorrected up delay max. difference of 4.9 ns is within the max. progr. delay range of 0 .. 6.6ns
  - for combinatorial signals, Xilinx allows max. delay constraining only
  - Xilinx compiler timing analysis can be used for delay correction
    - 270 row table + start up script to load the 270 delay lines
    - prog_delay(i) = (delay_max-delay(i)) * 0.566, i= 1..270
    - result after correction, see table below

Pad to Pad

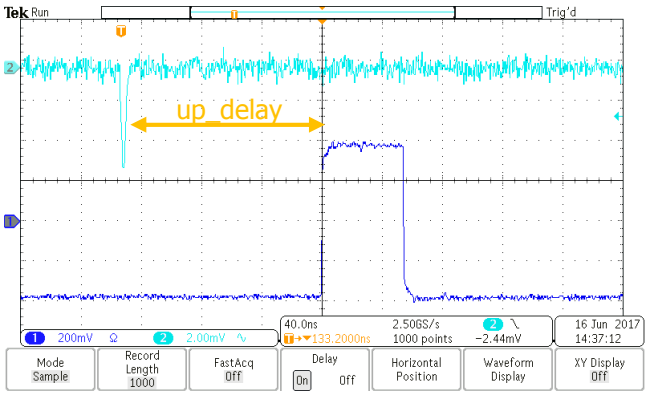
Source Pad	Destination Pad	Delay
L1_TRIG<1>	LVDS_IO_P_3	27.998
L1_TRIG<2>	LVDS_IO_P_3	29.119
L1_TRIG<3>	LVDS_IO_P_3	27.267
L1_TRIG<4>	LVDS_IO_P_3	29.528
L1_TRIG<5>	LVDS_IO_P_3	27.907

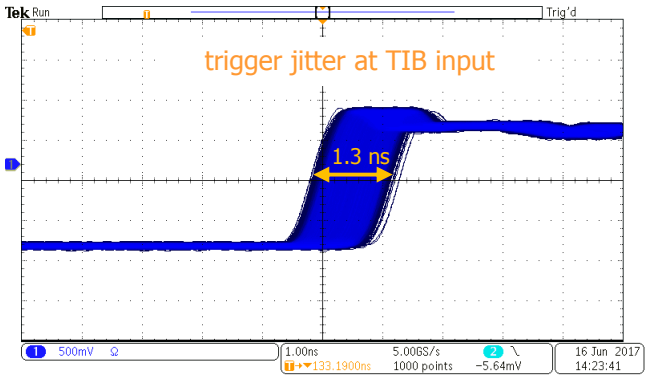
	up delay		down delay		round trip	
	no corr.	after corr.	no corr.		no corr.	after corr.
min	40.96 ns	45.58 ns	58.03 ns		99.17 ns	103.78 ns
max	45.86 ns	46.42 ns	58.60 ns		104.10 ns	104.95 ns
max-min	4.9 ns	**0.84 ns**	**0.57 ns**		4.93 ns	**1.17 ns**

- even better correction is doable, for a fully populated L2-crate, based on the measured individual up delay values for all 270 channels
- alternatively, correction based on the round trip delay measurement at the DTB

Upgoing Trigger, Jitter at TIB Input

- L0_TB + L0-mezzanine as test setup with 3 PMT-like signals of -5mV pk, 3NN trigger
- Scope with delayed triggering on one analog channel
- used the scope display in infinite persistance mode
- ~1.3 ns jitter observed

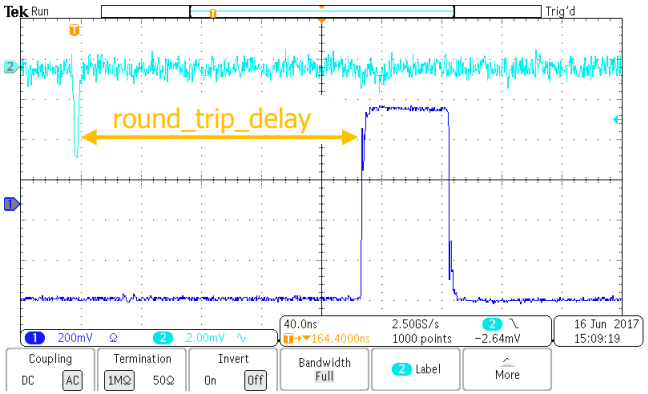


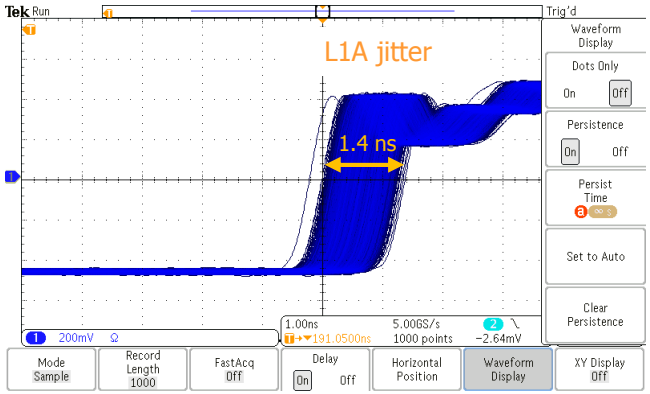


- L0 signal sampling within the DTB FPGA with 1GS/s => jitter must be >= 1ns
- to be considered:
  - L0 ASIC might be behave differently compared to the dig. L0 mezzanine
  - scope trigger jitter

Roundtrip Trigger, L1A Jitter (at FEB)

- same setup like described on previous slide, upgoing trigger backlooped (no TIB avail.)
- roundtrip delay ~190 ns
- ~1.4 ns jitter observed



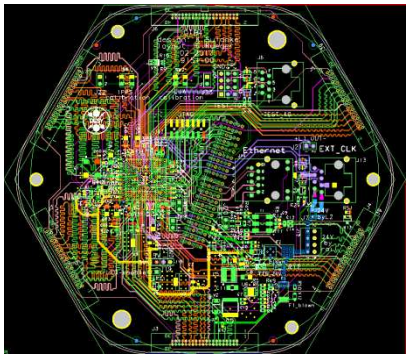


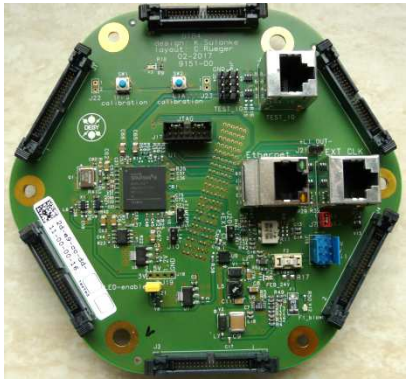
DT Power Consumption and Weight

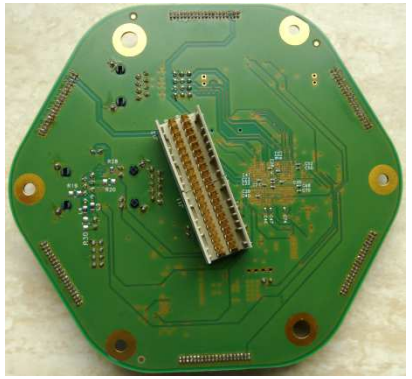
- measured
  - DTB4, 2.6 W 3NN, firmware dependant, estimated max. of 2.8 W
  - L2CB1, 3.2 W
  - CTDB1, 2.9 W
- -> fully populated L2 crate ~ 60 W
- -> overall power consumption ~ 800 W, based on 2.8 W per DTB4
- weight
  - L2-crate : ~9 kg (fully populated)
  - cabling : ~27 kg (Cat.7)
  - DTB4 : 265 x 96 g = 25 kg

DTB, Digital Trigger Backplane

- 4 th revision, 15 pcs. produced and tested
- 8 layer PCB, length & impedance matched diff. lines for precise timing
- 324 pin Spartan 6 FPGA, processes overlapping 37 pixel regions
- interface signals to FEB :
  - 24V, GND
  - 1PPS
  - diff. clock (frequency programmable, not used by NectarFEB)
  - L1A
- interface signals from FEB :
  - L0 (ToT discriminator output signals, by L0 ASIC)
  - BUSY
  - SPI (slow control)

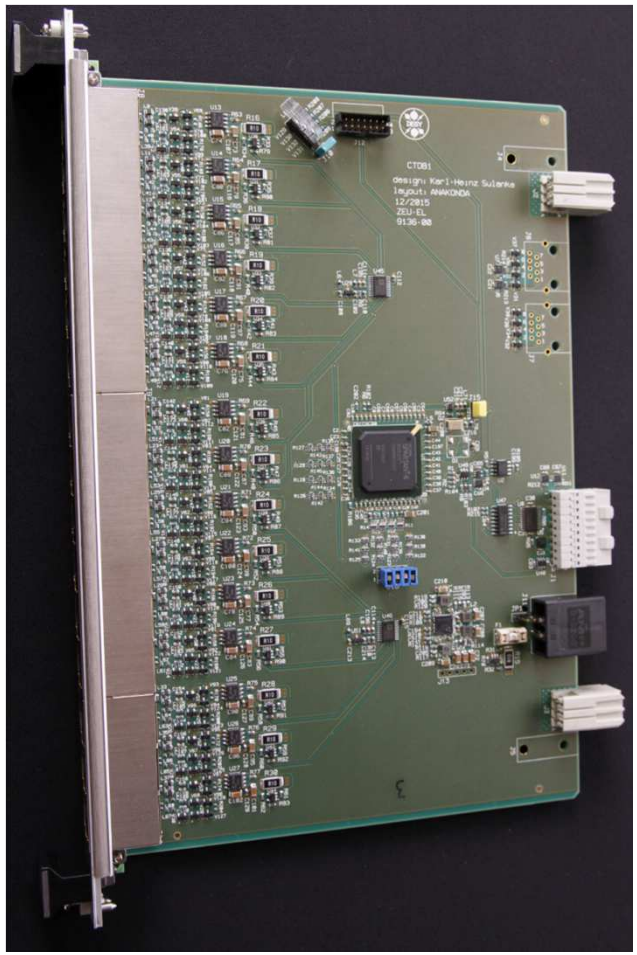






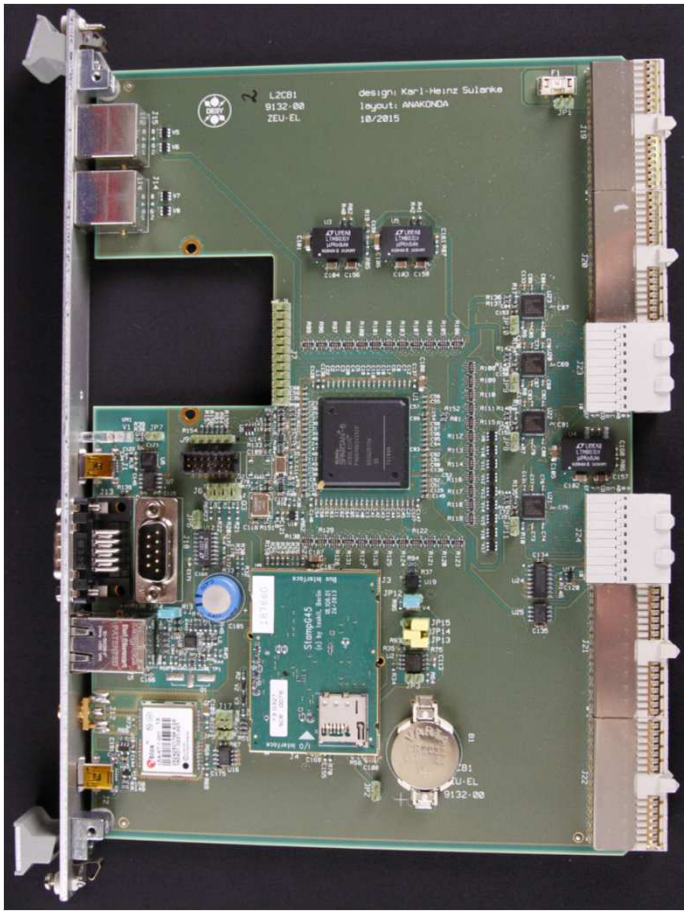
CTDB, Clock & Trigger Distribution Board

- 1st revision, 5 pcs. produced and tested
- 10 layer PCB, length & impedance matched diff.
- Spartan 6 FPGA
- SPI bus interface for slow control with L2CB as master
- standalone mode for test setup of up to 15 FEBs
- 15 channels (RJ45), each for
  - L1 and BUSY reception
  - clock & 1PPS fanout
  - camera trigger fanout
  - FEB power control
    - 24V switch
    - current measurement
    - inrush current limitter



L2CB, L2 Controller Board

- 1st revision, 3 pcs. produced and tested
- 10 layer PCB
- 676 pin Spartan 6 FPGA processes 265 L1s
- TIB interface (camera trigger, BUSY, 10MHz, 1PPS)
- ARM based microcontroller unit „Stamp9G45"
  - Linux
  - ethernet
  - high speed bus connection to the FPGA
  - FPGA, in system firmware update
- SPI bus for CTDB slow control
- TIB-clock and 1PPS fanout / distribution via backplane
- GPS (optional usage)
- extension slot



L2-Crate

- CDTB1 boards slide in easily
  - guide pins not needed
- L2CB1 needs some force (pin count = 560)
- backplane power & signal connectivity checked
  - including SPI bus
- seperate power supply for the L2 would be better (here, both are connected)
  - Should come up before the main psupply
- power rails for the connection of 8 parallel psupplies PULS-QT40.24x
  - or via connector