Digital Trigger Backplane, Firmware

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Approved by	Laboratory

		PLL	Phase Locked Loop
DTB	Digital Trigger Backplane	L1A	L1 accepted
FEB	Frontend Board	MCU	Microcontroller unit
SPI	Serial Peripheral Interface	BGA	Ball Grid Array
FPGA	Field Programmable Gate Array		
TIB	Trigger Interface Board		
CTDB	Clock & Trigger Distribution Board		
1PPS	1 Pulse Per Second		
TOT	Time Over Threshold		

History		
Version	Date	Observation
01	18/05/2020	Draft

Distribution	

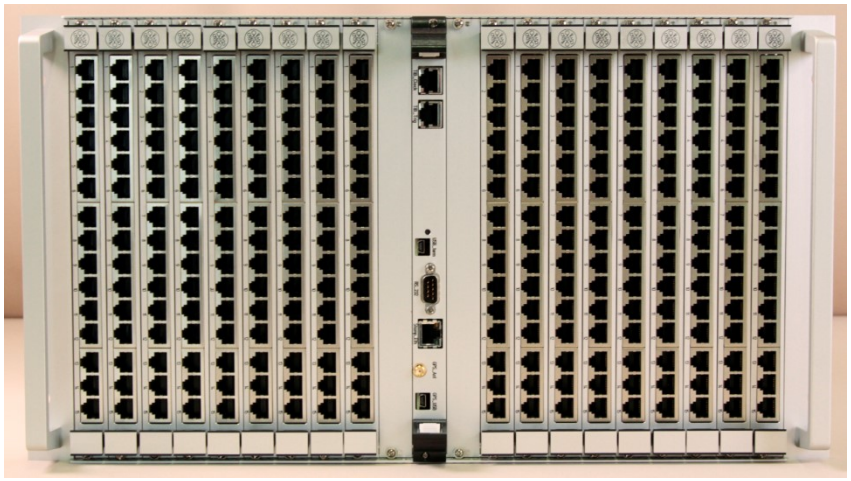
Table of Contents

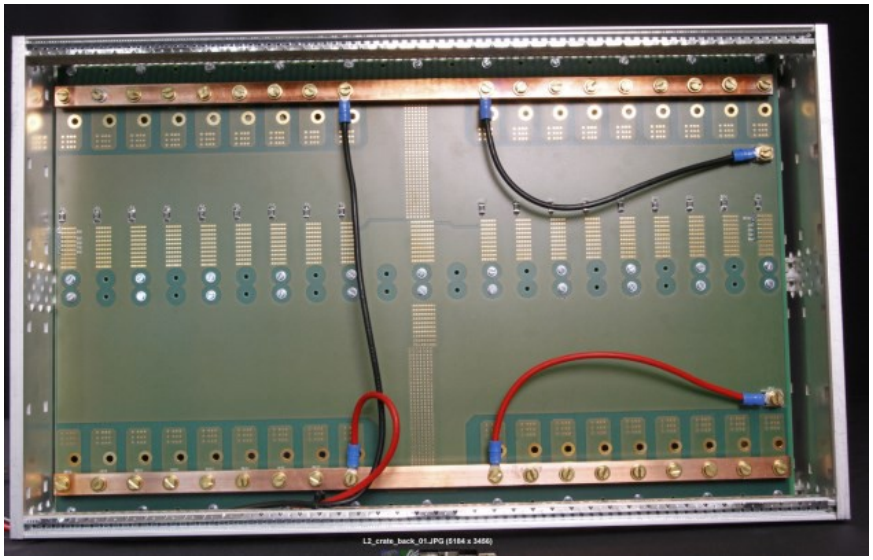
1 Introduction

This document describes the elements of the L2-Crate, with some focus on testing and reliability aspects. The L2-Crate consists out of 5 elements: the crate, the auxiliary power supply, the backplane, 18 CTDBs (Clock & Trigger Distribution Boards) and the L2CB (L2-Controller Board).

2 The Crate

The 6U crate is an off the shelf product of the type Schroff 24563-442, featuring 21 slots (84HP). The card size is 233x160 mm. It fits in any standard 19" frame. So far, 3 crates have been assembled by the DESY workshop.

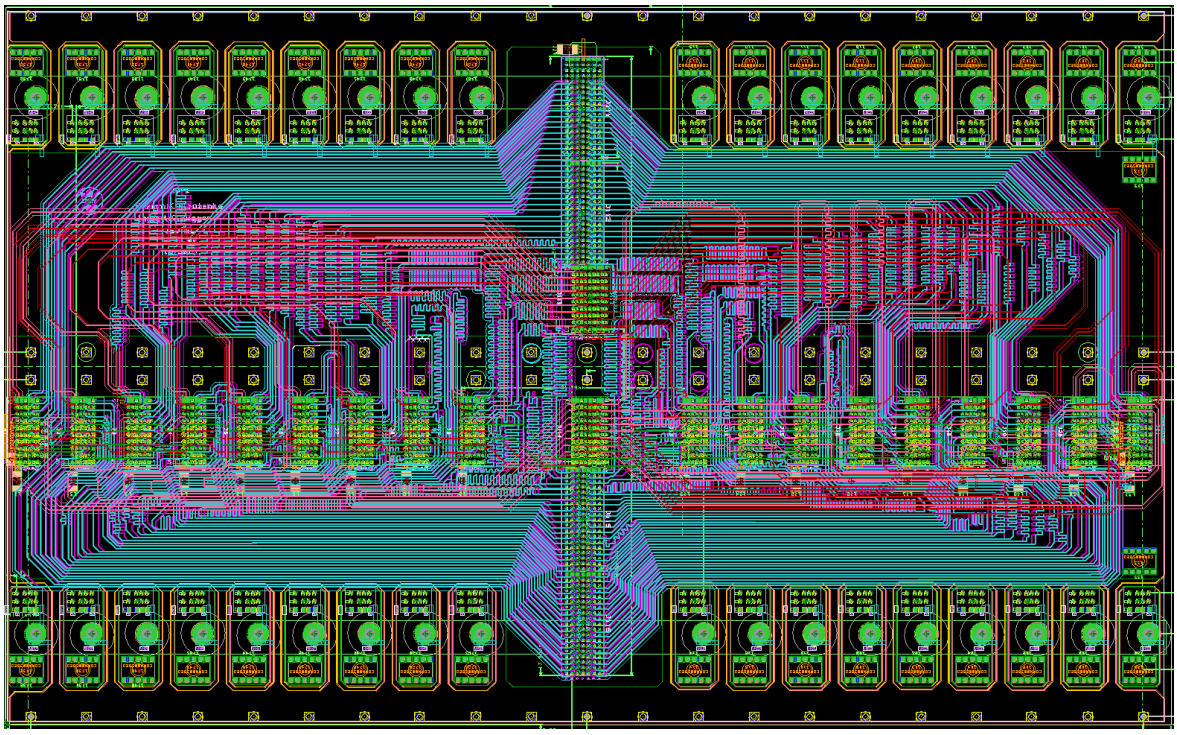




3 The Backplane

The backplane is fully passive. It connects the L2CB with 18 CTDBs. All connectors are of the press-fit type. Only two parts are soldered, a polysilicon fuse and a zero ohm resistor (single bug fix). The drill diameter for the connector holes have been carefully chosen and checked, to guarantee reliable connections. The upper current limit for the CTDB power connectors is 48A. The nominal load is about 12A (15 x 0.75A).

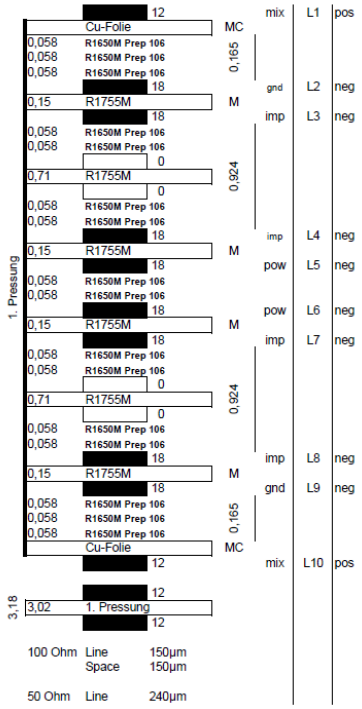
The PCB of the size 330x480x3.18 mm has 10 layers.



All relevant signals lines (clock, PPS, up going trigger, down going trigger) are impedance and length matched. The length matching is in a range of +/-2mm. According to the test protocol of the PCB vendor (andus), the impedance mismatch of the 50 ohm and 100 ohm lines is less than 10%. See below the layer stack and the test protocol. For optimal signal transmission and symmetry the connector pinouts have been chosen in a way to avoid any (!) vias.

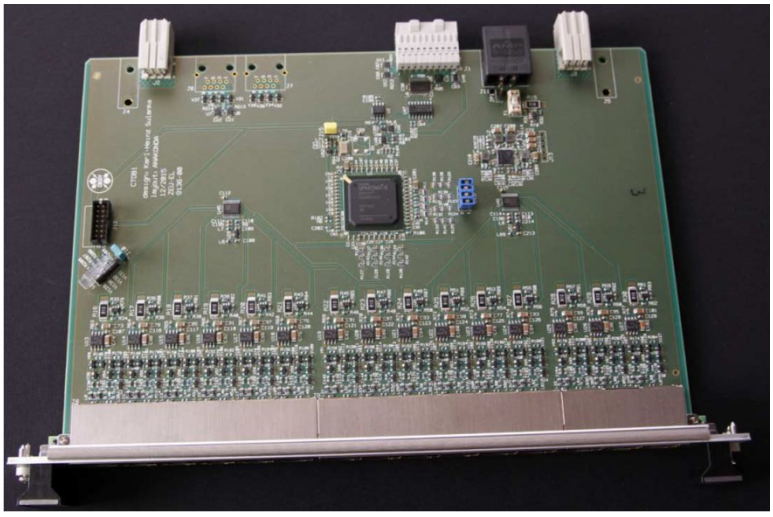
Each slot has its own hard wired CTDB address. This way the CTDB do not need any address jumper, a potential error source. At slot 15 an address bit has been left open accidently. A zero ohm 0603 resistor, soldered to a neighbor GND pin is used to fix this issue.

Format: **330x480**
Stärke/mm: **3,18**
ohne Aufbau: 3,04
Lagenanzahl: 10
-
-
Erstausdruck



Beschreibung	Lage	Mittelwert	Auftragsnummer	Serien No.	Datum
♂ Diff. 100R P1A	L3	93.30	2023304	1	09/12/15
♂ Diff. 100R P2A	L4	93.19	2023304	1	09/12/15
♂ Single P7A	L7	46.39	2023304	1	09/12/15
♂ Single P8A	L8	46.02	2023304	1	09/12/15
♂ Diff. 100R P1B	L1	104.95	2023304	1	09/12/15
♂ Diff. 100R P4B	L10	102.73	2023304	1	09/12/15
♂ Single P5B	L1	47.81	2023304	1	09/12/15
♂ Single P6B	L10	46.78	2023304	1	09/12/15
♂ Diff. 100R P1A	L3	94.91	2023304	2	09/12/15
♂ Diff. 100R P2A	L4	94.54	2023304	2	09/12/15
♂ Single P7A	L7	47.34	2023304	2	09/12/15
♂ Single P8A	L8	46.40	2023304	2	09/12/15
♂ Diff. 100R P1B	L1	101.91	2023304	2	09/12/15
♂ Diff. 100R P4B	L10	102.78	2023304	2	09/12/15
♂ Single P5B	L1	47.55	2023304	2	09/12/15
♂ Single P6B	L10	48.61	2023304	2	09/12/15
♂ Diff. 100R P1A	L3	94.64	2023304	3	09/12/15
♂ Diff. 100R P2A	L4	94.20	2023304	3	09/12/15
♂ Single P7A	L7	46.67	2023304	3	09/12/15
♂ Single P8A	L8	46.62	2023304	3	09/12/15
♂ Diff. 100R P1B	L1	101.69	2023304	3	09/12/15
♂ Diff. 100R P4B	L10	101.68	2023304	3	09/12/15
♂ Single P5B	L1	46.61	2023304	3	09/12/15
♂ Single P6B	L10	46.58	2023304	3	09/12/15
♂ Diff. 100R P1A	L3	93.77	2023304	4	09/12/15
♂ Diff. 100R P2A	L4	94.16	2023304	4	09/12/15
♂ Single P7A	L7	46.91	2023304	4	09/12/15
♂ Single P8A	L8	45.99	2023304	4	09/12/15
♂ Diff. 100R P1B	L1	106.34	2023304	4	09/12/15
♂ Diff. 100R P4B	L10	104.46	2023304	4	09/12/15
♂ Single P5B	L1	46.91	2023304	4	09/12/15
♂ Single P6B	L10	46.63	2023304	4	09/12/15
♂ Diff. 100R P1A	L3	93.60	2023304	5	09/12/15
♂ Diff. 100R P2A	L4	94.51	2023304	5	09/12/15
♂ Single P7A	L7	46.99	2023304	5	09/12/15
♂ Single P8A	L8	46.03	2023304	5	09/12/15
♂ Diff. 100R P1B	L1	103.06	2023304	5	09/12/15
♂ Diff. 100R P4B	L10	100.91	2023304	5	09/12/15
♂ Single P5B	L1	47.65	2023304	5	09/12/15
♂ Single P6B	L10	47.60	2023304	5	09/12/15

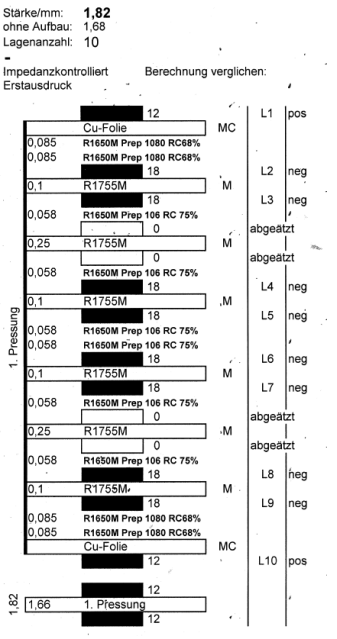
4 The CTDB



The CTDB has 15 identical channels (RJ-45 ports). The main tasks are:

- FEB power distribution, switching
- FEB current monitoring , inrush current limiting and overcurrent protection
- Clock and PPS fanout
- L1 (by FEB + DTB) reception
- BUYS reception
- L1A fanout

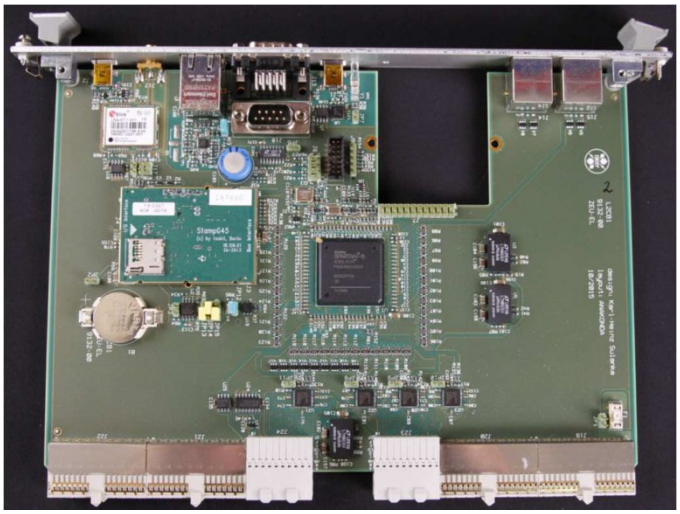
It is a 10 layer PCB with length and impedance matched lines.
See the layer stack and impedance test protocol below:



Beschreibung	Lage	Mittelwert	Auftragsnummer	Serien No.	Datum
Diff. 100R P4	L8	95.15	2029477	6	05/02/18
Single 50R P5	L1	47.18	2029477	6	05/02/18
Single 50R P6	L4	47.25	2029477	6	05/02/18
Single 50R P7	L7	49.28	2029477	6	05/02/18
Single 50R P8	L8	46.55	2029477	6	05/02/18
Diff. 100R P1	L1	94.39	2029477	7	05/02/18
Diff. 100R P2	L4	97.52	2029477	7	05/02/18
Diff. 100R P3	L7	100.84	2029477	7	05/02/18
Diff. 100R P4	L8	99.75	2029477	7	05/02/18
Single 50R P5	L1	53.00	2029477	7	05/02/18
Single 50R P6	L4	46.26	2029477	7	05/02/18
Single 50R P7	L7	48.83	2029477	7	05/02/18
Single 50R P8	L8	53.72	2029477	7	05/02/18
Diff. 100R P1	L1	98.00	2029477	8	05/02/18
Diff. 100R P2	L4	95.57	2029477	8	05/02/18
Diff. 100R P3	L7	100.33	2029477	8	05/02/18
Diff. 100R P4	L8	99.77	2029477	8	05/02/18
Single 50R P5	L1	47.72	2029477	8	05/02/18
Single 50R P6	L4	52.44	2029477	8	05/02/18
Single 50R P7	L7	49.09	2029477	8	05/02/18
Single 50R P8	L8	48.51	2029477	8	05/02/18
Diff. 100R P1	L1	97.49	2029477	9	05/02/18
Diff. 100R P2	L4	94.72	2029477	9	05/02/18
Diff. 100R P3	L7	101.44	2029477	9	05/02/18
Diff. 100R P4	L8	99.53	2029477	9	05/02/18
Single 50R P5	L1	47.21	2029477	9	05/02/18
Single 50R P6	L4	50.42	2029477	9	05/02/18
Single 50R P7	L7	48.58	2029477	9	05/02/18
Single 50R P8	L8	48.43	2029477	9	05/02/18
Diff. 100R P1	L1	98.03	2029477	10	05/02/18
Diff. 100R P2	L4	99.47	2029477	10	05/02/18
Diff. 100R P3	L7	101.60	2029477	10	05/02/18
Diff. 100R P4	L8	100.99	2029477	10	05/02/18
Single 50R P5	L1	47.44	2029477	10	05/02/18
Single 50R P6	L4	49.22	2029477	10	05/02/18
Single 50R P7	L7	49.35	2029477	10	05/02/18
Single 50R P8	L8	48.82	2029477	10	05/02/18
Diff. 100R P1	L1	98.24	2029477	11	05/02/18
Diff. 100R P2	L4	96.93	2029477	11	05/02/18
Diff. 100R P3	L7	100.20	2029477	11	05/02/18
Diff. 100R P4	L8	100.01	2029477	11	05/02/18
Single 50R P5	L1	47.04	2029477	11	05/02/18
Single 50R P6	L4	47.58	2029477	11	05/02/18
Single 50R P7	L7	48.91	2029477	11	05/02/18
Single 50R P8	L8	48.60	2029477	11	05/02/18
Diff. 100R P1	L1	95.97	2029477	12	05/02/18
Diff. 100R P2	L4	96.16	2029477	12	05/02/18
Diff. 100R P3	L7	98.78	2029477	12	05/02/18
Diff. 100R P4	L8	99.62	2029477	12	05/02/18
Single 50R P5	L1	46.55	2029477	12	05/02/18
Single 50R P6	L4	47.70	2029477	12	05/02/18
Single 50R P7	L7	48.74	2029477	12	05/02/18

Central element is a Xilinx Spartan 6 FPGA. The slow control functions, like FEB power on/off or FEB-current measurement are controlled by the L2CB via a shared SPI bus. The CTDB can also be used in standalone mode, e.g. for small test setups.
The channel to channel clock / PPS skew has been measured, is better than 100ps. The power consumption is 2.9W. Presently the second revision is being used.

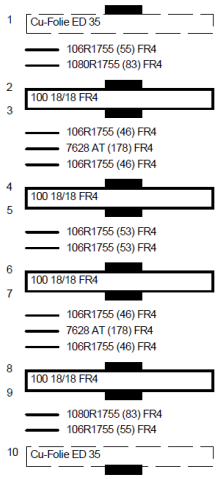
5 The L2CB



The L2CB is the upper element in the digital trigger hierarchy. The 265 L1-trigger signals are connected to a single 676 pin Xilinx Spartan 6 FPGA. These are the main tasks / features:

- Processing (presently just OR-ing) the 265 L1 trigger signals, generating the up going trigger, further processed by the TIB
- Collecting and OR-ing the FEBs busy signal, further processed by the TIB
- Distributing the down going camera trigger, delivered by the TIB
- Distributing the clock and PPS signal, received from the TIB
- CTDB slow control
- Providing an Ethernet connection, using an off the shelf, ARM based MCU (“Stamp8G45”)
- In system FPGA firmware update by the MCU
- GPS (optional usage)
- Extension slot

The 10 layer PCB stack and impedance measurement protocol is shown below:

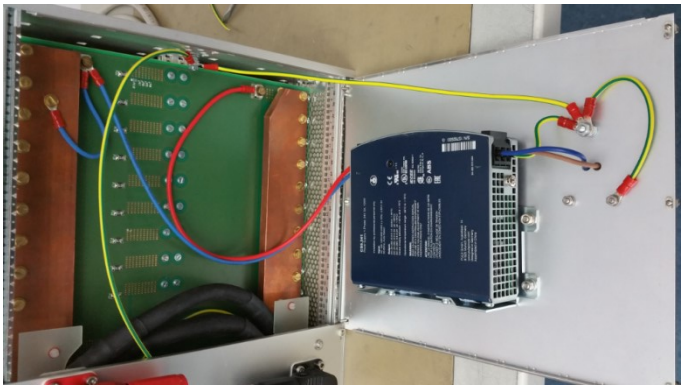


Beschreibung	Lage	Mittelwert	Auftragsnummer	Serien No.
Diff. 100R P1	L1	90.70	2023117	1
Diff. 100R P2	L3	93.43	2023117	1
Diff. 100R P3	L7	94.43	2023117	1
Diff. 100R P4	L10	91.08	2023117	1
Single 50R P5	L1	46.15	2023117	1
Single 50R P6	L3	45.82	2023117	1
Single 50R P7	L7	47.01	2023117	1
Single 50R P8	L10	46.11	2023117	1
Diff. 100R P1	L1	95.71	2023117	2
Diff. 100R P2	L3	93.78	2023117	2
Diff. 100R P3	L7	92.52	2023117	2
Diff. 100R P4	L10	95.36	2023117	2
Single 50R P5	L1	47.47	2023117	2
Single 50R P6	L3	46.35	2023117	2
Single 50R P7	L7	47.52	2023117	2
Single 50R P8	L10	47.54	2023117	2
Diff. 100R P1	L1	95.32	2023117	3
Diff. 100R P2	L3	93.21	2023117	3
Diff. 100R P3	L7	94.62	2023117	3
Diff. 100R P4	L10	99.97	2023117	3
Single 50R P5	L1	47.83	2023117	3
Single 50R P6	L3	45.96	2023117	3
Single 50R P7	L7	47.06	2023117	3
Single 50R P8	L10	48.39	2023117	3
Diff. 100R P1	L1	96.11	2023117	4
Diff. 100R P2	L3	94.28	2023117	4
Diff. 100R P3	L7	93.50	2023117	4
Diff. 100R P4	L10	92.87	2023117	4
Single 50R P5	L1	47.49	2023117	4
Single 50R P6	L3	46.09	2023117	4
Single 50R P7	L7	46.48	2023117	4
Single 50R P8	L10	48.14	2023117	4

The power consumption is 3.2W. The first revision works like expected.

6 The Auxiliary Power Supply

The 24V auxiliary power supply (CS5.241-C1) will be powered first, before the main camera 24V power supplies. This way the FPGA at the L2CB and the CTDB are already loaded and functional. Due to the small size of 124x117x32 mm the power supply can be accommodated directly in the back of the L2-crate. The maximum current is 5A (Ambient temperature < 60°C). The nominal current, drawn by the CTDBs and the L2CB is about 2.5A.



7 Testing and Calibration

7.1 PPS and Clock Skew Measurement

At the DESY test setup 45 channels (3 CTDBs) have been investigated. Two DTBs were in use, one with a fixed connection to slot 1 / channel 1, the other plugged to the remaining channels. The signal TIMEPPS was probed next to the FEB connector. The measurements accuracy was limited by the scope with 1GHz analog Bandwidth and 5GS/s sampling rate (Tektronix MDO3104).

A maximum skew of 140ps was found. Typical values are shown on the right.

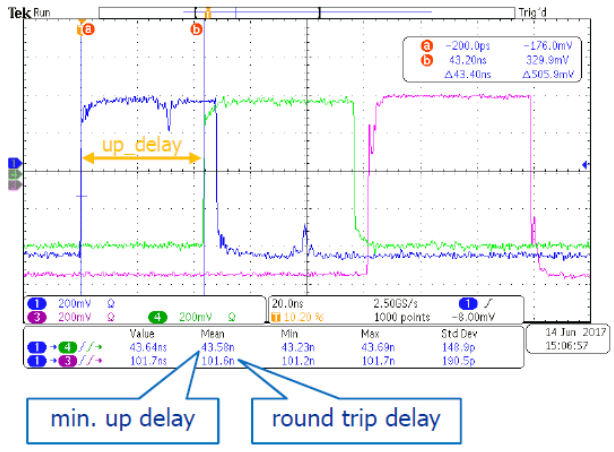
Although the skew is very small, it can be compensated in steps of 37ps by software, using the appropriate DTB-register.

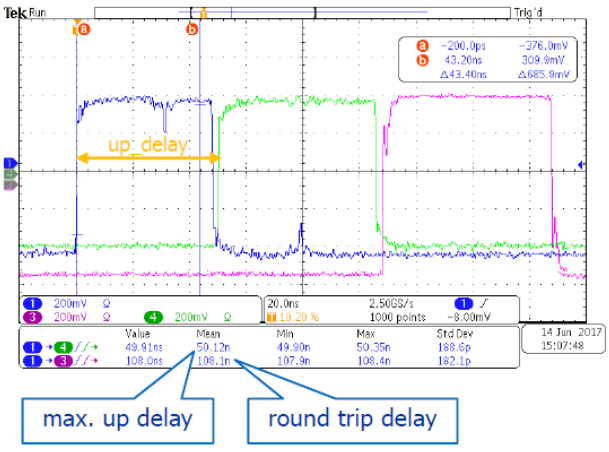
As I know, similar test results have been gained at the Saclay test setup.

slot1	0.00
	-30.00
	-25.00
	-15.00
	10.00
	-50.00
	0.00
	-50.00
	-85.00
	-80.00
	-50.00
	-70.00
	-90.00
	-80.00
	-80.00
slot2	-80.00
	-80.00
	-65.00
	0.00
	-60.00
	-85.00
	-70.00
	-100.00
	-70.00
	-95.00
	-70.00
	-80.00
	-95.00
	-130.00
	-140.00
slot3	-140.00
	-95.00
	-100.00

7.2 L1 Up / Down Delay Measurement / Calibration

For the measurement 90 L1 trigger channels have been investigated, using a CTDB being plugged to slots 1,2,3,9,17,21(most left, ..middle, most right). For the roundtrip measurement the L1 up trigger got back looped, instead of using a TIB (was not available). See below:





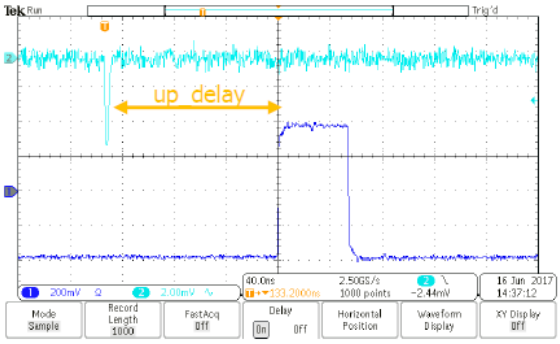
Blue = L1 trigger at DTB (CTDB connector)
Green = L2 trigger at L2CB (TIB connector)
Purple = L1A, camera trigger at FEB

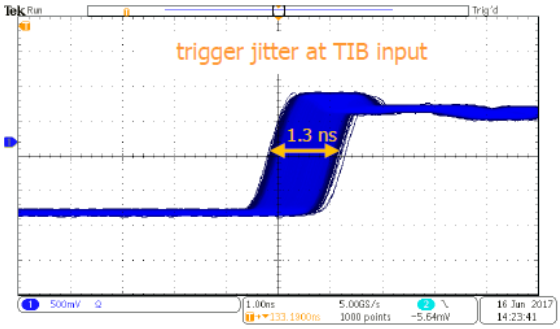
The measurements show, that the main contribution to the L1 up-delay comes from the L2CBs FPGA. There, all L1s hit a 265-inputs OR. The combinatorial delay depends on the FPGA internal routing, a channel to channel skew of up to 6.5 ns have been observed. By using the value of the Xilinx compiler timing analysis, the skew can be minimized. For this, the internal routing got frozen and a channel by channel constant input delay was added.
See below the values before and after the correction:

	up delay		down delay		round trip	
	no corr.	after corr.	no corr.		no corr.	after corr.
min	40.96 ns	45.58 ns	58.03 ns		99.17 ns	103.78 ns
max	45.86 ns	46.42 ns	58.60 ns		104.10 ns	104.95 ns
max-min	4.9 ns	**0.84 ns**	**0.57 ns**		4.93 ns	**1.17 ns**

8 Up going Trigger, Jitter at the TIB Input

The L0 test board, fed by 3 PMT-like signals of -5mV peak, was used. The DTB trigger was set to 3NN. The scope, set to infinite persistence mode, was delay-triggered on one of the analog channels. The observed trigger jitter of +/-0.65ns seems to be a good value. One has to consider, that the asynchronous L0 signal is been sampled by the DTB at 1GSPS, resulting in +/-0.5ns already. The scope itself might contribute to the jitter as well.





9 Down Going Trigger

See the table above. Meant is the delay between the TIB output and the FEB input. The deviation for the 90 tested channels was below 0.57ns. An additional fine tuning in steps of 37ps can be achieved by accessing the L1A_DEL register of the DTB. Normally this is not required.

10 Temperature Measurements

Concerning temperature measurements, no records exist so far. If I rightly remember the temperature difference, both on the CTDB and the L2CB FPGA did not exceed 25°C. Other hot spots do not exist. These measurements will be repeated and recorded, once a fully equipped camera is available.

Looking to the measured power consumption (CTDB=2.9W, L2CB=3.2W) and considering the big amount of GND and power pins of the FPGAs (BGA), conducting the heat into the GND and power layers, I do not expect any problems.

The overall power consumption of the fully populated crate is below 60W (58W measured). Just in case, a set of cooling fans, to be installed underneath (?) the crate, is planned. It is also possible to mount some flat (10mm) fans directly in the top region of the crate.