Firmware Download Link: https://www-zeuthen.desy.de/~sulanke/Projects/CTA/Dig_trigger/NectarCam/L2/L2CB/firmware/

L2CB1 Firmware Properties

FPGA: Xilinx XC6SLX100-L1FGG676I

FLASH (SPI, 32 Mbit): AT45DB321E-SHF-B

Revision	Name	Clock source	VHDL-source	Short Description
005	l2cb1_005	External by TIB or local TCXO	l2cb1_005.vhd	clock and trigger fanout to 18 slots of the L2-crate, L1 trigger reception of 265 FEBs, FE-board power on/off via SPI (SPI master), L2 source for the TIB
007	l2cb1_007	External by TIB or local TCXO	L2CB_007_top.vhd	Like 005, but creates 66MHz clock out of the 10Mhz TIB-clock
008	l2cb1_008	External by TIB or local TCXO	L2CB_008_top.vhd	66MHz version, time stamp registers replaced by L1A up/down scaler, see L2CB1_user_manual_v4.pdf
009	L2cb1_009	External by TIB or local TCXO	L2CB_009_top.vhd	First firmware revision with MCF-trigger, set jumper to connect J7-15 to J7-17 , J7-16 to J7-18 (camera_trig->camera_trig_dld)
014	L2cb1_014	External by TIB or local TCXO	L2CB_014_top.vhd	firmware revision with MCF-trigger, set jumper to connect J7-15 to J7-17 , J7-16 to J7-18 (camera_trig->camera_trig_dld)
017	L2cb1_017	External by TIB or local TCXO	L2CB_017_top.vhd	ctrl_rg(13) being used as MCF_ENABLE (Muon Candidate Flag Enable) now, default is ON; BUSY-de-glitcher module implemented, to filter out seldom / random glitches of 3..4ns, seen at the TIB input, using tib_gclk3 (125Mhz), 3 samples with stable signal required;