L2 Controller Board Rev.1, User Manual

Author	*Laboratory*
Karl-Heinz Sulanke	DESY

Approved by	*Laboratory*

List of Abbreviations			
SPI	Serial Peripheral Interface	RW	Read / Write
L2CB	L2 Controller Board	RO	Read Only
CTDB	Clock & Trigger Distribution Board	RWC	Read / Write Clear
L2BP	L2 Crate Backplane	76h	76 hexadecimal
LVDS	Low Voltage Digital Signalling	RTC	Real Time Clock
TIB	Trigger Interface Board	MCU	Microcontroller Unit
PPS	Pulse Per Second	LVDS	Low Voltage Differential Signaling
FEB	Frontend Board	MCF	Muon Candidate Flag
L2BP	L2-crate Backplane	L1DT	L2-Trigger Dead Time
L1A	L1 trigger Accepted		

History			
Version	Date	Firmw. Rev.	Observation
1	18/10/2016	001	Draft
2	20/03/2017	002	
3	29/05/2018	005	
4	28/03/2023	008	
5	21/04/2023	008	Muon trigger introduced
6	01/03/2024	009	Muon trigger delay register introduced
7	11/09/2024	014	Programmable (**ctrl_rg(14)**) L2 trigger gating if FEB-BUSY is on
8	23/09/2024	016	Programmable upgoing TIB trigger (L1or = TIB_CAMERA_Tx) dead time register L1DT added. Programmable (**ctrl_rg(13**) Muon_Candidate_Flag-Enable added**.** **NOTE!!!** To be compliant with the L2CB1 schematic, the **naming has changed** as follows: L1xxx are going up to the TIB, while the downgoing trigger signals are L2xxx, send as L1A by the DTB to the FEB finally.
9	26/03/2025	021	**ctrl_rg(0**) =TIB_TRIG_ BUSY_BLOCK **ctrl_rg(12**) = BUSY-glitch-filter_enable introduced

Distribution	

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1 Introduction

The L2CB is the central board within the L2-crate. From the users point of view, the main parts are the MCU and the FPGA. The MCU controls the FPGA. The FPGA has mainly three functions. Firstly, it receives all 265 L1 triggers and generates a L2-trigger for the TIB. Secondly it controls the 18 CTDBs, e.g. power on / off FEBs including FEB-current monitoring. Thirdly it provides the clock, PPS and L2 trigger signals to be fanned out via the CTDBs to the FEBs as L1A.

2 The L2CB Components

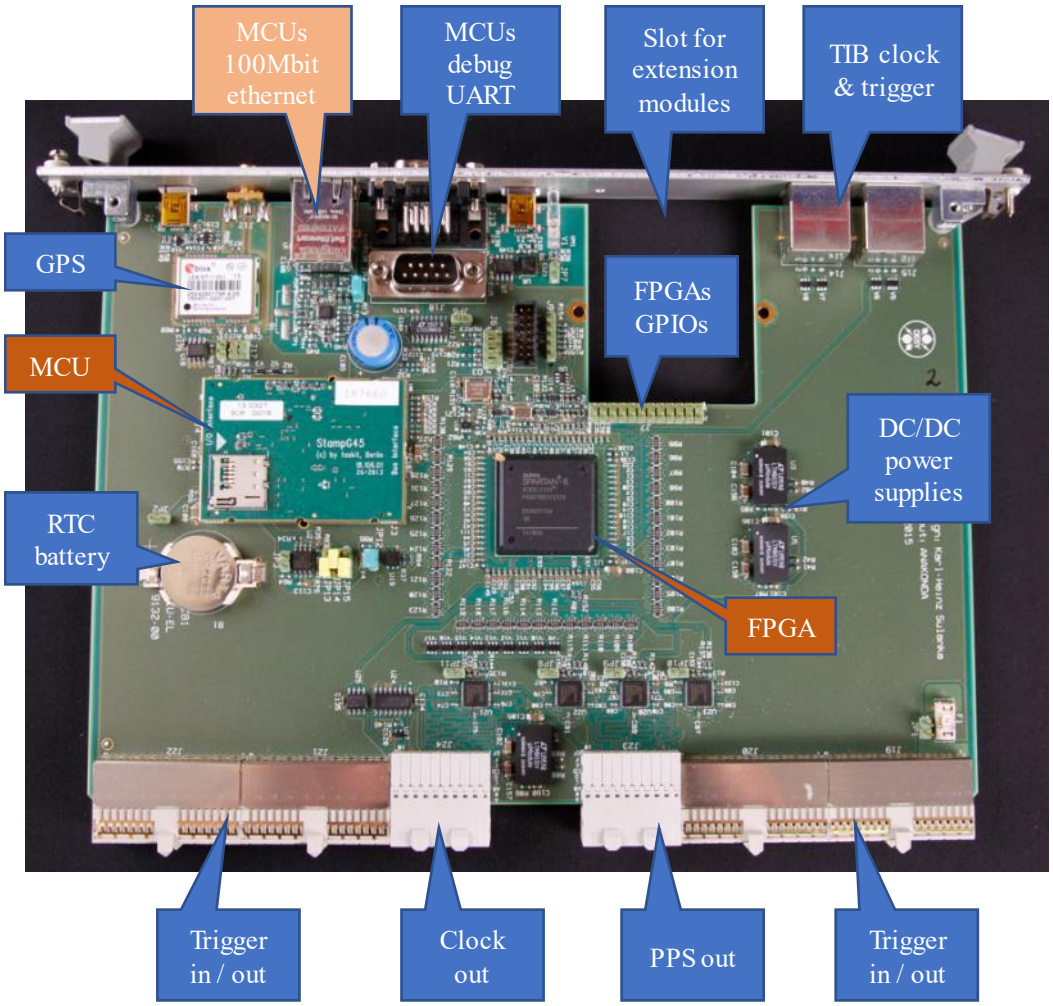


Figure 1 L2CB Components

3 FPGA Firmware, Block Diagram

The FPGA is connected to the MCU (piggy back module) Stamp9G45 by a SRAM like bus, comprising 20 address lines, 16 data lines and control signals. Address decoder and read / write control logic is implemented to access the 18 registers, being used presently.

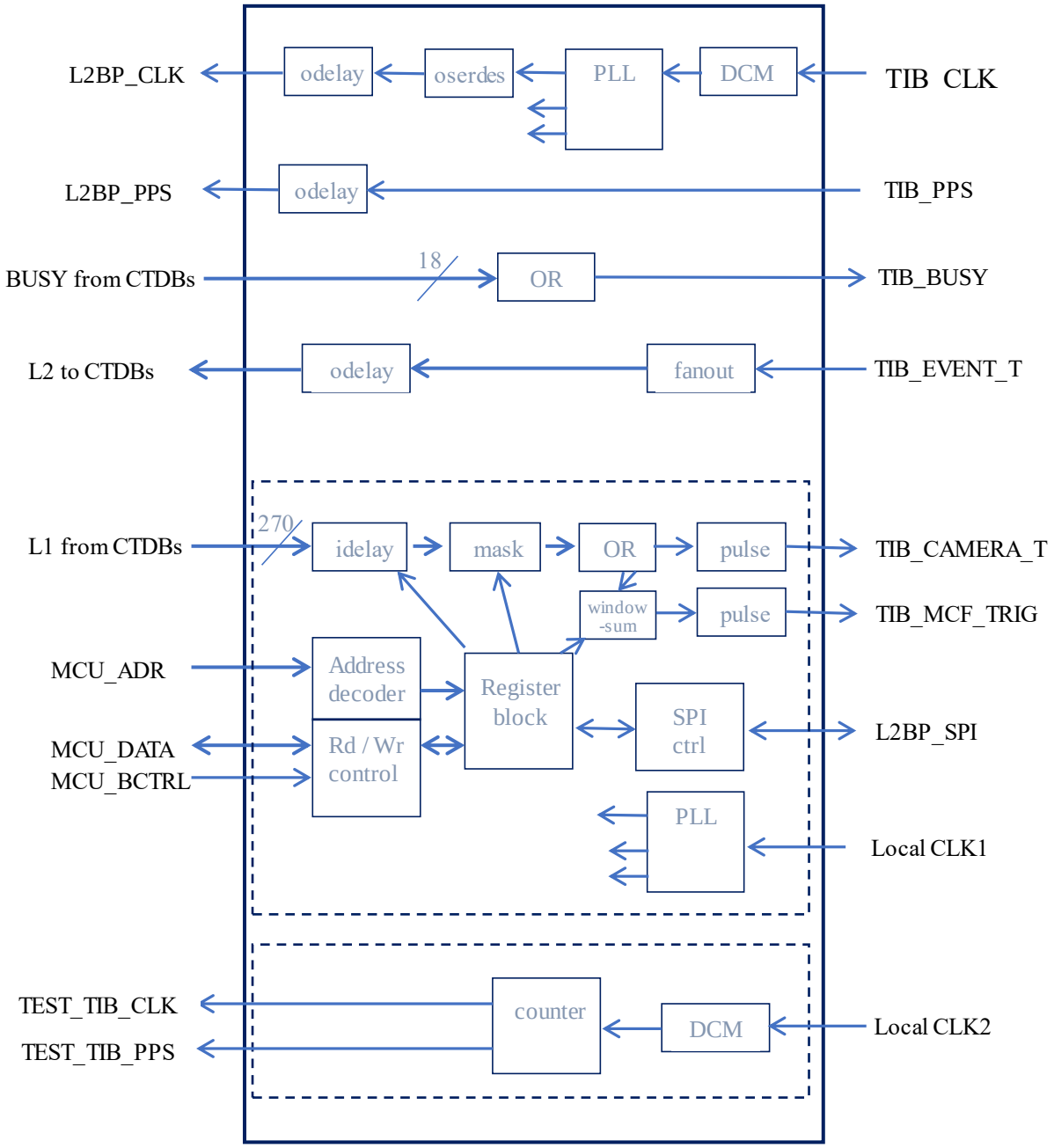


Figure 2 FPGA, firmware block diagram

4 L2CB Interfaces

4.1 *Ethernet to FPGA*

The microcontroller based unit Stamp9G45 is used as a 100Mbit Ethernet to FPGA-bridge. It shares a 16 bit memory bus interface with the FPGA.

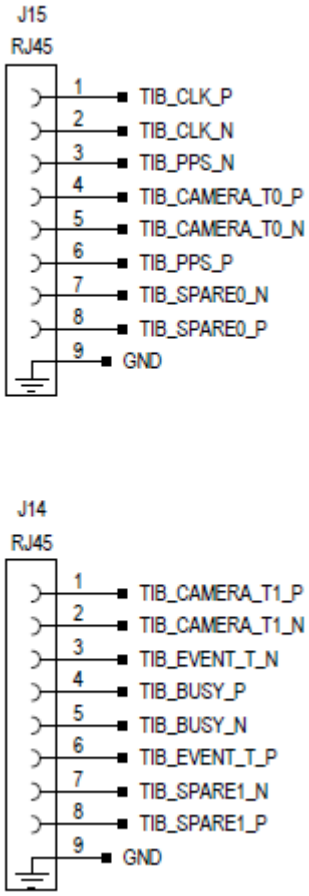
For detailed information check the taskit webpage.

Figure 3 MCU Stamp9G45

To communicate with each of the 18 CTDBs a shared SPI bus on the L2BP is implemented. The L2CB is the bus master.

4.2 *L2CB to TIB*

The L2CBs upper RJ45 connector signals are described below. All signal levels are LVDS. It is assumed, that the leading edge of the 1PPS signal follows the 10MHz leading edge after 7ns. For more details check the L2CB schematic.



Signal	Remark
TIB_CLK	10MHZ, TIB output
TIB_PPS	PPS, TIB output
TIB_CAMERA_T0	L2 trigger, TIB input
TIB_CAMERA_T1	L2 trigger, TIB input
TIB_BUSY	FEB Ored busy-signal, TIB input
TIB_EVENT	L2 trigger, TIB output
TIB_SPAREx	Reserved, TIB input

Figure 4 TIB signals at RJ45 connectors

4.3 *L2CB to CTDB*

The CTDB registers are being accessed through the L2-crate backplane (L2BP). All 18 CTDBs are sharing a SPI Bus. How to initiate the SPI read or write cycle, see below, the register description.

SPI_SCLK	L2CB output that provides 32 clock cycles at each slow control access. The frequency of the clock it is 6.25 MHZ . The electrical standard for this signal is LVDS. Other frequencies are possible.
SPI_SYNCn	L2CB output , low during the slow control access and else high. Electrical standard for this signal is LVDS.
SPI_MOSI	Master output / slave input data line. A 32-bit word is transmitted at each slow control access. Electrical standard for this signal is LVDS. The most significant bit is transmitted first. The format of the 32-bit word is shown in table 1.
SPI_MISO	Master input / slave output data line. Electrical standard for this signal is LVDS. A 16-bit word is transmitted at each slow control access. The most significant bit is transmitted first. Active at a read access, else tristated. This line provides the information of the addressed CTDB register.

Table 1 L2 Backplane, SPI Bus signals

Bit range	Usage
31	RD = '0', WR = '1'
30-16	Address_14..0, register address
15-0	Data_15..0, data word

Table 2 Slow control 16 bit data field, Bit-15 (MSB) is sent first

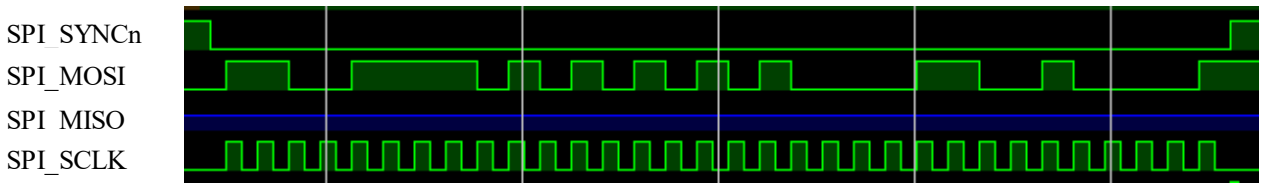


Figure 5 Example, writing data 4321h to address 4f55h

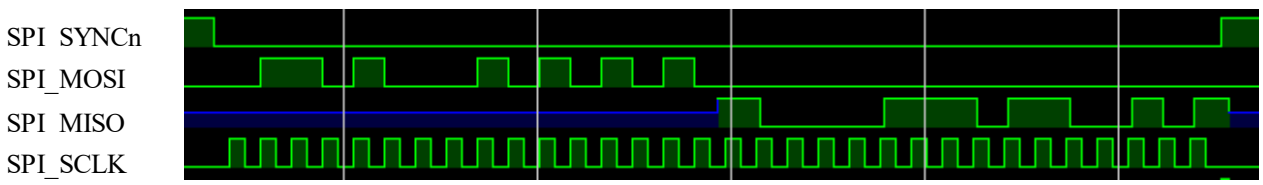


Figure 6 Example, reading data 8765h from address 68aah

Measured SPI bus cycles are illustrated below. The Bus cycle time is about 5.4 us. Higher rates can be achieved by adapting the L2CB firmware accordingly.

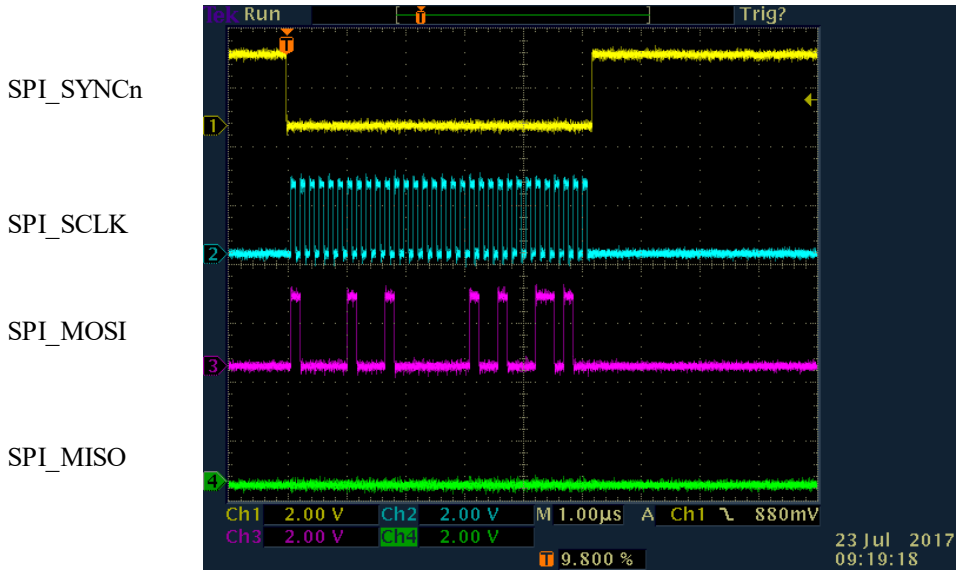


Figure 7 SPI write cycle of 1234h to address 20h of CTDB at slot 2

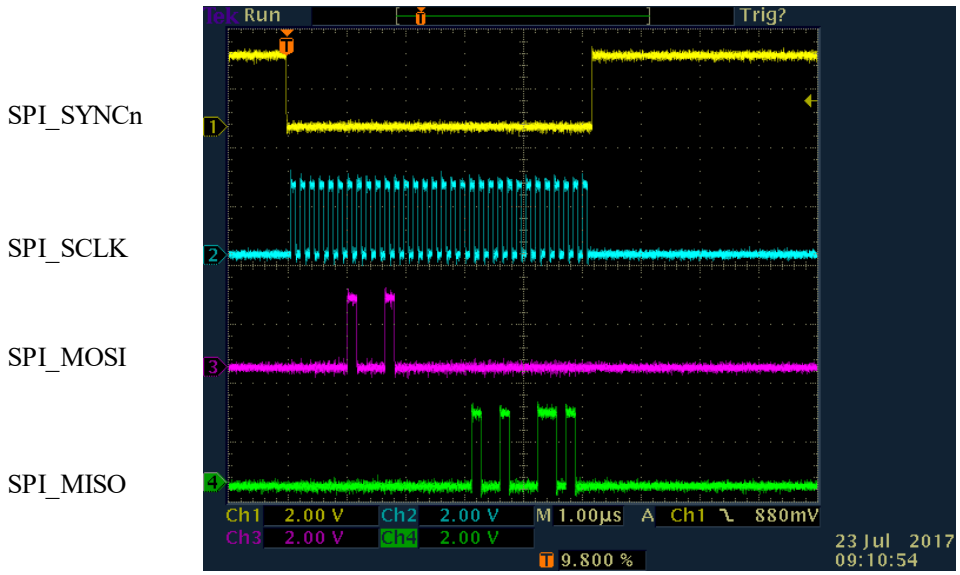


Figure 8 SPI read of 1234h from address 20h of CTDB at slot 2

5 L2CB Register Address Map, Base Address = 000h

hex addr.	Name	Usage
00	CTRL	Control register
02	STAT	Status register
04	SPAD	SPI Address register
06	SPTX	SPI Tx Data register
08	SPRX	SPI Rx Data register
0a	TSTMP0	Time stamp, bits 15..0
0c	TSTMP1	Time stamp, bits 31..16
0e	TSTMP2	Time stamp, bits 47..32
10	TEST	Test register, 16 bit R/W
12	L1SEL	L1 Trigger channel select, for masking and up delay adjust
14	L1MSK	L1 Trigger mask for channels of selected L2-crate slot
16	L1DEL	L1 trigger delay in 37ps steps, 0..5ns
18	MUTHR	Muon threshold, amount of L1s, causing a Muon-trigger, ***1**
20	MUDEL	Programmable Muon trigger delay dealing with the time required by the 265bit adder, in steps of 5ns
22	L2DT	L2 dead time in multiples of 5ns
...		
...		
fe	FREV	Firmware Revision, bits 15..0

The registers can be accessed by the Stamp9G45 module via ethernet or the RS232 interface.

***1** available at firmware revisions 009 and later*

Register Description

attribute	explanation
RW	Read / Write
RO	Read Only
RWC	Read / Write Clear (writing a '1' clears the bit)

CTRL @ address 00h, 16 bit RW, power_on_value = 3001h

Bit	Attr.	Usage
15	RW	0 to 1 change latches a 48 bit time stamp counter, clocked by TIB_10MHz
14	*RW*	
13	RW	MCF_ENABLE, '0' prevents the MCF-trigger being propagated to the TIB (signal TIB_SPARE1_P/N at J14-8/7), '1'= active, default is '1'
12	RW	BUSY_GLITCH_FILTER_ENABLE, '1'= active, default is '1' *[1]
11..1	RW	reserved
0	RW	TIB_TRIGGER_BUSY_BLOCK, '1'= active, default is '1' *[1]

*[1] at firmware rev. 021 and higher

STAT @ address 02h, 16 bit RO, RWC, power_on_value = 0 (0000h)

Bit	Attr.	Usage
0	RO	'1'= SPI bus cycle busy
1	RO	'1'= L1 delay set busy
2	RO	'1' = TIB is in (stuck) busy state
15..2	'0'	Reserved, read value is '0'

Status bits to poll on the readiness of the operation.

Any write operation to the SPAD register initiates a SPI cycle to access a certain CDTB. For SPI write operations, data have to be written to the SPTX register first ! Before initiating the next SPI cycle check STAT-bit_0 (polling on readiness).

SPAD @ address 04h, 13 bit RW, power_on_value = 0 (0000h)

Bit	Attr.	Usage
7..0	RW	CTDB register address
12..8	RW	L2-Crate, CTDB slot number: 1..9, 13..21
14..13	'0'	Reserved, write '0'
15	RW	'1' = Write cycle, '0' = Read cycle

SPTX @ address 06h, 16 bit RW, power_on_value = 0 (0000h)

Bit	Attr.	Usage
15..0	RW	SPI (CTDB register) data, to be sent

SPRX @ address 08h, 16 bit RO, power_on_value = 0 (0000h)

Bit	Attr.	Usage
15..0	RO	SPI (CTDB register) data received

The 0 to 1 transition of the CTRL-reg. bit_15 latches the 48 bit counter, driven by a 125MHz clock (8ns). The clock is synchronous to the TIB-10MHz clock.

TSTMP0 @ address 0ah, 16 bit RO, power_on_value = 0 (0000h)

Bit	Attr.	Usage
15..0	RO	time stamp, bits 15..0 , multiples of 8ns

TSTMP1 @ address 0ch, 16 bit RO, power_on_value = 0 (0000h)

Bit	Attr.	Usage
15..0	RO	time stamp, bits 31..16

TSTMP2 @ address 0eh, 16 bit RO, power_on_value = 0 (0000h)

Bit	Attr.	Usage
15..0	RO	time stamp, bits 47..32

TEST @ address 10h, 16 bit RW, power_on_value = 0 (0000h)

Bit	Attr.	Usage
15..0	RW	read / write test register, no additional functionality

L1SEL @ address 12h, 16 bit RW, power_on_value = 0 (0000h)

Bit	Attr.	Usage
3..0	RW	CTDB channel number of selected slot, valid are: 1..15
8..4	RW	L2-crate slot number, valid are: 1..9, 13..21
15..9	RO	unused, read value is '0'

After power on, all L1s are blocked. Write a '1' to the selected L1MSK bit for enabling the dedicated L1 signal.

L1MSK @ address 14h, 16 bit RW, power_on_value = 0 (0000h)

Bit	Attr.	Usage
0	RO	unused, read value is '0'
15..1	RW	trigger mask for the selected (L1SEL reg.) slot, each channel has its own select bit, valid are 0000h...fffeh, '0' means L1-trigger of the selected channel is not used

Before changing the L1 delay of a particular channel, check the STAT-bit_1 (polling on readiness). The delay for other channels can be set immediately. Note, the readiness for a particular channel requires the occurrence of several L1 signals.

L1DEL @ address 16h, 8 bit RW, power_on_value = 0 (0000h)

Bit	Attr.	Usage
7..0	RW	L1 delay of selected (by L1SEL reg.) trigger channel, usable range 0..128 (x 37ps)
15..8	RO	00h

MUTHR @ address 18h, 9 bit RW, power_on_value = 14h,***1**

Bit	Attr.	Usage
8..0	RW	Muon trigger threshold, amount of simultaneous L1s within the programmable (MUDEL) trigger window, default is 20 (dec)
15..9	RO	00h

***1** available at firmware revisions 013 and later

MUDEL @ address 20h, 4 bit RW, power_on_value = 0ah,***2**

Bit	Attr.	Usage
3..0	RW	Muon trigger window in multiples of 5ns after the L1-up (TIB_CAMERA_T) LH-edge, default is 50ns
15..4	RO	00h

***2** available at firmware revisions 014 and later

L1DT @ address 22h, 8 bit RW, power_on_value = 0000h,***3**

Bit	Attr.	Usage
7..0	RW	L1-up trigger (TIB_CAMERA_Tx) dead time, multiples of 5ns
16..8	RO	00h

***3** available at firmware revisions 016 and later, at 00h the dead time is 15ns

FREV @ address fe, 16 bit RO

Bit	Attr.	Usage
15..0	RO	read back of the L2CB firmware revision

6 Register Access

6.1 *Via OPCUA Server*

An OPCUA server, developed by David Melkumyan, is running on the MCU. For details, check MST-CAM-TN-0481-DESY.

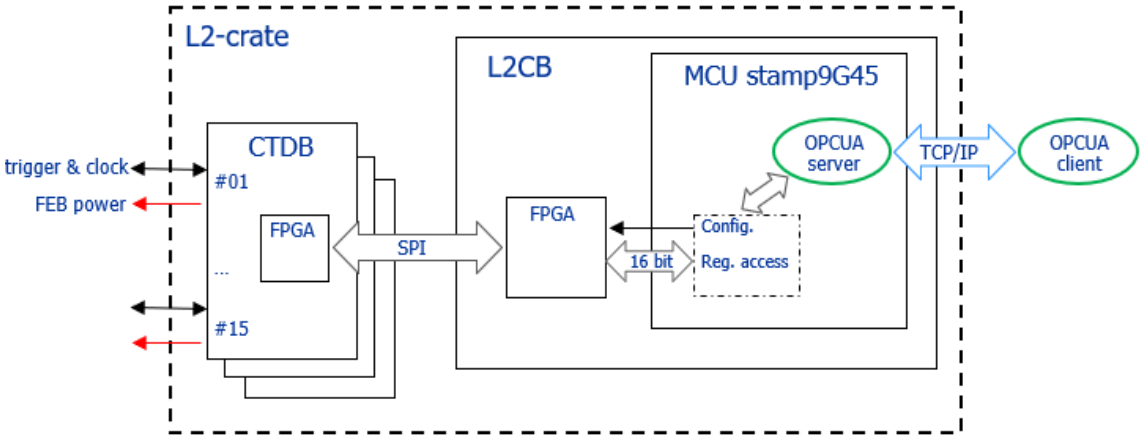


Figure 9 Register access via OPCUA server

6.2 *Using a simple Register Read / Write Tool*

A simple register access tool is implemented on the MCU as well. Esp. for debugging it can be very useful. Instead of the ethernet connection one can also use the MCUs debug RS232 / UART port with the following settings: 115200baud, 1,8,1,no parity, no flow control .

login:root password:taskit

Useful commands are:

ls /opt/cta/bin

cta_ctrl -h // CTDB access

smcrw -h // L2CB register access