Clock & Trigger Distribution Board Rev.1, User Manual

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List of Abbreviations

76h	76 hexadecimal
CTDB	Clock & Trigger Distribution Board
DTB	Digital Trigger Backplane
FEB	Frontend Board
L2BP	L2 Crate Backplane
L2CB	L2 Controller Board
LVDS	Low Voltage Digital Signalling
MISO	master in slave out
MOSI	master out slave in
PDB	Power Distribution Box
PMT	Photo Multiplier Tube
RO	Read Only
RW	Read / Write
RWC	Read / Write Clear
SCLK	serial clock
SPI	Serial Peripheral Interface
SYNCn	low active synchronization (frame signal)
TIB	Trigger Interface Box

History		
Version	Date	Observation
1	06/12/2017	1st Revision

Distribution	

Table of Contents

1. Introduction

This document describes the CTDB, in detail its register functionality. Each CTDB is connected to 15 FEBs via Cat.7 cables. The L2-crate is populated with 18 CTDBs. The slot address (L2-crate position, the CTDB is plugged to) of each CTDB is hard encoded in the L2BP, means there is no need to assign an address e.g. by using jumpers. The CTDB, like the L2CB is powered by an auxiliary power supply, NOT by the main camera power supply being used to power the 265 FEBs. The auxiliary power supply comes up first, ensuring that all FPGAs are loaded, before the software is able to power on the FEBs.

Main tasks of the CTDB are:

- clock and 1PPS distribution to the FEBs, sourced by the L2CB
- reception and propagation of 15 L1 signals
- fanning out and propagating the camera trigger signal to the FEBs
- reception and propagation of the FEB BUSY signals to the L2CB

The 256 x 16 bit register block is accessible via the SPI bus, physically located on the L2BP. This SPI bus is shared among all 18 CTDBs, populating the L2-crate. Bus master is the L2CB.

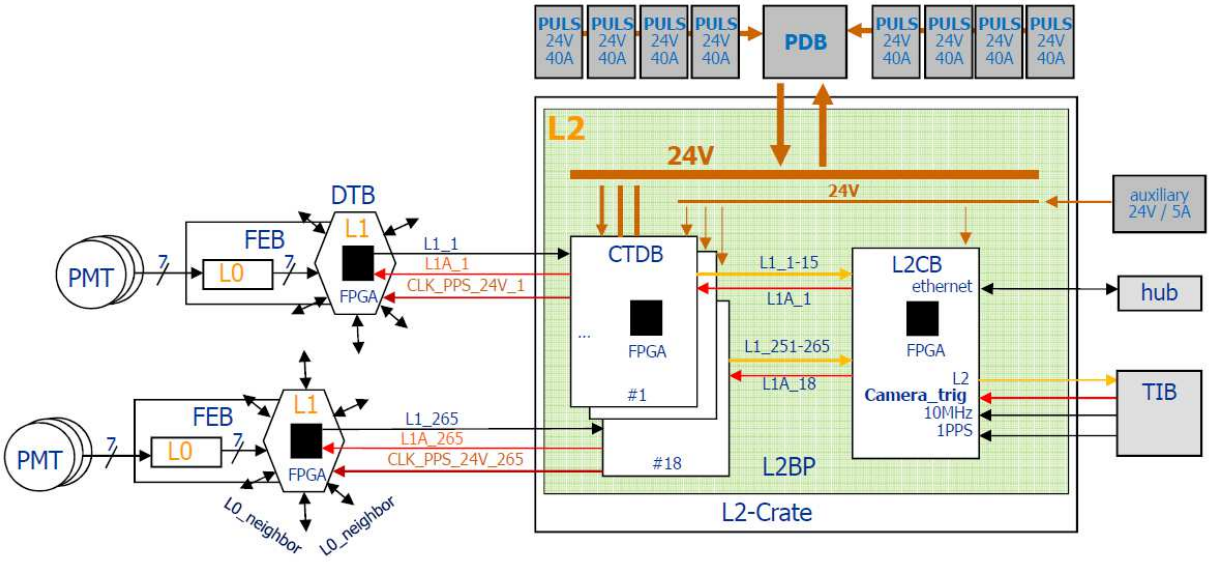

Figure 1: Trigger and Power Topology

2. Slow Control via SPI Bus

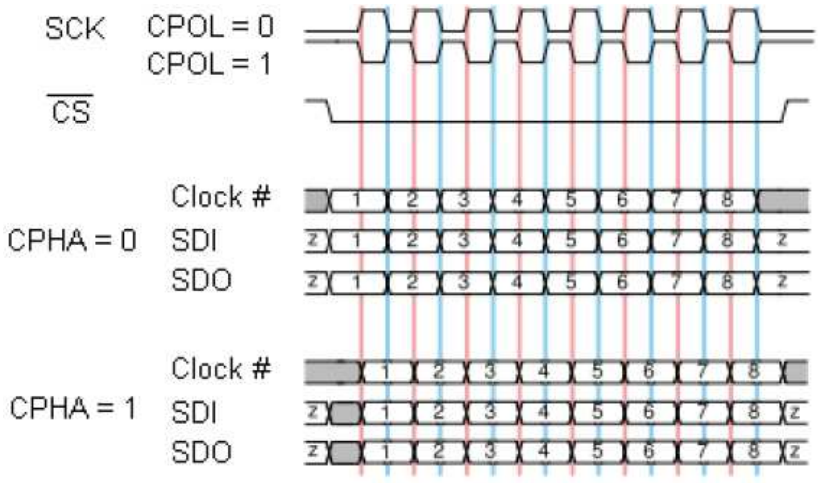

Figure 2: SPI Bus Modes. The used SPI Bus mode is of the type CPOL = 0, CPHA = 1

L2 Backplane, SPI Bus signals	
SPI_SCLK	L2CB output that provides 32 clock cycles at each slow control access. The frequency of the clock it is 6.25 MHZ . The electrical standard for this signal is LVDS. Other frequencies are possible.
SPI_SYNCn	L2CB output , low during the slow control access and else high. Electrical standard for this signal is LVDS.
SPI_MOSI	Master output / slave input data line. A 32-bit word is transmitted at each slow control access. Electrical standard for this signal is LVDS. The most significant bit is transmitted first. The format of the 32-bit word is shown in table 1.
SPI_MISO	Master input / slave output data line. Electrical standard for this signal is LVDS. A 16-bit word is transmitted at each slow control access. The most significant bit is transmitted first. Active at a read access, else tristated. This line provides the information of the addressed CTDB register.

Bit range	Usage
31	RD = ‘0’, WR = ‘1’
30..29	‘0’, not used
28..24	slot address 4..0 (1..9, 13..21)
23..16	CTDB register address 7..0
15..0	CTDB register data 15..0

Table 1: SPI bit usage, Bit-31 (MSB) is sent first

SPI_SYNC

SPI_SCLK

SPI_MOSI

SPI_MISO

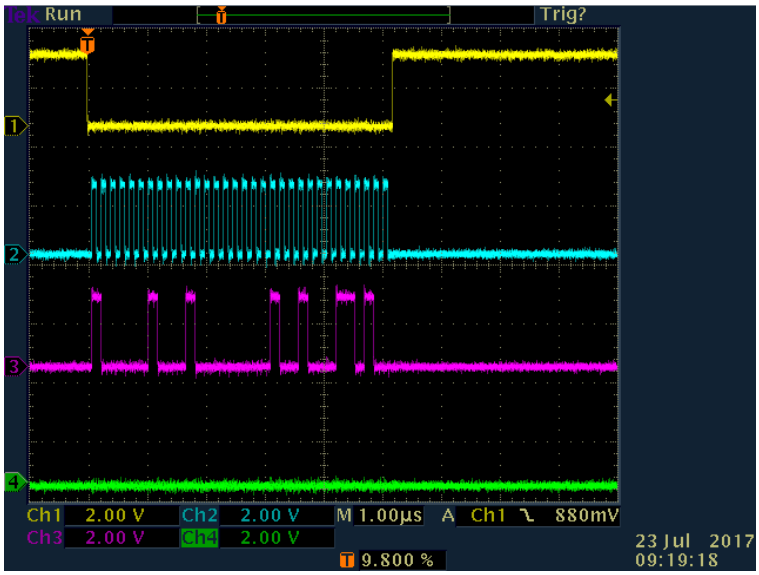

Figure 5: Measured, SPI write cycle of 1234h to address 20h of CTDB at slot 2

SPI_SYNC

SPI_SCLK

SPI_MOSI

SPI_MISO

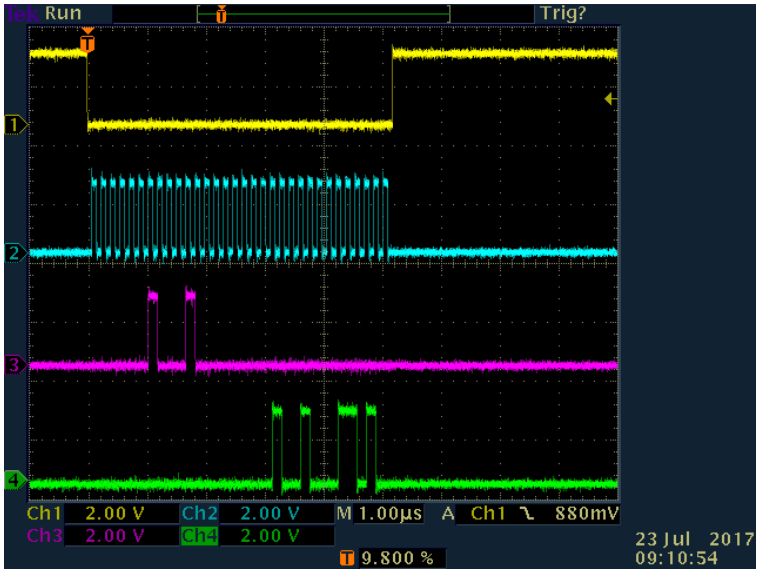

Figure 6: Measured, SPI read of 1234h from address 20h of CTDB at slot 2

Measured SPI bus cycles are illustrated above. The Bus cycle time is about 5.4 us. Higher rates can be achieved by adapting the L2CB firmware accordingly.

3. FEB Powering and Current Measurement

To power on the FEBs, one has to set the appropriate bit of the PONF register. The bit position corresponds to the CTDB channel number, with number one for the top and number 15 for the bottom channel. The numbers are engraved at the left side of the RJ45 connectors. Because the CTDB channel numbering starts with '1', Bit_0 of the registers PONF, OVER_CUR and UNDER_CUR is unused.

The firmware continuously measures the current for the 15 FEBs. The default cycle time is 44.8us. The registers CUR_01 to CUR_15 provide a 12 bit current value. To get mA it has to be multiplied with 0.485 resulting in almost 2A for the full range.

The current limits are defined by the CUR_MIN and CUR_MAX registers. Once the current of a particular channel is not within the limits, the power gets shut down immediately and the STAT register bit_0 pops up. By reading both, the OVER_CUR and the UNDER_CUR register, the male functioning channel can be identified easily by the appropriate bit been set. In case of a real shortcut, it is possible that the bit of the UNDER_CUR register is set, instead of the expected bit of the OVER_CUR register. Reason is the power switch circuit FPF2702MX , acting faster than the firmware fuse (max. 44.8us).

To recover from such a state, the appropriate bit of the PONF has to be cleared and set again. This operation clears the corresponding error status bits as well.

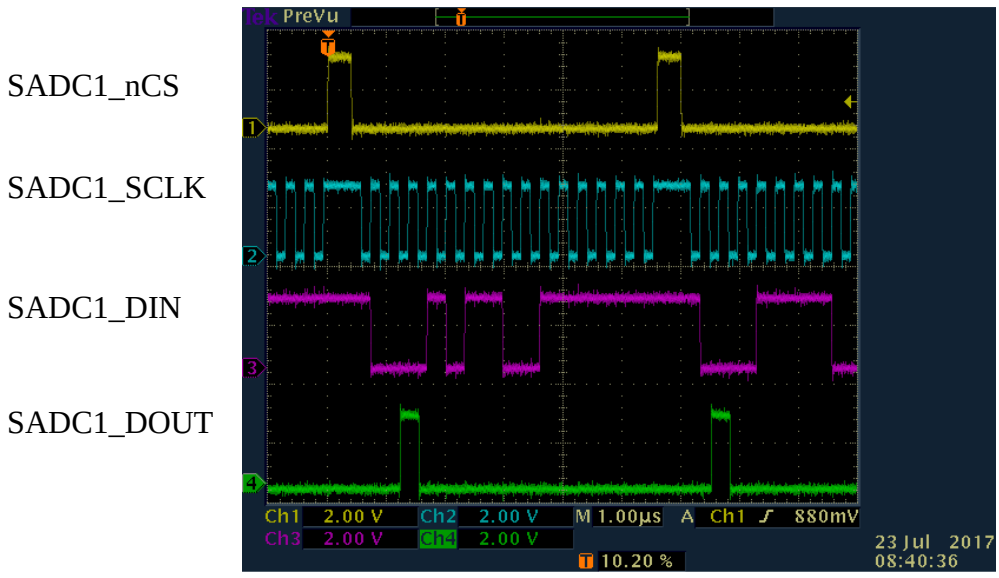

Figure 7: SPI signals of the ADC AD7928 (U45, U46), used for the current measurement

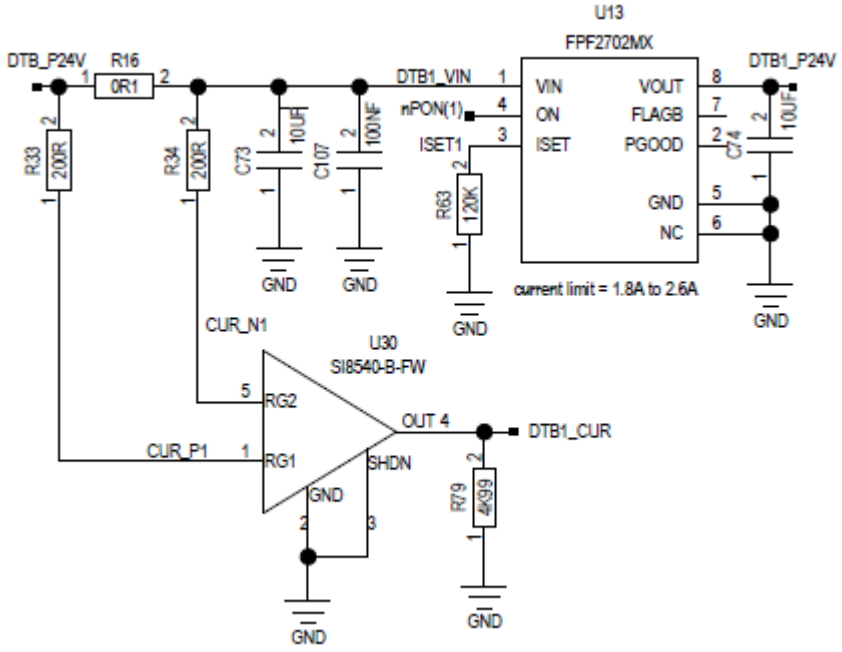

Figure 8: power switch circuit FPF2702MX

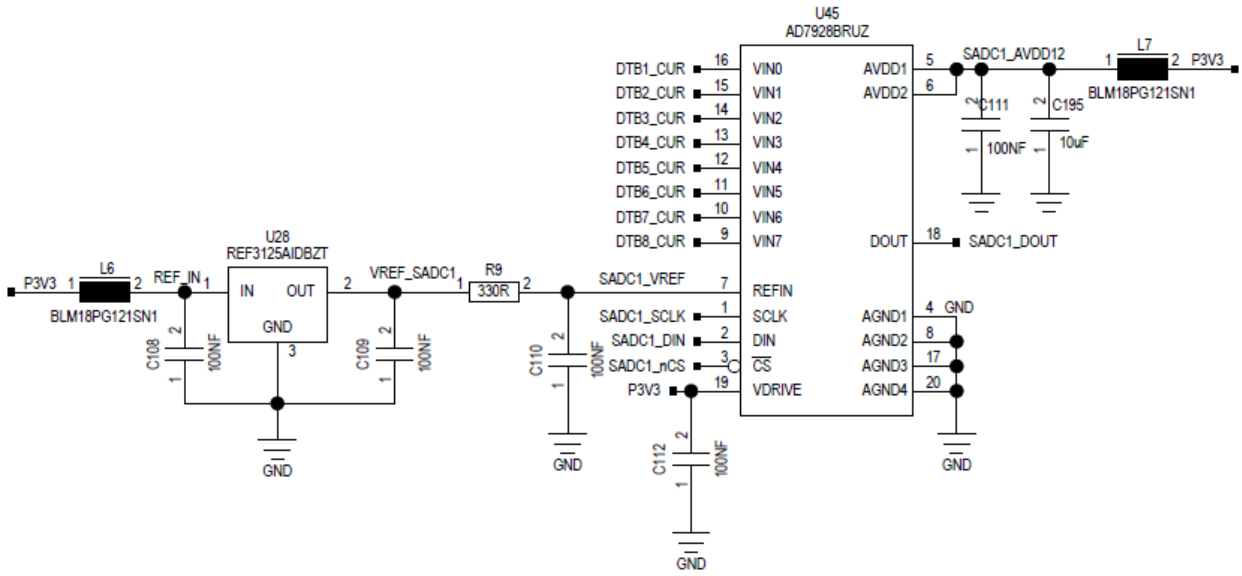

Figure 9: one of two ADCs AD7928, being used for the current measurement

3.1 FEB Powering by Jumper

Figure 10: Test pins SEL(0) to SEL(3)

The FEBs can also be powered in groups by setting jumpers on the test pin field J16, signals SEL(0)...SEL(3), according to the following schema:

SEL-jumper set				CTDB channel powered														
3	**2**	**1**	**0**	**15**	**14**	**13**	**12**	**11**	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**
			x															x
		x															x	x
		x	x													x	x	x
	x														x	x	x	x
	x		x											x	x	x	x	x
	x	x											x	x	x	x	x	x
	x	x	x									x	x	x	x	x	x	x
x											x	x	x	x	x	x	x	x
x			x							x	x	x	x	x	x	x	x	x
x		x							x	x	x	x	x	x	x	x	x	x
x		x	x					x	x	x	x	x	x	x	x	x	x	x
x	x						x	x	x	x	x	x	x	x	x	x	x	x
x	x		x			x	x	x	x	x	x	x	x	x	x	x	x	x
x	x	x			x	x	x	x	x	x	x	x	x	x	x	x	x	x
x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x

The jumper setting overwrites the software control. The current limitation is fixed at 2A. The DEBUG register value must be 0000h (power up value).

4. Register Description

Some registers, located at the top address region, allow additional tuning. Their default settings after power on usually do not need any modification. But if required, there is some room for optimizing or debugging.

4.1. PON_TIME Register

This register defines the period of time in ms, after software controlled power on, while the firmware fuse is disabled. Otherwise the firmware fuse would react, once the inrush current is above the programmed max. value of 1.6A (typical).The measurement below shows the typical FEB inrush current (green curve,~2A pk). The current limitation of about 2A here is due to the configuration of the FPF2702MX, see R63 at Figure 8.

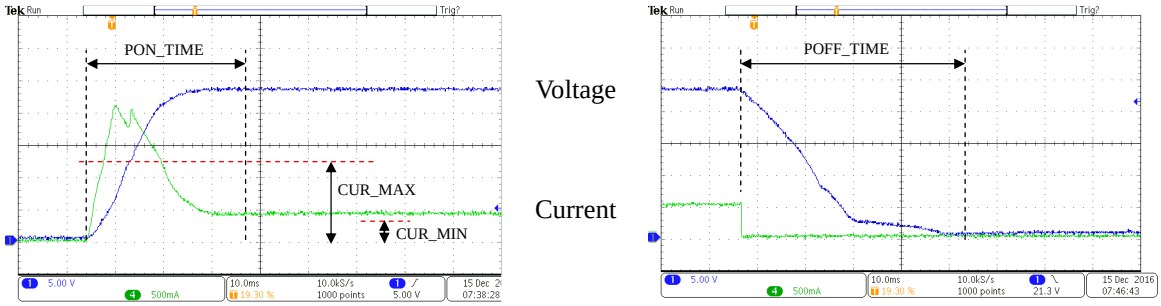

Figure 11: 24V Power on (left) and off (right), measured FEB current and voltage

4.2. POFF_TIME Register

This register defines the period of time in ms, after software controlled power off, before the next power on is possible. Goal is, to wait until all capacitors are fully discharged and the FEB voltage is almost zero. Keep in mind, the FPGA configuration needs a voltage ramp to get started.

4.3. ADC_SRATE Register

The refresh rate for the FEB current ADC can be set by writing a number between 8 and 255 to the ADC_SRATE register. The standard refresh rate is 44.8us (~22kHz) .

refresh_rate = 5.6us * ADC_RATE (= 44.8 us after power on)

4.4. DEBUG Register

The DEBUG register allows to program the usage of the test pin field J16 (SEL(0)..SEL(3)), see figure 10. After power up, the test pins can be used as inputs to power a group of FEBs according to the table shown at chapter 3.1. . By writing a value according to the table shown below, the test pins can be used to verify the timing of several signals, e.g. for the backplane SPI bus or the SPI bus used to control the two serial ADCs (FEB current measurement). Note, the pins 1,3,5,7 of J16 are connected to GND.

DEBUG-reg. value	J16-Pin	Signal (CTDB-schematic)	Remark
00h	2	SEL(0)-input	Set jumpers to power on groups of FEB w/o any software control. Current limit is fixed at about 2A .
	4	SEL(1)-input	
	6	SEL(2)-input	
	8	SEL(3)-input	
01h	2	SADC1_nCS	Check the timing for the current measurement by probing the SPI bus signals of the serial ADC AD7928 (U45).
	4	SADC1_SCLK	
	6	SADC1_DIN	
	8	SADC1_DOUT	
02h	2	SADC2_nCS	Check the timing for the current measurement by probing the SPI bus signals of the serial ADC AD7928 (U46).
	4	SADC2_SCLK	
	6	SADC2_DIN	
	8	SADC2_DOUT	
03h	2	SPI_SYNC	Check the timing and monitor the SPI bus communication on the L2-crates backplane, with the L2CB acting as the bus master.
	4	SPI_SCLK	
	6	SPI_MOSI	
	8	SPI_MISO	

5. Register Address Map

hex addr.	Name	Usage
00	PONF	Power On / Off register
01	CUR_01	value * 0.485 = FEB_24V_current in mA, RJ45 ports 1..15,
...		
0F	CUR_15	
10	CUR_00	value * 0.485 = CTDB_(own)_24V_current in mA
11	CUR_MIN	FEB current, lower limit
12	CUR_MAX	FEB current, upper limit
13	OVER_CUR	over current detected
14	UNDER_CUR	under current detected
20	CTRL	control register for common usage
21	STAT	status register for common usage
FB	PON_TIME	time in ms, to disable the firmware fuse after power on
FC	POFF_TIME	time in ms, after power down, before the next power on is possible
FD	ADC_SRATE	ADC (cur. measurement) sampling rate
FE	DEBUG	to program the usage of the test pins SEL0..3
FF	FREV	Firmware Revision, bits 15..0

6. Register, Bits and Bytes

PONF @ address 00h, 16 bit RW, power_on_value = 0 (0000h)

Bit	Attr.	Usage
0	RO	'0', reserved
15..1	RW	port_15..1, port_1 is the top connector, write a '1' to power on individual ports, write a '0' to power off the port or to clear the errors status

CUR_01..15 @ address 01..0Fh, 12 bit RO, power_on_value = 0 (0000h)

Bit	Attr.	Usage
11..0	RO	FEB current, 0.485 mA / bit, full scale ~2 A
15..12	RO	'0'

CUR_00 @ address 10h, 12 bit RO, power_on_value = 0 (0000h)

Bit	Attr.	Usage
11..0	RO	CTDB-own current load at 24V_aux, 0.485 mA / bit, full scale ~2 A
15..12	RO	'0'

CUR_MIN @ address 11h, 12 bit RW, power_on_value = 100 mA (00CEh)

Bit	Attr.	Usage
11..0	RW	lower current limit, 0.485 mA / bit, full scale ~ 2 A
15..12	RO	'0'

CUR_MAX @ address 12h, 12 bit RW, power_on_value = 1600 mA (0CE3h)

Bit	Attr.	Usage
11..0	RW	uppper current limit, 0.485 mA / bit, full scale ~2 A
15..12	RO	'0'

OVER_CUR @ address 13h, 15 bit RO, power_on_value = 0 (0000h)

Bit	Attr.	Usage
0	RO	'0', reserved
15..1	RO	ports 15..1, '1' = individual current above the max. current limit

UNDER_CUR @ address 14h, 15 bit RO, power_on_value = 0 (0000h)

Bit	Attr.	Usage
0	RO	'0', reserved
15..1	RO	ports 15..1, '1' = individual current below the min. current limit

CTRL @ address 20h, 16 bit RW, power_on_value = 0 (0001h)

Bit	Attr.	Usage
0	RW	firmware fuse enable (check, if FEB current is within the limits)
15..1	RW	reserved

STAT @ address 21h, 16 bit RO, power_on_value = 0 (0000h)

Bit	Attr.	Usage
0	RO	over or under current for at least 1 of the 15 ports detected
1	RO	if set, current values are available, "dummy", is on 20us after FPGA load
15..2	RO	'0', reserved

PON_TIME @ address FBh, 8 bit RW, power_on_value = 0032h (50ms)

Bit	Attr.	Usage
7..0	RW	period of time, after power on, while the firmware fuse is disabled, multiples of 1ms
15..8	RO	'0'

POFF_TIME @ address FCh, 8 bit RW, power_on_value = 003Ch (60ms)

Bit	Attr.	Usage
7..0	RW	period of time, after powering off, preventing power up while capacitors at the FEB are not yet fully discharged
15..8	RO	'0'

ADC_RATE @ address FDh, 8 bit RW, power_on_value = 0 (0008h)

Bit	Attr.	Usage
7..0	RW	FEB current ADC, refresh rate, only number >=8 will be accepted, standard min refresh rate is 44.8us refresh_rate = 5.6us * ADC_RATE (= 44.8 us after power on)
15..8	RO	'0'

DEBUG @ address FEh, 8 bit RW, power_on_value = 0 (0000h)

Bit	Attr.	Usage
7..0	RW	00h : power on groups of FEBs by setting jumpers 01h : serial ADC1 (U45), monitoring SPI bus signals at test pin field J16 02h : serial ADC2 (U46), monitoring SPI bus signals at test pin field J16 03h : L2-crate backplane, monitoring SPI bus signals
15..8	RO	'0'

FREV @ address FFh, 16 bit RO, power_on_value : binary firmware rev. number

Bit	Attr.	Usage
15..0	RO	CTDB firmware revision