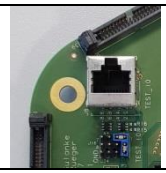
Firmware Download Link: https://www-zeuthen.desy.de/~sulanke/Projects/CTA/Dig_trigger/NectarCam/L1/rev4/firmware/

DTB4 Firmware Properties

FPGA: Xilinx XC6SLX16-3CSG324I

FLASH (SPI, 8 Mbit): AT45DB081D

Revision	Name	Clock source	Trigger delay	Time resolution	VHDL-source	Short Description
004	dtb4_3nn_004	50 MHz external clock	~190 ns (PMT to L1A)	1 ns	dtb4_3nn_004	RJ45: J13-8/7 = TRIG_L1_out J13-4/5 = TRIG_L2_in J13-6/3 = BUSY_out J13-1/2 =1PPS_CLK_24V_in Sampling rate 1 GSPS. External 50 MHz clock modulated with 1PPS. 37 pixel region covered. NectarCam pixel numbering schema implemented. Several 8bit-registers implemented, accessible via FEB/SPI Bus, see **DTB_user_manual_xx.pdf**. Delay tuning via register write in 37ps steps for 1PPS, L1A, 37 L0s. Central cluster power on L0 delay is 60h. New L0 delay values can get loaded, even with L0_BUSY = 1. L0 delay calibration possible using custom cable and the test connector J8 + button SW1.
005	dtb4_3nn_005	50 MHz external clock	~190 ns (PMT to L1A)	1 ns	dtb4_3nn_005	see above, additionally implemented: -L1 scaler -new trigger algorithm “trigger 1_of_37”
006	dtb4_3nn_006	50 MHz external clock	~190 ns (PMT to L1A)	1 ns	dtb4_3nn_006	see above, additionally implemented: - STAT-reg., bit_4, “PPS_ERROR” -PPS_ERR_CT register
007	dtb4_3nn_007	50 MHz external clock	~180 ns (PMT to	1 ns	dtb4_3nn_007	L0 delay schema improved, addional L0 offset for the central cluster is NOT NEEDED anymore, 8ns range for all pixels, coarse (0..7ns)

			L1A)			and additive fine delay (0..1ns) available now. PPS_DEL_CAL reg. address moved to 15
008	dtb4_3nn_008	50 MHz external clock	~180 ns (PMT to L1A)	1 ns	dtb4_3nn_008	CTRL reg., new: bit_5 used as PPS_ERR_CT – clear now, new register added: TRIG_MASK_0 .._6, register TRIG_MASK_C, TRIG_MASK_N removed
009	dtb4_3nn_009	50 MHz external or (!) 25 MHz local clock	~180 ns (PMT to L1A)	1 ns	dtb4_3nn_009	when using local clock (standalone mode) put jumpers on J16_3-1 and J16_2-J24_1(GND) 
010	dtb4_3nn_010	50 MHz external or (!) 25 MHz local clock	~180 ns (PMT to L1A)	1 ns	dtb4_3nn_010	L1 scaler window programmable in steps of 10ms now using the (new) RW register L1_SC_WIN @ 02h, range is 10 ms to 2.55 s
011	dtb4_3nn_011	50 MHz external or (!) 25 MHz local clock	~180 ns (PMT to L1A)	1 ns	dtb4_3nn_011	like rev. 010, with L1A trigger bug fixed (local clock mode)
012	dtb4_3nn_012	50 MHz external or (!) 25 MHz local clock	~180 ns (PMT to L1A)	1 ns	dtb4_3nn_012	when using local clock (standalone mode) put jumpers on J16_3-1 and J16_2-J24_1(GND) like rev. 011, but J13_BUSY_OUT_P/N will get swapped with J13_L2_IN_P/N if J16 is jumpered to local clock mode
013	dtb4_3nn_013	50 MHz external or (!) 25 MHz local clock	~180 ns (PMT to L1A)	1 ns	dtb4_3nn_013	minor change for the L2 input stage (w. delay control) to deal with the loss of the very first L1A (Saclay, ~15 out of 62 boards)
014	dtb4_3nn_014	50 MHz external or (!) 25 MHz local clock	~180 ns (PMT to L1A)	1 ns	dtb4_3nn_014	L1A delay control removed, to deal with the loss of the very first L1A
015	dtb4_3nn_015	50 MHz external or (!) 25 MHz local clock	~180 ns (PMT to L1A)	1 ns	dtb4_3nn_015	first L1A loss fixed (?), L1A delay control removed
016	dtb_3nn_016	66 MHz external or 25 MHz local clock (?)	?	?	dtb4_3nn_016	First rev., that provides an 66MHz clock to the FEB. Not yet fully tested (2021-03-16) !!! Use together with the 66MHz firmware revisions of the CTDB and L2CB.

017	dtb_3nn_017	66 MHz external or 25 MHz local clock	~180 ns (PMT to L1A)		dtb4_3nn_017	When jumpering for local clock mode, the FEB clock EXTCLK_P/N is 66.67MHz else 66MHz. A clean EXTCLK-up after power on is implemented.
018	dtb4_3nn_018	50 MHz external or (!) 25 MHz local clock	~180 ns (PMT to L1A)	1 ns	dtb4_3nn_018	FEB-BUSY can be probed as single ended 2.5V LVTTL signal at SW2-2
019	dtb4_3nn_019	50 MHz external or (!) 25 MHz local clock	~180 ns (PMT to L1A)	1 ns	dtb4_3nn_019	FEB-BUSY can be probed as single ended 2.5V LVTTL signal at SW2-2 CTRL-bit6 = '1' blocks the FEB-BUSY, default is '0'
020	dtb4_3nn_020	50 MHz external or (!) 25 MHz local clock	~180 ns (PMT to L1A)	1 ns	dtb4_3nn_020	L1A scaler implemented at register 17h, 18h
021	dtb4_3nn_021	50 MHz external or (!) 25 MHz local clock	~180 ns (PMT to L1A)	1 ns	dtb4_3nn_021	L1A delay adjustment, register 08h, reactivated
022	dtb4_3nn_022	50 MHz external or (!) 25 MHz local clock	~180 ns (PMT to L1A)	1 ns	dtb4_3nn_022	DEBUG register introduced, supporting L1A to FEB-BUSY tests. For details check the DTB_user_manual_31.pdf
023	dtb4_3nn_023	50 MHz external or (!) 25 MHz local clock	~180 ns (PMT to L1A)	1 ns	dtb4_3nn_023	L1A at BUSY - 16bit scaler implemented Using the DEBUG register with 01h caused the L1A to stuck
025	dtb4_3nn_025	50 MHz external or (!) 25 MHz local clock	~180 ns (PMT to L1A)	1 ns	dtb4_3nn_025	Optional TRGL1 blocking if BUSY, bug (rev.024) fixed
026	dtb4_3nn_026	50 MHz external or (!) 25 MHz local clock	~180 ns (PMT to L1A)	1 ns	dtb4_3nn_026	L1A delay adjustment removed again