# Firmware Download Link: <https://www-zeuthen.desy.de/~sulanke/Projects/CTA/Dig_trigger/NectarCam/L1/rev4/firmware/>

# DTB4 Firmware Properties

FPGA: Xilinx XC6SLX16-3CSG324I

FLASH (SPI, 8 Mbit): AT45DB081D

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| --- | --- | --- | --- | --- | --- | --- |
| **Revision** | **Name** | **Clock source** | **Trigger delay** | **Time resolution** | **VHDL-source** | **Short Description** |
| 004 | dtb4\_3nn\_004 | 50 MHz external clock | ~190 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_004 | RJ45: J13-8/7 = TRIG\_L1\_out J13-4/5 = TRIG\_L2\_in  J13-6/3 = BUSY\_out J13-1/2 =1PPS\_CLK\_24V\_inSampling rate 1 GSPS.External 50 MHz clock modulated with 1PPS. 37 pixel region covered. NectarCam pixel numbering schema implemented.Several 8bit-registers implemented, accessible via FEB/SPI Bus, see **DTB\_user\_manual\_xx.pdf**. Delay tuning via register write in 37ps steps for 1PPS, L1A, 37 L0s. Central cluster power on L0 delay is 60h. New L0 delay values can get loaded, even with L0\_BUSY = 1.L0 delay calibration possible using custom cable and the test connector J8 + button SW1. |
| 005 | dtb4\_3nn\_005 | 50 MHz external clock | ~190 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_005 | see above, additionally implemented:-L1 scaler-new trigger algorithm “trigger 1\_of\_37” |
| 006 | dtb4\_3nn\_006 | 50 MHz external clock | ~190 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_006 | see above, additionally implemented:- STAT-reg., bit\_4, “PPS\_ERROR”-PPS\_ERR\_CT register  |
| 007 | dtb4\_3nn\_007 | 50 MHz external clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_007 | L0 delay schema improved, addional L0 offset for the central cluster is NOT NEEDED anymore, 8ns range for all pixels, coarse (0..7ns) and additive fine delay (0..1ns) available now.PPS\_DEL\_CAL reg. address moved to 15 |
|  |  |  |  |  |  |  |
| 008 | dtb4\_3nn\_008 | 50 MHz external clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_008 | CTRL reg., new: bit\_5 used as PPS\_ERR\_CT – clear now,new register added: TRIG\_MASK\_0 ..\_6,register TRIG\_MASK\_C, TRIG\_MASK\_N removed |
| 009 | dtb4\_3nn\_009 | 50 MHz external or (!) 25 MHz local clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_009 | H:\zn\Projects\CTA\Bpl_Trig\doc\DTB4_locally_clocked_jumper_snippet.jpgwhen using local clock (standalone mode) put jumpers on J16\_3-1 and J16\_2-J24\_1(GND)  |
| 010 | dtb4\_3nn\_010 | 50 MHz external or (!) 25 MHz local clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_010 | L1 scaler window programmable in steps of 10ms now using the (new) RW register L1\_SC\_WIN @ 02h, range is 10 ms to 2.55 s |
| 011 | dtb4\_3nn\_011 | 50 MHz external or (!) 25 MHz local clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_011 | like rev. 010, with L1A trigger bug fixed (local clock mode) |
| 012 | dtb4\_3nn\_012 | 50 MHz external or (!) 25 MHz local clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_012 | when using local clock (standalone mode) put jumpers on J16\_3-1 and J16\_2-J24\_1(GND) like rev. 011, but J13\_BUSY\_OUT\_P/N will get swapped with J13\_L2\_IN\_P/N if J16 is jumpered to local clock mode |
| 013 | dtb4\_3nn\_013 | 50 MHz external or (!) 25 MHz local clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_013 | minor change for the L2 input stage (w. delay control) to deal with the loss of the very first L1A (Saclay, ~15 out of 62 boards) |
| 014 | dtb4\_3nn\_014 | 50 MHz external or (!) 25 MHz local clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_014 | L1A delay control removed, to deal with the loss of the very first L1A |
| 015 | dtb4\_3nn\_015 | 50 MHz external or (!) 25 MHz local clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_015 | first L1A loss fixed (?), L1A delay control removed |
| 016 | dtb\_3nn\_016 | 66 MHz external or 25 MHz local clock (?) | ? | ? | dtb4\_3nn\_016 | First rev., that provides an 66MHz clock to the FEB. Not yet fully tested (2021-03-16) !!!Use together with the 66MHz firmware revisions of the CTDB and L2CB. |
| 017 | dtb\_3nn\_017 | 66 MHz external or 25 MHz local clock | ~180 ns(PMT to L1A) |  | dtb4\_3nn\_017 | When jumpering for local clock mode, the FEB clock EXTCLK\_P/N is 66.67MHz else 66MHz. A clean EXTCLK-up after power on is implemented. |
| 018 | dtb4\_3nn\_018 | 50 MHz external or (!) 25 MHz local clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_018 | FEB-BUSY can be probed as single ended 2.5V LVTTL signal at SW2-2 |
| 019 | dtb4\_3nn\_019 | 50 MHz external or (!) 25 MHz local clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_019 | FEB-BUSY can be probed as single ended 2.5V LVTTL signal at SW2-2CTRL-bit6 = ‘1’ blocks the FEB-BUSY, default is ‘0’ |
| 020 | dtb4\_3nn\_020 | 50 MHz external or (!) 25 MHz local clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_020 | L1A scaler implemented at register 17h, 18h |
| 021 | dtb4\_3nn\_021 | 50 MHz external or (!) 25 MHz local clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_021 | L1A delay adjustment, register 08h, reactivated |
| 022 | dtb4\_3nn\_022 | 50 MHz external or (!) 25 MHz local clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_022 | DEBUG register introduced, supporting L1A to FEB-BUSY tests. For details check the DTB\_user\_manual\_31.pdf |
| 023 | dtb4\_3nn\_023 | 50 MHz external or (!) 25 MHz local clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_023 | L1A at BUSY - 16bit scaler implementedUsing the DEBUG register with 01h caused the L1A to stuck |
| 025 | dtb4\_3nn\_025 | 50 MHz external or (!) 25 MHz local clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_025 | Optional TRGL1 blocking if BUSY, bug (rev.024) fixed |
| 026 | dtb4\_3nn\_026 | 50 MHz external or (!) 25 MHz local clock | ~180 ns(PMT to L1A) | 1 ns | dtb4\_3nn\_026 | L1A delay adjustment removed again |