Digital Trigger Backplane User Manual

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List of Abbreviations			
ATBP	Analog Trigger Backplane	RW	Read / Write
DTB	Digital Trigger Backplane	RO	Read Only
FEB	Frontend Board	RWC	Read / Write Clear
SPI	Serial Peripheral Interface	76h	76 hexadecimal

History		
Version	Date	Observation
1	10/10/2016	Draft
1a	06/11/2016	Draft, corrected
1b	08/11/2016	see TRIG_PULS register description
1c	14/02/2017	STAT reg. bits changed, L0_DELAY_BUSY explanation added
1d	15/02/2017	initial L0 delay removed
20	03/03/2017	valid for DTB4 now, trigger 2 of 37 added for L0 delay calibration
21	18/09/2017	L1 scaler added, trigger 1_of_37 added, L0_DEL_SEL reg. renamed to PIXEL_SEL reg.
22	27/09/2017	added correct max. L0 delay value of 5ns (87h)
23	18/10/2017	PPS_ERR_CT register and new STAT-reg. bit added
24	06/11/2017	see description of the L0_DEL register, coarse and fine delay introduced
25	21/11/2017	CTRL reg. description corrected (bit_7)
26	20/12/2017	CTRL reg., new: bit_5 used as PPS_ERR_CT – clear now new register added: TRIG_MASK_0 .._6 register TRIG_MASK_C, TRIG_MASK_N removed
27	20/02/2018	common firmware / description for locally and externally clocked DTB now
28	26/02/2018	new register introduced, L1_SC_WIN, L1 scaler window programmable now, from 10ms to 2.55s
29	19/10/2023	FEB-BUSY blocker by using CTRL-bit6 introduced, available for DTB firmware rev. >=19
30	29/02/2024	16bit L1A counter implemented, for test purposes
31	21/03/2024	DEBUG control register implemented, allows to block L1As in case of a BUSY signal, available for DTB firmware rev. >=22
32	22/03/2024	16bit L1A-while-BUSY counter implemented, for test purposes

Distribution	

Table of Contents

1 Introduction

This document describes the slow control software interface between the NectarCam frontend board and the Digital Trigger Backplane. Up to 128 8-bit registers can be implemented.

Valid for firmware Rev. **DTB4_3nn_010**

2 Local clocking of the DTB

Usually the DTB is externally clocked by the CTDB via it's Cat.7 cable connection. Especially for the FEB test it is useful to run the DTB in a standalone mode, clocked by the 25 MHz local oscillator Q1. To run the DTB in the locally clocked mode one has to set a jumper on J16_3-1 and J16_2-J24_1 (GND), see snippet.

Compared to the externally clocked mode there are some minor differences:

- 1PPS (signal TIMEPPS) is made from the local clock
- the camera trigger "L1A" is per default the looped backed up going trigger. To disable the loop back bit_7 of the CTRL register must be set.

3 Pixel Numbering Schema

The pixel numbering schema is the one used by the NectarCam team, viewing from outside on the focal plane. The shown cluster numbering is used within the DTB firmware, therefor relevant for the DTB register description.

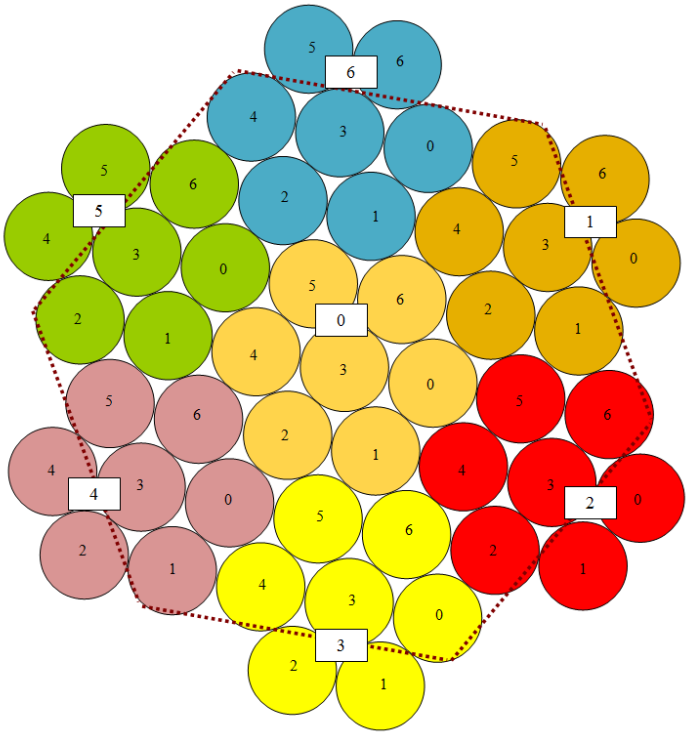


Figure 1: Pixel Numbering Schema, focal plane view

4 The Digital Trigger Backplane Slow Control via SPI Bus

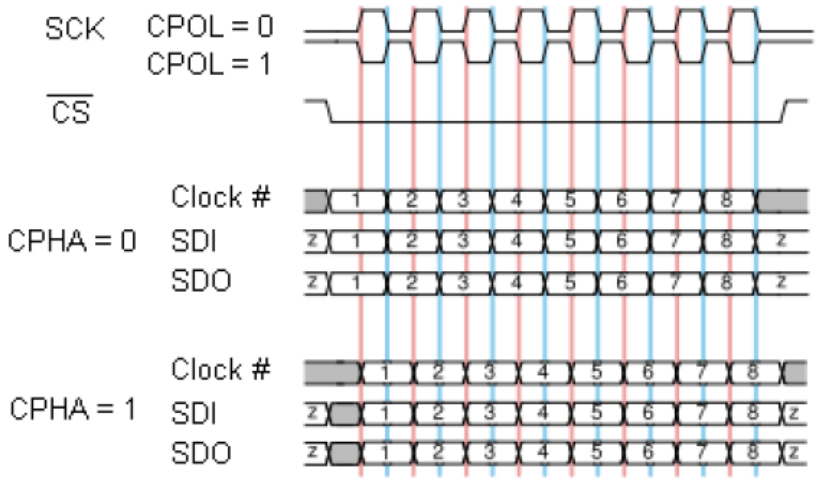


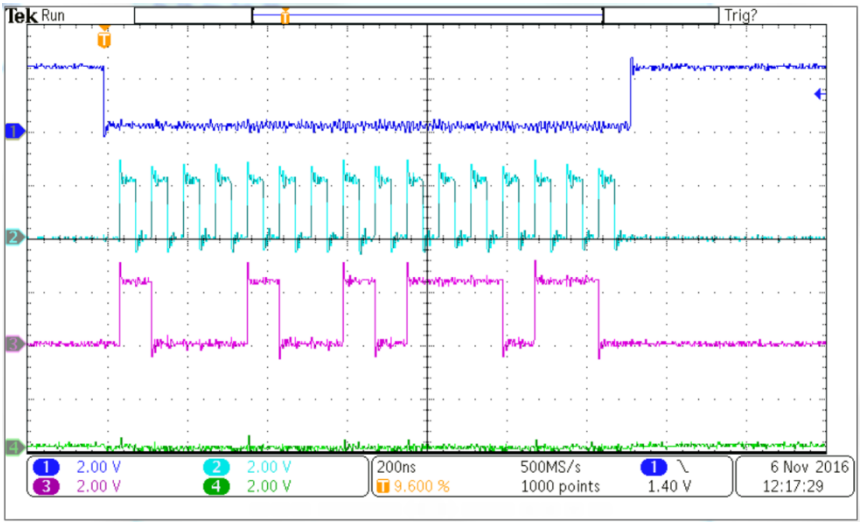
Figure 2: SPI Bus Modes

The used SPI Bus mode is of the type CPOL = 0, CPHA = 1, see figure 2.

FE_SPI_CLK	FE output that provides 16 clock cycles at each slow control access. The frequency of the clock it is not specified. Reasonable values are in the range from 500KHz to 10MHz. The electrical standard for this signal is either LVCMOS_3.3V or LVCMOS_2.5V.
FE_SPI_CE	FE output , low during the slow control access and else high. Electrical standard for this signal is either LVCMOS_3.3V or LVCMOS_2.5V.
FE_SPI_MOSI	Master output / slave input data line. A 16-bit word is transmitted at each slow control access. The most significant bit is transmitted first. The format of the 16-bit word is shown in table 1.
FE_SPI_MISO	Master input / slave output data line. A 8-bit word is transmitted at each slow control access. The most significant bit is transmitted first. In a read access, this line provides the information of the addressed register .

Bit range	Usage
15	RD = ‘0’, WR = ‘1’
14-8	Address_7..0, register address
7-0	Data_7..0, data byte

Table 1: Slow control 16 bit data field, Bit-15 (MSB) is sent first



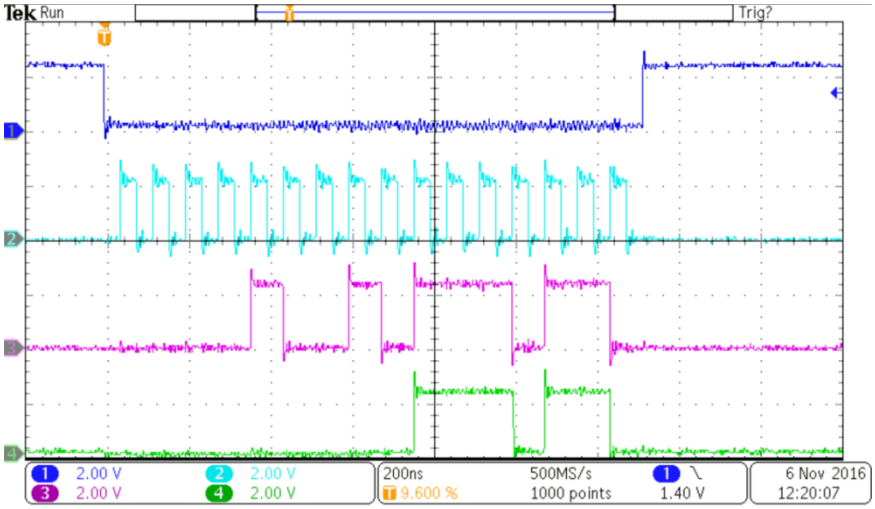
FE_SPI_CE

FE_SPI_CLK

FE_SPI_MOSI

FE_SPI_MISO

Figure 3: FEB signals, writing data 76h to address 09h at a SPI clock frequency of 12,5 MHz



FE_SPI_CE

FE_SPI_CLK

FE_SPI_MOSI

FE_SPI_MISO

Figure 4: FEB signals, reading data 76h from address 09h at a SPI clock frequency of 12,5 MHz

5 1PPS / L1A delay calibration (presently NOT IMPLEMENTED !)

Connect the RJ45 connector to J8 ("TEST_IO") and the white/brown twisted pair either to J9 ("+TIMEPPS-") or J10 ("+L1A") of the backplane to be calibrated. Connect the black/brown twisted pair to either to J9 ("+TIMEPPS-") or J10 ("+L1A") of the central backplane. Press either SW1 ("1PPS calibration") or SW2 ("L1A calibration"). A green light (V3) means, the calibration is done, a red light signalizes a failing calibration procedure. For confirmation press the unused switch.
If the calibration was successful the appropriate delay register contains the gained delay value and can get read out by software.
The RJ45 test connector ***is only available at DTB4.x****, got removed starting with DTB5.1.*

DTB4 signal	RJ45-pin	color	pair	connect to
TEST_IO2_P	4	black	1	"+" of central backplane
TEST_IO2_N	5	brown		"-" of central backplane
TEST_IO3_P	8	white	2	"+" of backplane to be calibrated
TEST_IO3_N	7	brown		"-" of backplane to be calibrated

Figure 5: calibration cable

6 Register Address Map

dec. addr.	Hex addr.	Name	Usage
0	00	CTRL	Control register
1	01	STAT	Status register
2	02	L1_SC_WIN	L1 scaler window
3	03	DEBUG	RW register for debug cases
4	04	TRIG_PULS	pulse width for up going (to CTDB) trigger pulse
5	05	TRIG_DTIM	trigger dead time
6	06	TRIG_WIN	trigger window using the leading L0-edges
7	07	PPS_DEL	1PPS input delay fine tuning in steps of 37 ps
8	08	L1A_DEL	L1A trigger (L2) input delay fine tuning in steps of 37 ps
9	09	PIXEL_SEL	Pixel select register
10	0A	L0_ DEL	L0 coarse & fine delay for the pixel selected in 1ns / 37 ps steps
11	*0B*	*L0_DEL_OFFS*	*reserved, will be implemented if required*
12	0C	L1_SCALER_L	L1 scaler in Hz, when overflow it stays at 0xFFFFh
13	0D	L1_SCALER_H	
14	0E	PPS_ERR_CT	1PPS error counter
15	0F	PPS_DEL_CAL	1PPS delay value after calibration
16	10	TRIG_MASK_0	trigger mask for the center cluster
17	11	TRIG_MASK_1	trigger mask for neighbor cluster #1
18	12	TRIG_MASK_2	trigger mask for neighbor cluster #2
19	13	TRIG_MASK_3	trigger mask for neighbor cluster #3
20	14	TRIG_MASK_4	trigger mask for neighbor cluster #4
21	15	TRIG_MASK_5	trigger mask for neighbor cluster #5
22	16	TRIG_MASK_6	trigger mask for neighbor cluster #6
23	17	L1A_SCALER_L	L1A scaler, lower 8 bit
24	18	L1A_SCALER_H	L1A scaler, upper 8 bit
25	19	L1A_BUSY_SC_L	L1A-while-BUSY scaler, lower 8 bit
26	1a	L1A_BUSY_SC_H	L1A-while-BUSY scaler, upper 8 bit
..			not used
125	7D		
126	7E	FW_REVL	Firmware Revision, bits 7..0

127	7F	FW_REVH	Firmware Revision, bits 15..8

6.1 Register Access

It is recommended to do the 1PPS delay adjustment (register PPS_DEL @ address 07) as a very first step, because it affects the FPGA internal clocks (PLL outputs).

6.2 Register Description

attribute	explanation
RW	Read / Write
RO	Read Only
RWC	Read / Write Clear (writing a '1' clears the bit)

CTRL @ address 00h, 8 bit RW, power_on_value = 0 (00h)

Bit	Attr.	Usage
3..0	RW	Trigger type select, 0 = 3NN, 1 = 1_of _7, 2 = 2_of_37, 4 = 1_of_37
4	RW	LED_ENABLE, '0' switches off all LEDs
5	RW	'1' clears the 1PPS-error counter, see reg. PPS_ERR_CT
6	RW	'1' blocks the FEB-BUSY, means it is not being propagated to the CTDB anymore, , available for DTB firmware rev. >=19
7	RW	in local clock mode '1' disables the loop back of the up going trigger to generate L1A

Use bits 0..3 to choose the trigger algorithm. After power on the 3NN trigger is functional immediately. The trigger window size is about 3ns. It can be changed by accessing the TRIG_WIN register.

The **trigger 3NN** generates a trigger, if within the 37 pixel area do exist 3 connected pixel.

The **trigger 1_of_7** generates a trigger, if one of the central cluster pixel fires.

The **trigger 2_of_37** can be used for L0 delay calibration. First the delay of the central pixel (reg. PIXEL_SEL = 03h) should be set to 7Bh , which corresponds to 4ns delay. Then, one of the surrounding 36 pixel can be selected by using the PIXEL_SEL register. By varying the L0 delay value (L0_DEL reg.), e.g. from 00h up to FBh and analyzing the trigger rate one can find the optimum delay value for the chosen pixel. This can be done for each pixel. It might be useful to adjust the trigger window size to 1 ns before.

The **trigger 1_of_37** can be used to check, if any of the 37 L0 signals is available. The PIXEL_SEL register must be used to select the pixel to be checked.

STAT @ address 01h, 8 bit RO, RWC

Bit	Attr.	Usage
0	RO	PPS_DELAY_BUSY
1	RO	L1A_DELAY_BUSY
2	RO	L0_DELAY_BUSY
3	RO	PPS_DELAY_CAL_BUSY
4	RO	PPS_ERROR
7..4	'0'	Reserved, read value is '0'

The L0_DELAY_BUSY reflects the delay status for the pixel, selected by the PIXEL_SEL register. The successful delay adjustment requires the availability of the selected signal. If the L0_DELAY_BUSY stays on, it means there was no L0 pulse to be delayed so far. Possible reasons: L0-threshold to high, broken wire, ... If a L0 delay value is written while the L0_DELAY_BUSY is on, the delay adjustment restarts with the latest value.

The L0_DELAY_BUSY is inactive, if one (accidently) tries to adjust the L0 delay for none existing pixels, e.g. when the cluster has no neighbor (outer cluster ring).

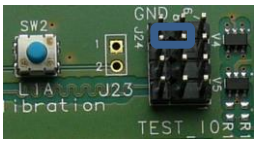
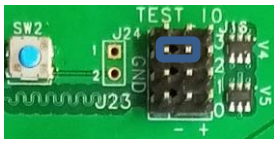
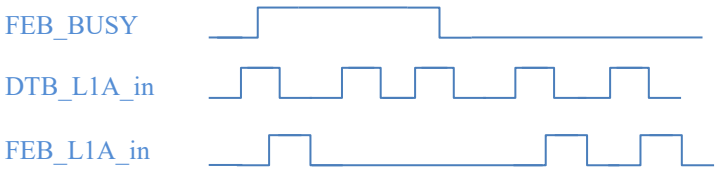
PPS_ERROR means, the register PPS_ERR_CT is not equal to zero.

L1_SC_WIN @ address 02h, 8 bit RW, power_on_value = 64h (1000 ms)

Bit	Attr.	Usage
7..0	RW	L1 scaler window size in multiples of 10 ms, writing 00h results in used / read back value of 01h, range is 10ms to 2.55 s

DEBUG @ address 03h, 8 bit RW, power_on_value = 0 (00h)

Bit	Attr.	Usage
7..0	RW	See table below

Encoding hex	description
01	L1A counter is disabled, when the FEB-BUSY is on, a jumper on TEST_IO_2 to GND overwrites this bit, see below DTB Rev4.2 and Rev.5.1. The FEB_L1A supression by the BUSY signal is depicted below.   
02	
03	

TRIG_PULS @ address 04h, 4 bit RW, 4 bit RO, power_on_value = 5 (40 ns)

Bit	Attr.	Usage
3..0	RW	up going (to CTDB) trigger signal, when 0 no pulse shaping of trigger signal !!! when 1..15, trigger pulse length in multiples of 8 ns
7..4	RO	'0'

Only for test purposes, programmable width of the up going trigger pulse.

TRIG_DTIM @ address 05h, 8 bit RW, power_on_value = 12 (0Ch)

Bit	Attr.	Usage
7..0	RW	trigger dead time in multiples of 8 ns

Trigger dead time in multiples of 8 ns (DTB system clock), default is 96ns.

TRIG_WIN @ address 06h, 3 bit RW, 5 bit RO, power_on_value = 2 (02h)

Bit	Attr.	Usage
2..0	RW	when 0 no pulse shaping of the L0 signals !!! when 1..7, pulse length of the shaped L0 signal, being used for the trigger. The trigger window = 2*x-1 ns
7..3	RO	'0'

Defines a trigger window for the leading edges of the L0 signals. This is achieved by pulse shaping the L0 (TOT) signal before they are entering the trigger fabric. Use a zero value for no pulse shaping.

PPS_DEL @ address 07h, 8 bit RW, power_on_value = 0 (00h)

Bit	Attr.	Usage
7..0	RW	1PPS input delay in multiples of 37 ps, max. range=5ns (87h)

Do the 1PPS delay adjustment as the **very first step**. It affects the DTB systems clock PLL.

L1A_DEL @ address 08h, 8 bit RW, power_on_value = 0 (00h)

Bit	Attr.	Usage
7..0	RW	L1A input delay in multiples of 37 ps, max. range=5ns (87h)

PIXEL_SEL @ address 09h, 3 bit RW, power_on_value = 0 (00h)

Bit	Attr.	Usage
2..0	RW	0..6,to select one of the pixel_0.._6
3	RO	'0'
6..4	RW	0..6,to select one of the cluster_0 .. _6
7	RO	'0'

Before adjusting the L0 delay, the appropriate pixel has to be selected, according to figure 1.

Also needed for the 1_of_37 trigger option

L0 _DEL @ address 0Ah, 5 bit RW, power_on_value = 0 (00h)

Bit	Attr.	Usage
4..0	RW	L0 input fine delay in multiples of 37 ps, pixel selected by reg. PIXEL_SEL , max. range=1ns (1Bh), additive to the coarse delay
7..5	RW	L0 input coarse delay in multiples of 1ns, pixel selected by reg. PIXEL_SEL , max. range = 7ns

Adjust the L0 delay for any of the 37 pixel, entering the trigger fabric. Use the PIXEL_SEL register first. Concerning bits 4..0 (fine delay), the L0_DELAY_BUSY (STAT-reg. bit_2) must be checked for readiness. Note that the delay procedures for a value of n (1..31) needs about 2..64 L0-pulses to get ready (L0_DELAY_BUSY = '0'). To get 1ns the useful max. value is 1Bh. Higher values results in some additional delay.

For bits 7..5, the coarse delay, the L0_DELAY_BUSY polling is **not necessary** ! It is functional immediately after the L0_DEL register write operation.

The delay setting is **identical for all clusters**. An extra offset for the central cluster is **not needed** anymore.

L0 _DEL _OFFS @ address 0Bh, 3 bit RW, power_on_value = 0 (00h)

Bit	Attr.	Usage
2..0	RW	L0 input coarse delay offset in multiples of 37 ps, pixel selected by reg. PIXEL_SEL , max. range=7ns
7..3	RO	'0'

L0 delay offset register, reserved, will be implemented, if required. This register can be used for rough equalizing of the L0 delay of all 37 pixels, just once after power on. This results in an equal delay range of +/-4 ns for each pixel, using the L0_DEL register.

L1_SCALER_L @ address 0Ch, 8 bit RO, power_on_value = 0 (00h)

Bit	Attr.	Usage
7..0	RO	binary frequency in Hz, lower 8 bit

L1_SCALER_H @ address 0Dh, 8 bit RO, power_on_value = 0 (00h)

Bit	Attr.	Usage
7..0	RO	binary frequency in Hz, upper 8 bit

PPS_ERR_CT @ address 0Eh, 8 bit RO, power_on_value = 0 (00h)

Bit	Attr.	Usage
7..0	RO	amount of consecutive 1PPS mismatches with respect to the DTB system clock, when overflow it stays at FFh

Presently, the 10MHz provided by the TIB are converted to 50MHz at the L2 crate and distributed to the DTBs, to be used as common system clock. Note, that the 1PPS delivered by the TIB must be synchronous to the 10MHz !

The counter increments, if the amount of DTB system clock (50 MHz) cycles between consecutive 1PPS signals is not exactly 50 Mio. When overflowing it stays at FFh.

Use CTRL-reg. bit_5 to clear the PPS_ERR_CT.

PPS_DEL_CAL @ address 0Fh, 8 bit RO, power_on_value = 0 (00h)

Bit	Attr.	Usage
7..0	RO	1PPS delay value after calibration

Trigger masking takes place directly at the FPGA inputs. Writing a ‘0’ to the appropriate bit position of the trigger mask register enforces a zero level for the incoming L0 signal. When writing FFh, the read back value corresponds to the pixel (numbers), which can get masked. The trigger mask applies for all trigger modes.

TRIG_MSK_0 @ address 10h, 7 bit RW, 1 bit RO, power_on_value = 127 (7Fh)

Bit	Attr.	Usage
6..0	RW	trigger mask for the central cluster, write '0' to disable the selected pixel
7	RO	'0'

TRIG_MSK_1 @ address 11h, 5 bit RW, 3 bit RO, power_on_value = 62 (3Eh)

Bit	Attr.	Usage
0	RO	'0'
5..1	RW	trigger mask for cluster #1, pixel #5..1
7..6	RO	'0'

TRIG_MSK_2 @ address 12h, 5 bit RW, 3 bit RO, power_on_value = 124 (7Ch)

Bit	Attr.	Usage
1..0	RO	'0'
6..2	RW	trigger mask for cluster #2, pixel #6..2
7	RO	'0'

TRIG_MSK_3 @ address 13h, 5 bit RW, 3 bit RO, power_on_value = 121 (79h)

Bit	Attr.	Usage
0	RW	trigger mask for cluster #3, pixel #0
2..1	RO	'0'
6..3	RW	trigger mask for cluster #3, pixel #6..3
7	RO	'0'

TRIG_MSK_4 @ address 14h, 5 bit RW, 3 bit RO, power_on_value = 107 (6Bh)

Bit	Attr.	Usage
1..0	RW	trigger mask for cluster #4, pixel #1..0
2	RO	'0'
3	RW	trigger mask for cluster #4, pixel #3
4	RO	'0'
6..5	RW	trigger mask for cluster #4, pixel #6..5
7	RO	'0'

TRIG_MSK_5 @ address 15h, 5 bit RW, 3 bit RO, power_on_value = 79 (4Fh)

Bit	Attr.	Usage
3..0	RW	trigger mask for cluster #5, pixel #3..0
5..4	RO	'0'
6	RW	trigger mask for cluster #5, pixel #6
7	RO	'0'

TRIG_MSK_6 @ address 16h, 5 bit RW, 3 bit RO, power_on_value = 127 (h)

Bit	Attr.	Usage
4..0	RW	trigger mask for cluster #6, pixel #4..0
7..5	RO	'0'

L1A_SCALER_L @ address 17h, 8 bit RWC, power_on_value = 0 (00h)

Bit	Attr.	Usage
7..0	RO	L1A scaler, lower 8 bit, any write clears both L1A_SCALER_x registers

L1A_SCALER_H @ address 18h, 8 bit RWC, power_on_value = 0 (00h)

Bit	Attr.	Usage
7..0	RO	L1A scaler, upper 8 bit, any write clears both L1A_SCALER_x registers

L1A_BUSY_SC_L @ address 19h, 8 bit RWC, power_on_value = 0 (00h)

Bit	Attr.	Usage
7..0	RO	L1A-while-busy scaler, lower 8 bit, any write clears both L1A_BUSY_SC_x registers

L1A_BUSY_SC_H @ address 1Ah, 8 bit RWC, power_on_value = 0 (00h)

Bit	Attr.	Usage
7..0	RO	L1A-while-busy scaler, upper 8 bit, any write clears both L1A_BUSY_SC_x registers

FW_REVL @ address 7Eh, 8 bit RO

Bit	Attr.	Usage
7..0	RO	read back of the firmware revision, bits 7..0

FW_REVH @ address 7Fh, 8 bit RO

Bit	Attr.	Usage
7..0	RO	read back of the firmware revision, bits 15..8