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| **L2CB Slow Control Switch ICD** |

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| **List of Abbreviations** |
| SPI | Serial Peripheral Interface | RW | Read / Write |
| L2CB | L2 Controller Board  | RO | Read Only |
| CTDB | Clock & Trigger Distribution Board | RWC | Read / Write Clear |
| L2BP | L2 Crate Backplane | 76h | 76 hexadecimal |
| LVDS | Low Voltage Digital Signalling |  |  |

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| **History** |
| Version | Date | Observation |
| 1 | 24/10/2020 | Draft |
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| **Distribution** |  |

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# Introduction

This document describes the slow control interface between the L2CB board and the CTDBs. E.g. to power on a FEB or to monitor the FEBs current, one has to access the appropriate CTDB registers via the L2BPs SPI bus.

# L2CB Interfaces

## Ethernet to FPGA

The microcontroller based unit Stamp9G45 is used as a 100MBit Ethernet to FPGA-bridge. It shares a 16 bit memory bus interface with the FPGA.

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| **Figure 1**: Stamp9G45 |

To communicate with each of the 18 CTDBs a shared SPI bus is implemented. The L2CB is the bus master.

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## SPI Bus, CTDB Access via L2BP

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| **Figure 2**: SPI Bus Modes. The used SPI Bus mode is of the type CPOL = 0, CPHA = 1 |

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| **L2 Backplane, SPI Bus signals** |
| SPI\_SCLK | L2CB output that provides 32 clock cycles at each slow control access. The frequency of the clock it is 6.25 MHZ . The electrical standard for this signal is LVDS. Other frequencies are possible. |
| SPI\_SYNCn | L2CB output , low during the slow control access and else high. Electrical standard for this signal is LVDS. |
| SPI\_MOSI | Master output / slave input data line. A 32-bit word is transmitted at each slowcontrol access. Electrical standard for this signal is LVDS.The most significant bit is transmitted first. The format of the 32-bit word is shown in table 1. |
| SPI\_MISO | Master input / slave output data line. Electrical standard for this signal is LVDS.A 16-bit word is transmitted at each slow control access. The most significant bit is transmitted first. Active at a read access, else tristated. This line provides the information of the addressed CTDB register. |

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| Bit range | Usage |
| 31 | RD = ‘0’, WR = ‘1’ |
| 30-16 | Address\_14..0, register address |
| 15-0 | Data\_15..0, data word |

**Table 1**: Slow control 16 bit data field, Bit-15 (MSB) is sent first

|  |  |
| --- | --- |
|  | SPI\_SYNCn |
| SPI\_MOSI |
| SPI\_MISO |
| SPI\_SCLK |
| **Figure 3**: Example, writing data 4321h to address 4f55h  |
|  | SPI\_SYNCn |
| SPI\_MOSI |
| SPI\_MISO |
| SPI\_SCLK |
| **Figure 4**: Example, reading data 8765h to address 68aah  |

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# L2CB Registers, Used for Slow Control

|  |  |  |
| --- | --- | --- |
| **hex addr.** | **Name** | **Usage** |
| 02 | STAT | Status register |
| 04 | SPAD | SPI Address register |
| 06 | SPTX | SPI Tx Data register |
| 08 | SPRX | SPI Rx Data register |

The registers can be accessed through the Stamp9G45 module via ethernet or RS232

## L2CB Register Description

|  |  |
| --- | --- |
| **attribute** | **explanation** |
| RW | Read / Write |
| RO | Read Only |
| RWC | Read / Write Clear (writing a ‘1’ clears the bit) |

**STAT** @ address 02h, 16 bit RO, RWC, power\_on\_value = 0 (0000h)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 0 | RO | ‘1’= SPI bus cycle busy |
| 1 | RO | ‘1’= L1 delay set busy |
| 15..2 | ‘0’ | Reserved, read value is ‘0’ |

Status bits to poll on the readiness of the operation.

Any write operation to the SPAD register initiates a SPI cycle. For SPI write operations, **data have to be written to the SPTX register first !** Before initiating the next SPI cycle **check STAT-bit\_0** (polling on readiness).

**SPAD** @ address 04h, 13 bit RW, power\_on\_value = 0 (0000h)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 7..0 | RW | CTDB register address |
| 12..8 | RW | L2-Crate, CTDB slot number: 1..9, 13..21 |
| 14..13 | ‘0’ | Reserved, write ‘0’ |
| 15 | RW | ‘1’ = Write cycle, ‘0’ = Read cycle |

**SPTX** @ address 06h, 16 bit RW, power\_on\_value = 0 (0000h)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 15..0 | RW | SPI (CTDB register ) data, to be sent |

**SPRX** @ address 08h, 16 bit RO, power\_on\_value = 0 (0000h)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 15..0 | RO | SPI (CTDB register ) data received |

## CTDB Register Address Map

|  |  |  |
| --- | --- | --- |
| **hex addr.** | **Name** | **Usage** |
| 00 | PONF | Power On / Off register |
| 01 | CUR\_01 | value \* 0.485 = FEB\_24V\_current in mA, RJ45 ports 1..15, |
| ... |  |
| 0F | CUR\_15 |
| 10 | CUR\_00 | value \* 0.485 = CTDB\_(own)\_24V\_current in mA |
| 11 | CUR\_MIN | FEB current, lower limit |
| 12 | CUR\_MAX | FEB current, upper limit |
| 13 | OVER\_CUR | over current detected |
| 14 | UNDER\_CUR | under current detected |
|  |  |  |
| 20 | CTRL | control register for common usage |
| 21 | STAT | status register for common usage |
|  |  |  |
| FB | PON\_TIME | time in ms, to disable the firmware fuse after power on |
| FC | POFF\_TIME | time in ms, after power down, before the next power on is possible |
| FD | ADC\_SRATE | ADC (cur. measurement) sampling rate |
| FE | DEBUG | to program the usage of the test pins SEL0..3 |
| FF | FREV | Firmware Revision, bits 15..0 |

For details check the CTB\_user\_manual.

# FEB Powering by CTDB Access

Before powering the FEBs, the minimum and maximum current values have to be written (initialization) to the registers CUR\_MIN and CUR\_MAX first. To power on a dedicated CDTB channel one has to set the appropriate bit of the PONF register. The state machine goes to the state POWERING\_ON. In this state the electronic fuse (continuous current check by ADC) is disabled. The unavoidable current peak would result in an immediate power off switching. After 50ms (default, programmable, see reg. PON\_TIME) the state machine changes to the POWER\_ON state.

Now the current is monitored, can get read out, using the registers CUR\_01 to CUR\_15. In case of a power failure for a particular channel, its power is switched off automatically. The failure status is kept in the registers OVER\_CUR and UNDER\_CUR until the appropriate bit of the PONF register is cleared, resulting in the state transition from POWER\_FAIL to POWERING\_OFF. This state will be left after 60ms (default, programmable, see reg. POFF\_TIME).

The POWERING\_OFF state is also involved, when a regular power off by software occurs. It is required, to ensure, that all capacitors are completely discharged (+24V -> 0V), before repowering the FEB again. A clean power up ramp is needed for a proper FEBs FPGA load.

POWER

OFF

POWERING

ON

POWER ON

POWERING

OFF

POWER

OFF

POWERING ON

24V=ON

Software

power-on

power-on

timer exp.

Over\_cur. or

Under\_cur.

Software

power-off

Software

power-off

POWER ON

24V=ON

POWER FAIL

24V=OFF

POWERING OFF

24V=OFF

power-off

timer exp.

POWER OFF

24V=OFF

# CTDB Power Switch and Current Monitoring Circuitry

