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| **CTDB-L2Crate Interface Definition** |

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| **Karl-Heinz Sulanke DESY** | |  |  | |
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| **List of Abbreviations** | | | |
| CTDB | Clock & Trigger Distribution Board |  |  |
| DTB | Digital Trigger Backplane |  |  |
| FEB | Frontend Board |  |  |
| L2BP | L2 Crate Backplane |  |  |
| LVDS | Low Voltage Digital Signalling |  |  |
| MISO | master in slave out |  |  |
| MOSI | master out slave in |  |  |
| PPS | Pulse Per Second |  |  |
| SPI | Serial Peripheral Interface |  |  |

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| **History** | | |
| Version | Date | Observation |
| 01 | 21/10/2020 | Draft |
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| **Distribution** |  |

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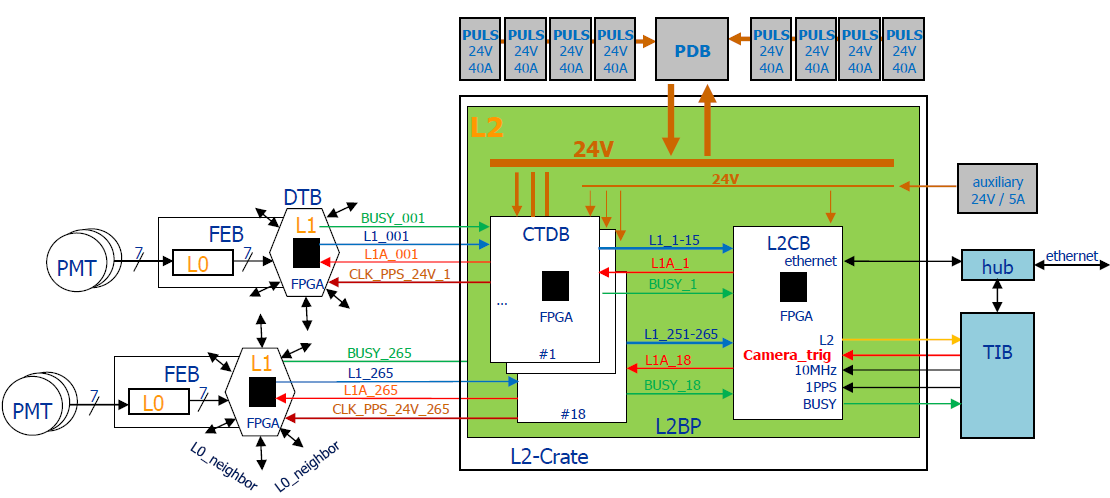
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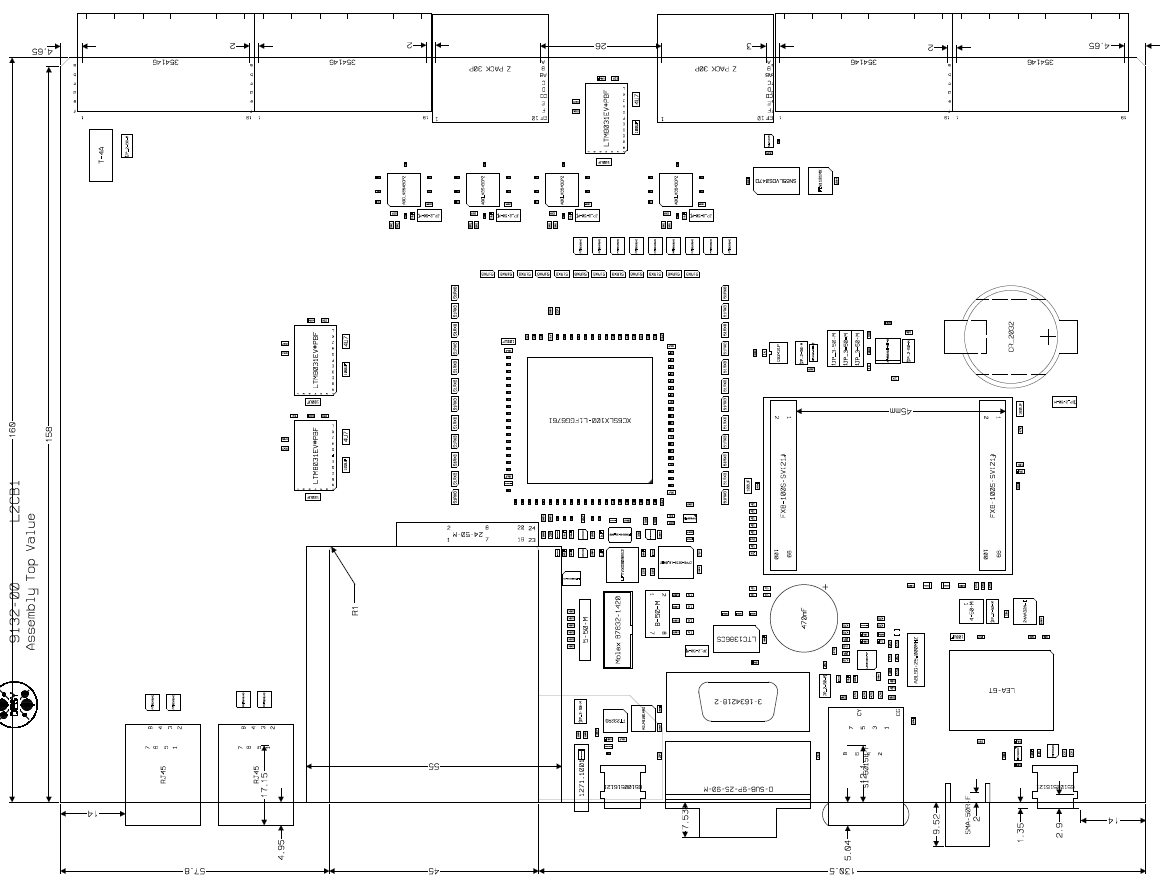
# Introduction

This document describes the interface between the L2CB and theL2Crate, see



# Mechanics

The L2CB is a 6U standard size card, 160 x 233.3 mm, fits into a 20.32mm grid (sliding rails grid).



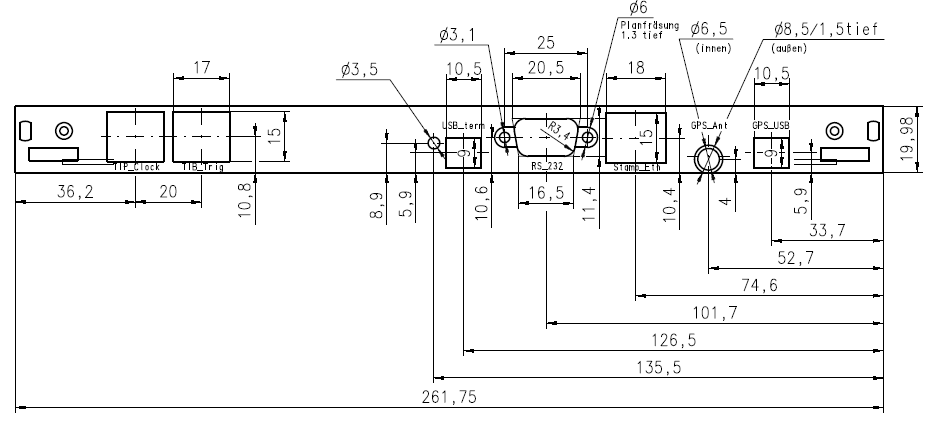
**L2BP**

**Conn.**

**Frontpanel**

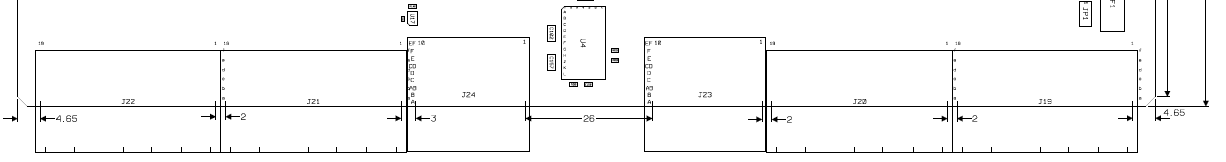
**Conn.**

## Frontpanel

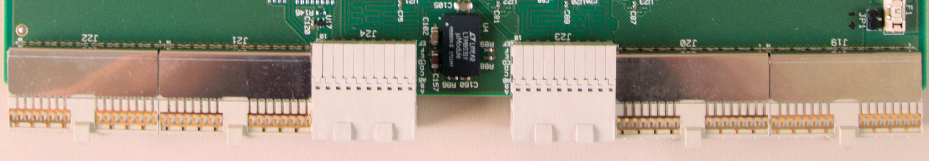


## Connector Arrangement

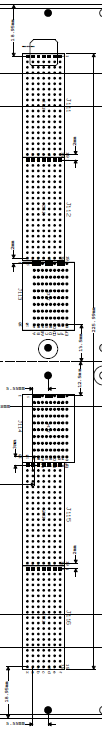
Two connectors at the back side of the card establishing the L2BP connections. J19 to J22 are being used for single ended signals, J23, J24 are carrying differential signals.



**L2CB**



**L2BP**



# Connector Types

Press fit types

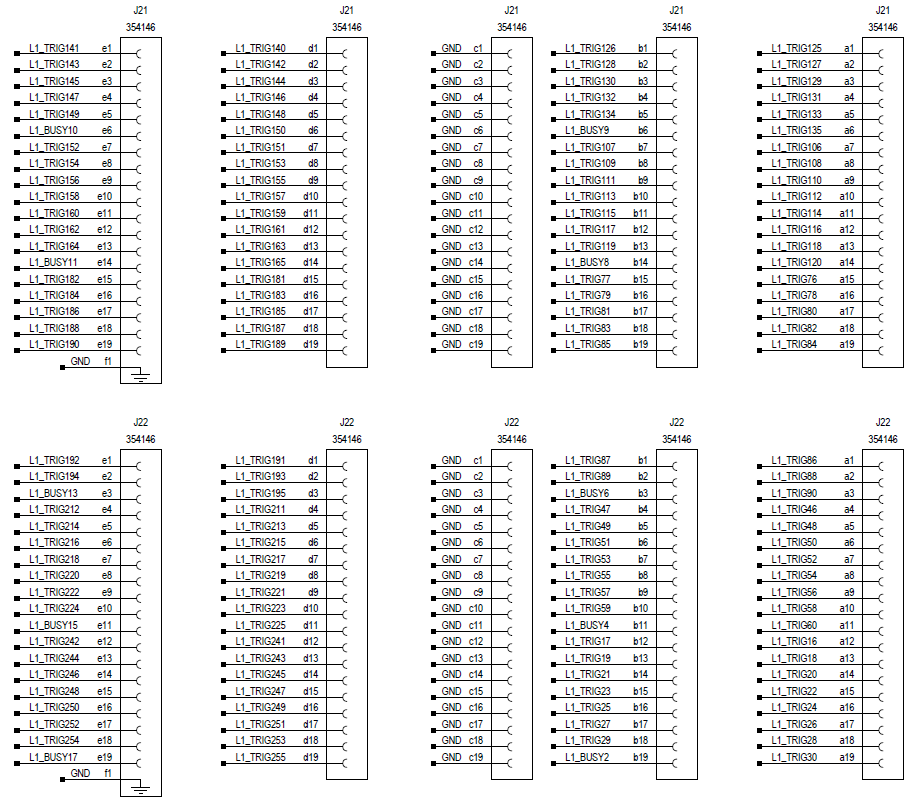
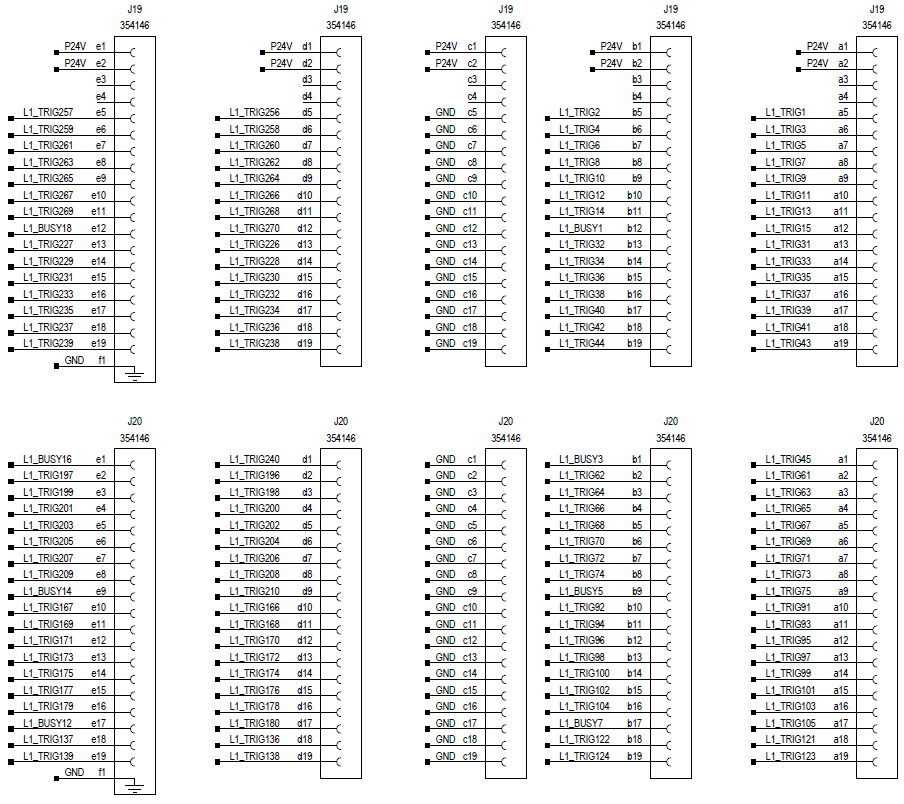
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| --- | --- | --- | --- | --- | --- |
| **side** | **connector type** | **manufacturer** | **man.-ID** | **RefDes & usage** |  |
| L2CB | Z-Pack, right angle | ERNI | 354146 | J19, J20, J21, J22  trigger & busy  signals  aux. +24V  GND |  |
| L2CB | Z-Pack, right angle | TE Connectivity | 6469081-1 | J23, J24,  clock, pps and L2 trigger  signals |  |
| L2BP | Z-Pack, straight | TE Connectivity | 6469083-1 | J113, J114 |  |
| L2BP | Z-Pack, straight | TE Connectivity | 5646532-1 | J111, J112,  J115, J116 |  |

# Connectors, Pin Usage and Signal Description

## L2CB Backplane Connectors J19, J20, J21, J22, Signals

see also L2CB schematic, sheet “conns”

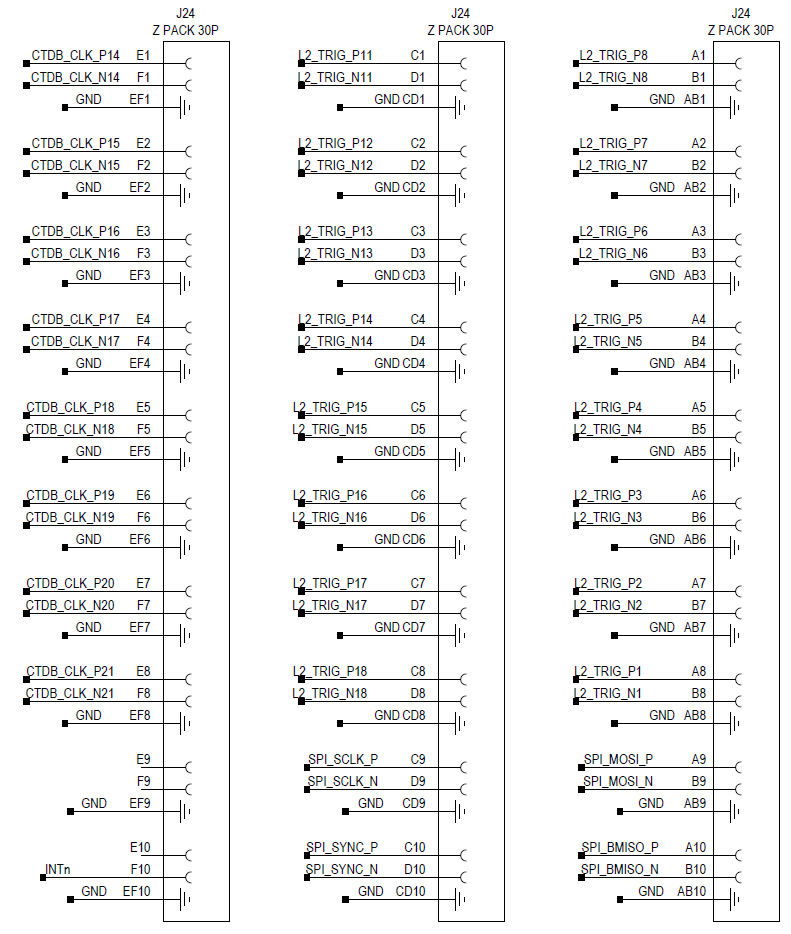
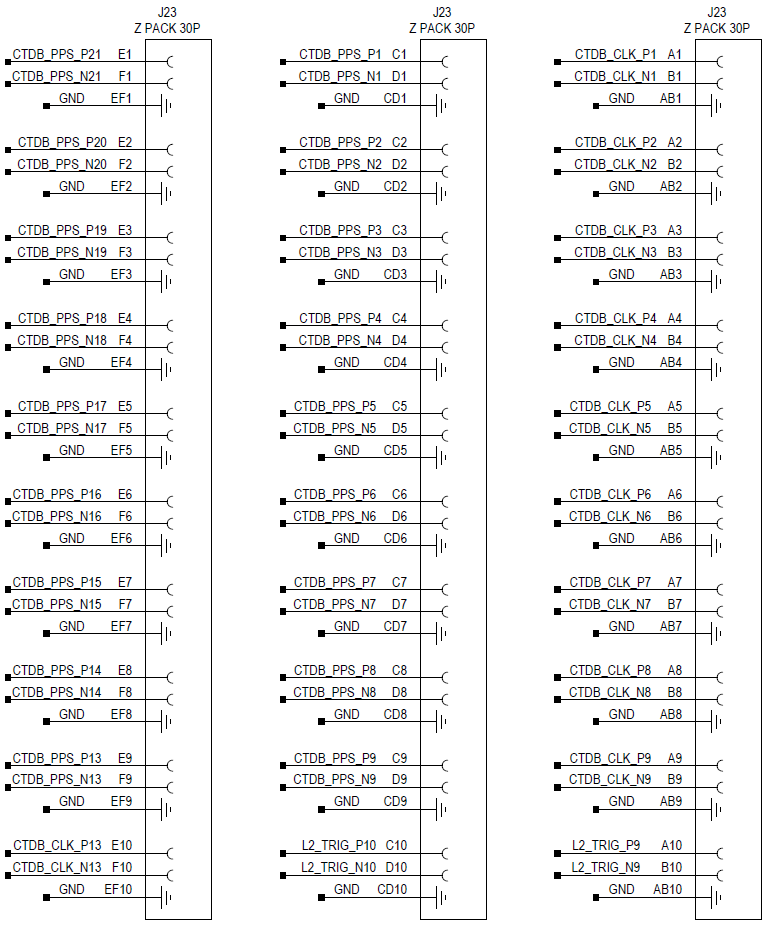
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| --- | --- | --- | --- |
| **signal** | **level** | **direction** | **description** |
| **L1\_TRIGxxx** | 1.2V | input | 51ohm termination to GND, up going L1-trigger, connected to FPGA |
| **L1\_BUSYxx** | 1.2V | input | 51ohm termination to GND, up going FEB-Busy, connected to FPGA |
| **P24V** | +24V | input | by auxiliary power supply |
| **GND** |  |  |  |



## L2CB Backplane Connectors J23, J24, Signals

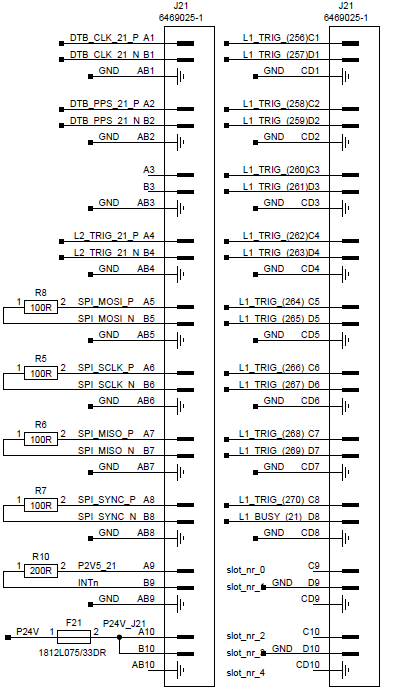
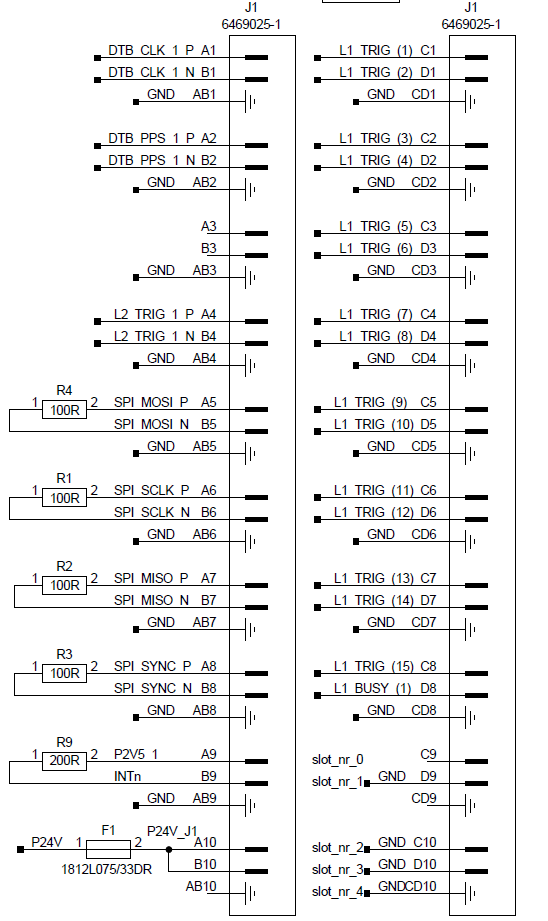
see also L2CB schematic, sheet “diffs”

|  |  |  |  |
| --- | --- | --- | --- |
| **signal** | **level** | **direction** | **description** |
| **CTDB\_CLK\_Pxx/Nxx** | LVDS | output | driven by fan out chip ADCLK854BCPZ |
| **CTDB\_PPS\_Pxx/Nxx** | LVDS | output | driven by fan out chip ADCLK854BCPZ |
| **L2\_TRIG\_Pxx\_Nxx** | LVDS | output | L1A provided by the TIB and fan out by the FPGA |
| **SPI\_SYNC\_P/N** | LVDS | output | used for CTDB register access, from FPGA, driven by driver IC SN65LVDS047D |
| **SPI\_CLK\_P/N** | LVDS | output |
| **SPI\_MOSI\_P/N** | LVDS | output |
| **SPI\_MISO\_P/N** | LVDS | input | received by IC FIN1101MX, to FPGA |
| **INTn** | 1.8V | input | shared CTDB interrupt line, received by IC 74LVC1G125, connected to FPGA |
| **GND** |  |  |  |



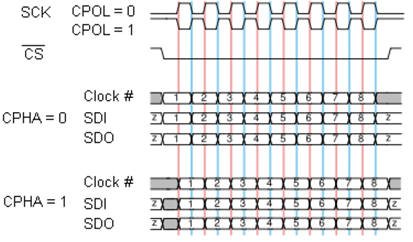
## L2BP Backplane SPI Bus and Interrupt Signal Termination

see also L2BP schematic. The SPI bus and the interrupt (INTn) are terminated at slot\_1 and slot\_21. So far, the INTn signal is not being used.



# SPI Bus

All slow control is achieved, by using the L2BP-SPI bus, controlled by the L2CBs FPGA.



SPI Bus Modes. The used SPI Bus mode is of the type: CPOL = 0, CPHA = 1

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| **L2 Backplane, SPI Bus signals** | |
| **SPI\_SCLK** | L2CB output that provides 32 clock cycles at each slow control access. The frequency of the clock it is 6.25 MHZ . The electrical standard for this signal is LVDS. Other frequencies are possible. |
| **SPI\_SYNCn** | L2CB output , low during the slow control access and else high. Electrical standard for this signal is LVDS. |
| **SPI\_MOSI** | Master output / slave input data line. A 32-bit word is transmitted at each slow  control access. Electrical standard for this signal is LVDS.  The most significant bit is transmitted first. The format of the 32-bit word is shown in table 1. |
| **SPI\_MISO** | Master input / slave output data line. Electrical standard for this signal is LVDS.  A 16-bit word is transmitted at each slow control access. The most significant bit is transmitted first. Active at a read access, else tristated. This line provides the information of the addressed CTDB register. |

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| **Bit range** | **Usage** |
| 31 | RD = ‘0’, WR = ‘1’ |
| 30..29 | ‘0’, not used |
| 28..24 | slot address 4..0 (1..9, 13..21) |
| 23..16 | CTDB register address 7..0 |
| 15..0 | CTDB register data 15..0 |

Bit-31 (MSB) is sent first

## SPI Bus Timing

Measured SPI bus cycles are illustrated below. The Bus cycle time is about 5.4 us. Higher rates can be achieved by adapting the L2CB firmware accordingly.

|  |  |  |  |
| --- | --- | --- | --- |
| SPI\_SYNC | | write_0x1234_slot2_rg_addr_0x20 | |
| SPI\_SCLK | |
| SPI\_MOSI | |
| SPI\_MISO | |
|  | |
| Measured, SPI write cycle of 1234h to address 20h of CTDB at slot 2 | | | |
|  | | | |
| SPI\_SYNC | | read_0x1234_slot2_rg_addr_0x20 | |
| SPI\_SCLK | |
| SPI\_MOSI | |
| SPI\_MISO | |
|  | |
| Measured, SPI read of 1234h from address 20h of CTDB at slot 2 | | | |