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| **Digital Trigger Backplane, Firmware** |

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| **List of Abbreviations** | | | |
| L2CB | L2-crate Controller Board | PLL | Phase Locked Loop |
| DTB | Digital Trigger Backplane | L1A | L1 trigger Accepted |
| FEB | Frontend Board | DCM | Digital Clock Manager |
| SPI | Serial Peripheral Interface | MCU | Microcontroller Unit |
| FPGA | Field Programmable Gate Array |  |  |
| TIB | Trigger Interface Board |  |  |
| CTDB | Clock & Trigger Distribution Board |  |  |
| PPS | Pulse Per Second |  |  |
| L2BP | L2-crate Backplane |  |  |

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| **History** | | |
| Version | Date | Observation |
| 01 | 18/05/2020 | Draft |
| 02 | 18/10/2020 | final |
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| **Distribution** |  |

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# Introduction

This document describes the basic functionality of the L2CB1’s firmware, valid for firmware Rev. l2cb1\_005**.**

# FPGA

The FPGA of the type Xilinx XC6SLX100-L1FGG676I is the main part of the L2CB. After power on, it can get loaded from a serial Flash (AT45DB321E-SHF-B). The latter can be updated via a JTAG connection, using Xilinx programming hardware (e.g. Platform Cable USB II).

The mostly used way is to load the configuration by an onboard MCU (Stamp9G45). This way, the FPGA image can be reloaded / updated any time by software.

# Firmware Description

## Clock and PPS Fanout

The FPGA receives a 10MHz clock and a PPS signal, provided by the TIB. The PPS is doubled by the FPGA, to provide two external fan out chips with their input signals. Internal programmable delay stages are used to compensate for the output skew of both signals.

A DCM generates 50MHz from the TIBs10MHz clock. A PLL generates several system clocks from the 50MHz.Two oserdes stages plus output delays are being used to generate the 50MHz to be distributed via the L2BP to the 18 CTDBs. For test purposes (absence of a TIB) artificial TIB\_CLK /\_PPS are being generated, using a local oscillator.

## L1 Trigger Processing

270 (5 redundant) L1 trigger signals, driven by 18 CTDBs, are directly connected to the FPGA. To compensate for FPGA internal delays, each L1 triggers passes an in-system programmable delay line. Next stage is a 270 bit trigger mask, allowing to disable male functioning or not used (calibration) trigger signals. Finally, all L1 triggers are connected to a 270-input OR. The output signal of this big OR is pulse shaped (52ns) and sent to the TIB.

## L2 Trigger Fanout

The camera trigger, delivered by the TIB, gets fan out (1 to 18) and according to the systematic skew, corrected by delay stages, before being passed to the L2BP.

## BUSY Signals

An OR of the 18 BUSY signals of the CTDBs is directly propagated to the TIB.

## MCU Interface

The FPGA is connected to the MCU (piggy back module) Stamp9G45 by a SRAM like bus, comprising 20 address lines, 16 data lines and control signals. Address decoder and read / write control logic is implemented to access the 18 registers, being used right now.

## Register Block

18 16-Bit register are being used for status and control, SPI bus (L2BP) control, L1-trigger masking, testing and firmware revision read back. For test purposes a 48-bit time stamp register is implemented.

## CTDB Access via L2BP

The L2CB, as the SPI master, is controlling the L2BPs SPI bus. This way any register of any of the 18 CTDBs can get accessed. The data flow is: Ethernet-MCU-L2CB\_FPGA-L2BP-CTDB\_FPGA.

## L2CB Firmware, Block Diagram

BUSY from CTDBs

L1 from CTDBs

TIB\_TRIG

TIB\_CAM\_TRIG

odelay

fanout

SPI

ctrl

Register

block

Local CLK2

DCM

counter

TIB\_CLK

L2BP\_CLK

odelay

TEST\_TIB\_CLK

TEST\_TIB\_PPS

DCM

PLL

oserdes

TIB\_PPS

L2BP\_PPS

odelay

OR

18

TIB\_BUSY

270

idelay

mask

OR

pulse

Address

decoder

Rd / Wr

control

MCU\_ADR

MCU\_DATA

MCU\_BCTRL

L2BP\_SPI

L2 to CTDBs

Local CLK1

PLL

## FPGA Occupancy, Firmware Rev. l2cb1\_005

Copied from the ISE Place and Route Report

Device Utilization Summary:

Slice Logic Utilization:

Number of Slice Registers: 7,765 out of 126,576 6%

Number used as Flip Flops: 7,765

Number used as Latches: 0

Number used as Latch-thrus: 0

Number used as AND/OR logics: 0

Number of Slice LUTs: 7,740 out of 63,288 12%

Number used as logic: 7,469 out of 63,288 11%

Number using O6 output only: 4,953

Number using O5 output only: 78

Number using O5 and O6: 2,438

Number used as ROM: 0

Number used as Memory: 2 out of 15,616 1%

Number used as Dual Port RAM: 0

Number used as Single Port RAM: 0

Number used as Shift Register: 2

Number using O6 output only: 2

Number using O5 output only: 0

Number using O5 and O6: 0

Number used exclusively as route-thrus: 269

Number with same-slice register load: 266

Number with same-slice carry load: 3

Number with other load: 0

Slice Logic Distribution:

Number of occupied Slices: 3,823 out of 15,822 24%

Number of MUXCYs used: 2,332 out of 31,644 7%

Number of LUT Flip Flop pairs used: 9,510

Number with an unused Flip Flop: 2,347 out of 9,510 24%

Number with an unused LUT: 1,770 out of 9,510 18%

Number of fully used LUT-FF pairs: 5,393 out of 9,510 56%

Number of slice register sites lost

to control set restrictions: 0 out of 126,576 0%

## Timing Constraints

#Copied from the file L2CB\_005.ucf

#

NET "QOSC1\_OUT" TNM\_NET = "qosc1\_clk";

TIMESPEC "TS\_qosc1\_clk" = PERIOD "qosc1\_clk" 40 ns HIGH 50%;

#

NET "QOSC2\_OUT" TNM\_NET = "qosc2\_clk";

TIMESPEC "TS\_qosc2\_clk" = PERIOD "qosc2\_clk" 100 ns HIGH 50%;

#

NET "TIB\_CLK\_P" TNM\_NET = "tib\_clk";

TIMESPEC "TS\_tib\_clk" = PERIOD "tib\_clk" 100 ns HIGH 50%;

#NET "TIB\_PPS\_P" OFFSET = IN 93 ns VALID 100 ns BEFORE "TIB\_CLK\_P";

#

#

PIN L1\_TRIG\* TNM = l1\_trigger;

PIN LVDS\_IO\_P<3> TNM = tib\_trigger;

TIMESPEC TS\_l1\_delay = FROM "l1\_trigger" TO "tib\_trigger" 28.0 ns;# DATAPATHONLY;

#

NET "TIB\_EVENT\_T\_P" CLOCK\_DEDICATED\_ROUTE = TRUE;

#

NET "EBI1\_NWE" CLOCK\_DEDICATED\_ROUTE = TRUE;

NET "EBI1\_NRD" CLOCK\_DEDICATED\_ROUTE = TRUE;

#