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| DTS Performance Verification |

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| **List of Abbreviations** | | | |
| DTS | Digital Trigger System |  |  |
| CTDB | Clock & Trigger Distribution Board |  |  |
| DTB | Digital Trigger Backplane |  |  |
| FEB | Frontend Board |  |  |
| L2BP | L2 Crate Backplane |  |  |
| L2CB | L2 Crate Controller Board |  |  |
| TOT | Time over Threshold |  |  |
| PMT | Photo Multiplier Tube |  |  |
| NSB | Night Sky Background |  |  |
|  |  |  |  |

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| **History** | | |
| Version | Date | Observation |
| 01 | 21/10/2020 | Draft |
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| **Distribution** |  |

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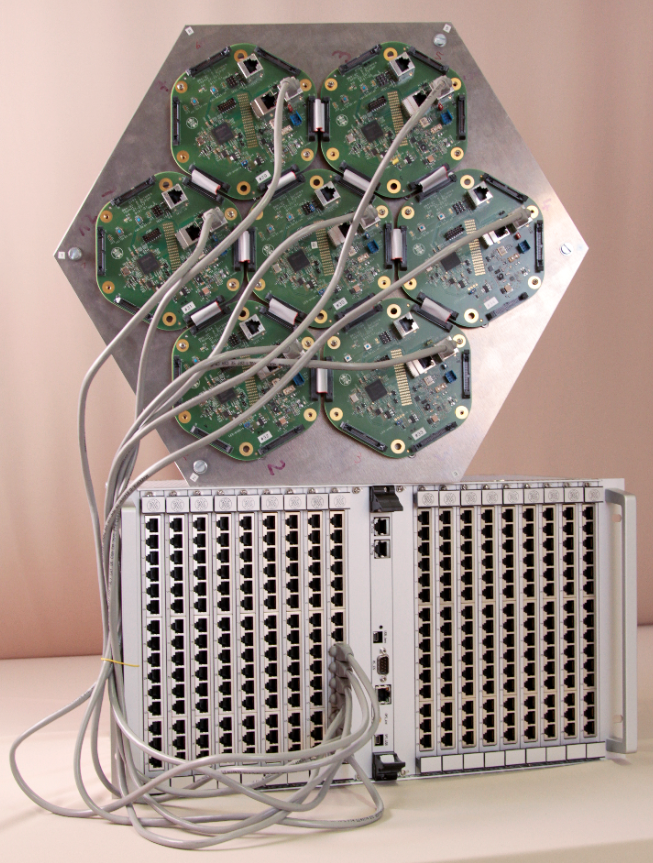
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# Introduction

This document describes the measures used, to test DTS systems performance. Most of the tests have been performed, using the 7 cluster test setup at DESY.

# DESY Test Setup



# Items to be tested

|  |  |
| --- | --- |
| **Item** | **remark** |
| Clock and PPS distribution | skew and jitter |
| L0 delay adjustment | for optimum trigger performance |
| 3NN trigger vs. trigger window | overlapping 37 pixel regions |
| Trigger timing | up an down going trigger, skew and jitter |
| Trigger jitter at TIB input |  |

# Clock and PPS Distribution

To measure the PPS and clock deviation (skew) 3 CTDBs (45 channels) were investigated. With the help of the Tektronix scope MDO3104 (1Ghz, 5GS/s) the measurements were taken. One has to consider, that for measuring skews in the range of some hundred 100ps, this test setup has a limited accuracy.

To investigate the L2Crate (CTDB) channel to channel skew, two DTB4s, one with a fixed connection to L2-crate slot 1, channel 1, the other plugged to the remaining channels, have been used.

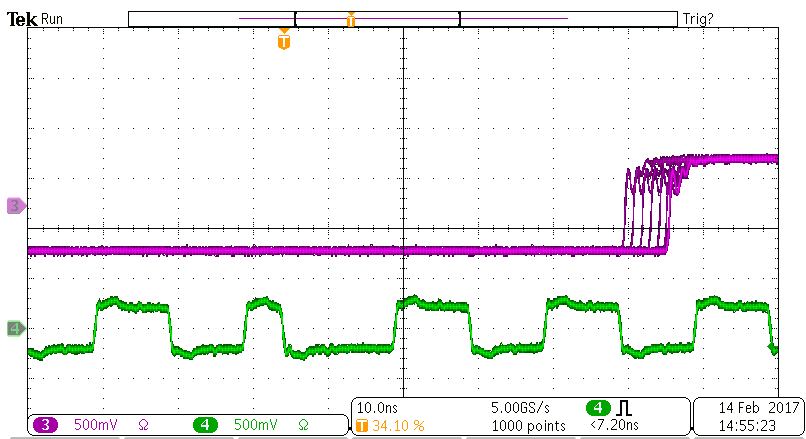


The signal TIMEPPS was probed next to the FEB connector.

Typical values, in ps are shown on the right.

The maximum skew found was **140 ps.**

These measurements are showing, that the initial power-on-accuracy of the PPS signal is already very good. Further reduction of the skew is achieved by tuning the PPS delay of each channel by software (see DTB\_user\_manual). The measurement below shows the received input clock, modulated with the PPS signal (green) and the FEBs PPS (purple). The PPS delay got tuned (in steps of 1ns for better visibility). The minimum step size is 37ps, the range about 7ns.

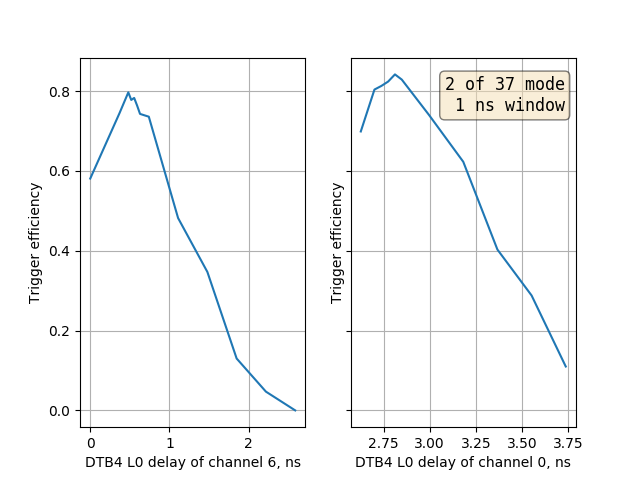


# L0 Delay Adjustment

The DTBs FPGA is processing the L0 (TOT) signals of a 37 pixel region. For the proper functionality it is essential, that all L0 signals hit the trigger logic at the same time. The PCB traces are tuned to be equal by a tolerance better than +/- 1mm. The flat cable interconnect has the same length (40mm) everywhere. Still, there are some FPGA internal delay skews, to be compensated for an optimum trigger performance. Very likely there is also some delay skew related the PMT and the connected AFE plus discriminator chip. Like for the PPS calibration, in system tunable input delay stages are implemented in firmware. The following steps have to be undertaken (DTB register access):

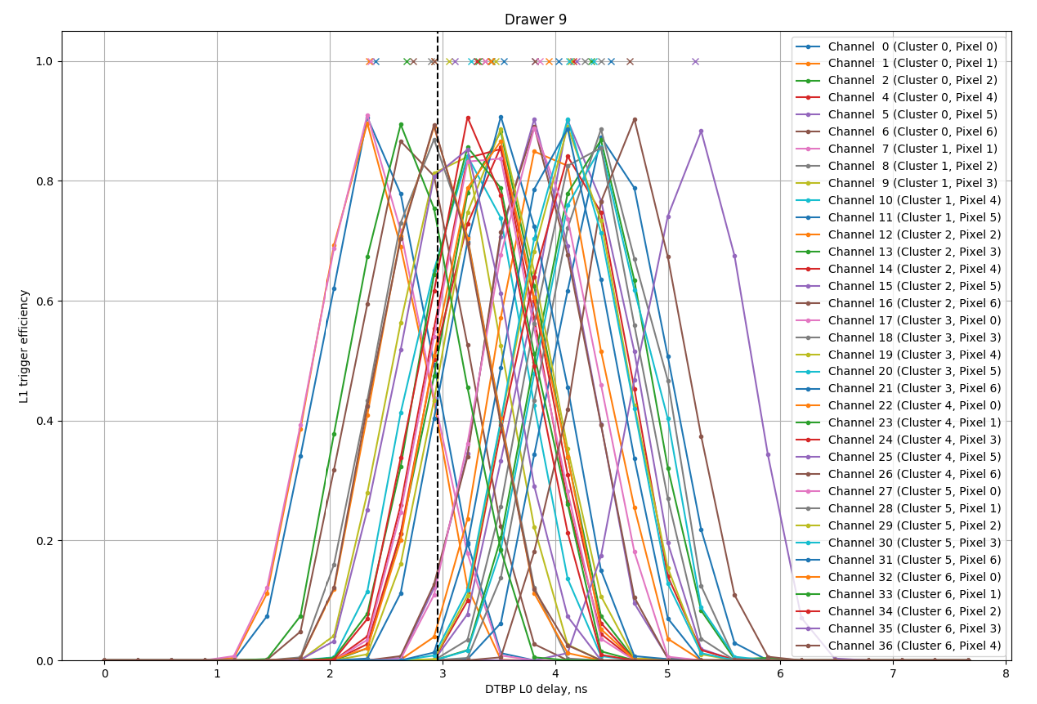
1. Set the trigger algorithm to AND\_2\_of\_37 (ctrl-reg.) to get a trigger, if the central pixel AND one of the selected surrounding are seeing light at the same time.
2. Set the trigger window to 1ns
3. Set the trigger mask, to select the pixel to be calibrated, 1 of 36
4. Use an uniform laser source
5. Adjust the L0 delay of the selected pixel for a **max. trigger rate**
6. Go to step 3. and repeat the measurement, until all 36 pixel got delay tuned
7. Finally store the gained values, to be loaded after the next camera power cycle

The diagrams below, by Patrick Sizun, show the tuning of two pixels in steps of 37ps. Note, for the 1ns trigger window, a 100 % trigger efficiency is not possible, due to the asynchronous sampling of the L0 signals with 1GSPS



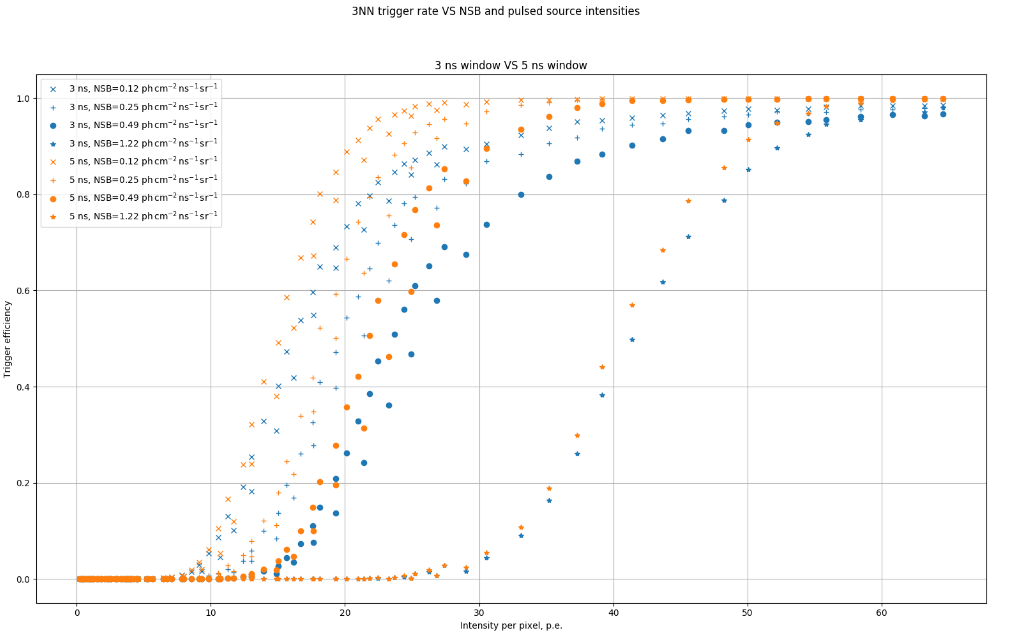
## L0 Delay Adjustment for a 37 Pixel Region

See below, results of a complete L0 delay adjustment, comprising 37 pixels. Courtesy Patrick Sizun



# 3NN Trigger Efficiency vs. Trigger Window

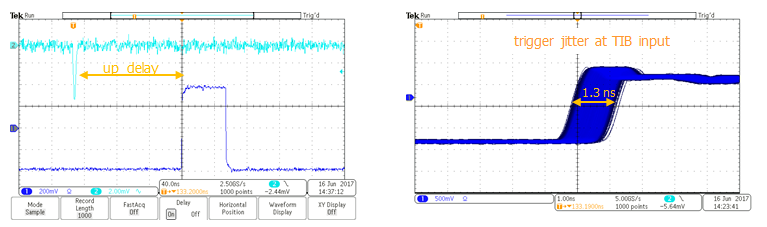
Shown below is the 3NN trigger rate with various NSB values, gained at the test setup at Saclay. Courtesy Patrick Sizun



# Trigger Up and Down Delay Measurement

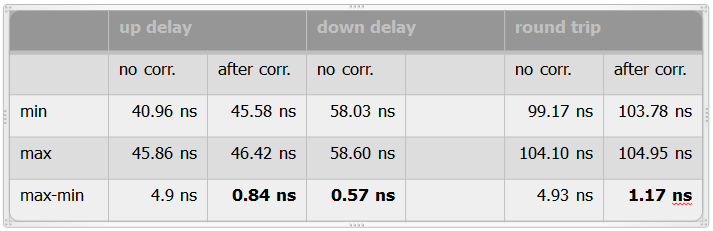
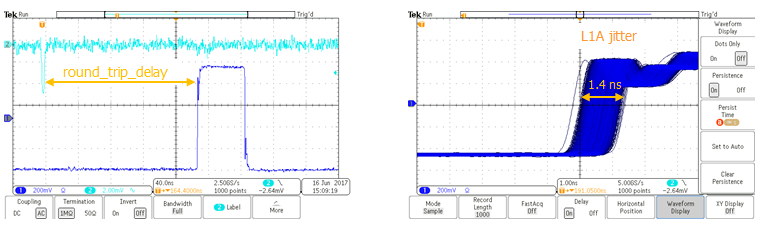
## Upgoing trigger

90 channels of the DESY test setup have been used. The L1 (trigger up) channel to channel skew is mainly caused by the L2 FPGA design, the 270 input trigger-OR. The uncorrected up delay max. skew of 4.9 ns is within the max. programmable (at L2CB) delay range of 0 .. 6.6ns.



## Roundtrip Delay Measurement

The round trip delay is measured by back looping the L2 trigger. A TIB was not available. The roundtrip delay is about 190ns. The down delay skew is very small. For all uncorrected and corrected delay values, see the table below. Additionally, the L1A trigger, arriving at the DTB can be adjusted in steps of 37ps.

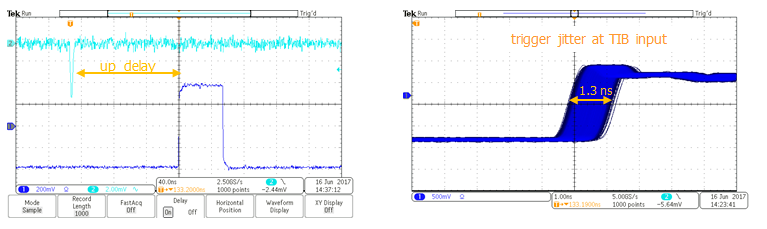


## Trigger Jitter at TIB Input

The test setup:

* L0\_TB + L0-mezzanine as test setup with 3 PMT-like signals of -5mV pk, 3NN trigger
* Scope with delayed triggering on one analog channel
* used the scope display in infinite persistance mode

An absolute (not RMS) jitter of 1.3ns have been observed. To be considered, the L0 signal is sampled at 1GSPS within the DTB FPGA => jitter must be >= 1ns.



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