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| **Digital Trigger Backplane User Manual** |

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| **List of Abbreviations** | | | |
| ATBP | Analog Trigger Backplane | RW | Read / Write |
| DTB | Digital Trigger Backplane | RO | Read Only |
| FEB | Frontend Board | RWC | Read / Write Clear |
| SPI | Serial Peripheral Interface | 76h | 76 hexadecimal |

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| **History** | | |
| Version | Date | Observation |
| 1 | 10/10/2016 | Draft |
| 1a | 06/11/2016 | Draft, corrected |
| 1b | 08/11/2016 | see TRIG\_PULS register description |
| 1c | 14/02/2017 | STAT reg. bits changed, L0\_DELAY\_BUSY explanation added |
| 1d | 15/02/2017 | initial L0 delay removed |
| 20 | 03/03/2017 | valid for DTB4 now, trigger 2 of 37 added for L0 delay calibration |
| 21 | 18/09/2017 | L1 scaler added, trigger 1\_of\_37 added, L0\_DEL\_SEL reg. renamed to PIXEL\_SEL reg. |
| 22 | 27/09/2017 | added correct max. L0 delay value of 5ns (87h) |
| 23 | 18/10/2017 | PPS\_ERR\_CT register and new STAT-reg. bit added |
| 24 | 06/11/2017 | see description of the L0\_DEL register, coarse and fine delay introduced |
| 25 | 21/11/2017 | CTRL reg. description corrected (bit\_7) |
| 26 | 20/12/2017 | CTRL reg., new: bit\_5 used as PPS\_ERR\_CT – clear now  new register added: TRIG\_MASK\_0 ..\_6  register TRIG\_MASK\_C, TRIG\_MASK\_N removed |
| 27 | 20/02/2018 | common firmware / description for locally and externally clocked DTB now |
| 28 | 26/02/2018 | new register introduced, L1\_SC\_WIN, L1 scaler window programmable now, from 10ms to 2.55s |

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| **Distribution** |  |

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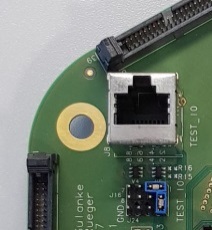
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# Introduction

This document describes the slow control software interface between the NectarCam frontend board and the Digital Trigger Backplane. Up to 128 8-bit registers can be implemented.

valid for firmware Rev. **DTB4\_3nn\_010**

# Local clocking of the DTB

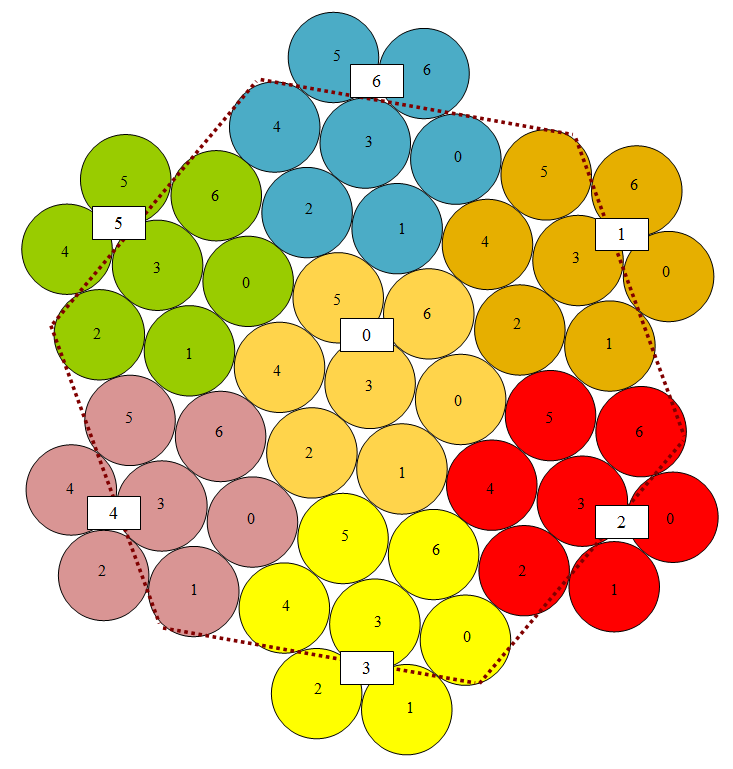
Usually the DTB is externally clocked by the CTDB via it’s Cat.7 cable connection. Especially for the FEB test it is useful to run the DTB in a standalone mode, clocked by the 25 MHz local oscillator Q1. To run the DTB in the locally clocked mode one has to set a jumper on J16\_3-1 and J16\_2-J24\_1 (GND), see snippet.

Compared to the externally clocked mode there are some minor differences:

* 1PPS (signal TIMEPPS) is made from the local clock
* the camera trigger “L1A” is per default the looped backed up going trigger. To disable the loop back bit\_7 of the CTRL register must be set.

# Pixel Numbering Schema

The pixel numbering schema is the one used by the NectarCam team, viewing from outside on the focal plane. The shown cluster numbering is used within the DTB firmware, therefor relevant for the DTB register description.



|  |
| --- |
|  |
| **Figure 1**: Pixel Numbering Schema, focal plane view |

# The Digital Trigger Backplane Slow Control via SPI Bus

|  |
| --- |
|  |
| **Figure 2**: SPI Bus Modes |

The used SPI Bus mode is of the type CPOL = 0, CPHA = 1, see figure 2.

|  |  |
| --- | --- |
| FE\_SPI\_CLK | FE output that provides 16 clock cycles at each slow control access. The frequency of the clock it is not specified. Reasonable values are in the range from 500KHz to 10MHz. The electrical standard for this signal is either LVCMOS\_3.3V or LVCMOS\_2.5V. |
| FE\_SPI\_CE | FE output , low during the slow control access and else high. Electrical standard for this signal is either LVCMOS\_3.3V or LVCMOS\_2.5V. |
| FE\_SPI\_MOSI | Master output / slave input data line. A 16-bit word is transmitted at each slow  control access. The most significant bit is transmitted first. The format of the 16-bit word is shown in table 1. |
| FE\_SPI\_MISO | Master input / slave output data line. A 8-bit word is transmitted at each slow  control access. The most significant bit is transmitted first. In a read access, this line provides the information of the addressed register . |

|  |  |
| --- | --- |
| Bit range | Usage |
| 15 | RD = ‘0’, WR = ‘1’ |
| 14-8 | Address\_7..0, register address |
| 7-0 | Data\_7..0, data byte |

**Table 1**: Slow control 16 bit data field, Bit-15 (MSB) is sent first

|  |  |
| --- | --- |
|  | FE\_SPI\_CE |
| FE\_SPI\_CLK |
| FE\_SPI\_MOSI |
| FE\_SPI\_MISO |
| **Figure 3**: FEB signals, writing data 76h to address 09h at a SPI clock frequency of 12,5 MHz | |

|  |  |
| --- | --- |
|  | FE\_SPI\_CE |
| FE\_SPI\_CLK |
| FE\_SPI\_MOSI |
| FE\_SPI\_MISO |
| **Figure 4**: FEB signals, reading data 76h from address 09h at a SPI clock frequency of 12,5 MHz | |

# *1PPS / L1A delay calibration (presently NOT IMPLEMENTED !)*

*Connect the RJ45 connector to J8 (“TEST\_IO”) and the white/brown twisted pair either to J9 (“+TIMEPPS-“) or J10 (“+L1A”) of the backplane to be calibrated. Connect the black/brown twisted pair to either to J9 (“+TIMEPPS-“) or J10 (“+L1A”) of the central backplane. Press either SW1 (“1PPS calibration”) or SW2 (“L1A calibration”). A green light (V3) means, the calibration is done, a red light signalizes a failing calibration procedure. For confirmation press the unused switch.*

*If the calibration was successful the appropriate delay register contains the gained delay value and can get read out by software.*

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| DTB4 signal | RJ45-pin | color | pair | connect to |
| TEST\_IO2\_P | 4 | black | 1 | “+” of central backplane |
| TEST\_IO2\_N | 5 | brown | “-” of central backplane |
| TEST\_IO3\_P | 8 | white | 2 | “+” of backplane to be calibrated |
| TEST\_IO3\_N | 7 | brown | “-” of backplane to be calibrated |

**Figure 5**: calibration cable

# Register Address Map

|  |  |  |  |
| --- | --- | --- | --- |
| **dec.**  **addr.** | **hex addr.** | **Name** | **Usage** |
| 0 | 00 | CTRL | Control register |
| 1 | 01 | STAT | Status register |
| 2 | 02 | L1\_SC\_WIN | L1 scaler window |
| 3 | 03 | *not used* | *reserved, was TRIG\_MASK\_N before* |
| 4 | 04 | TRIG\_PULS | pulse width for up going (to CTDB) trigger pulse |
| 5 | 05 | TRIG\_DTIM | trigger dead time |
| 6 | 06 | TRIG\_WIN | trigger window using the leading L0-edges |
| 7 | 07 | PPS\_DEL | 1PPS input delay fine tuning in steps of 37 ps |
| 8 | 08 | L1A\_DEL | L1A trigger (L2) input delay fine tuning in steps of 37 ps |
| 9 | 09 | PIXEL\_SEL | Pixel select register |
| 10 | 0A | L0\_ DEL | L0 coarse & fine delay for the pixel selected in 1ns / 37 ps steps |
| *11* | *0B* | *L0\_DEL\_OFFS* | *reserved, will be implemented if required* |
| 12 | 0C | L1\_SCALER\_L | L1 scaler in Hz, when overflow it stays at 0xFFFFh |
| 13 | 0D | L1\_SCALER\_H |
| 14 | 0E | PPS\_ERR\_CT | 1PPS error counter |
| 15 | 0F | PPS\_DEL\_CAL | 1PPS delay value after calibration |
| 16 | 10 | TRIG\_MASK\_0 | trigger mask for the center cluster |
| 17 | 11 | TRIG\_MASK\_1 | trigger mask for neighbor cluster #1 |
| 18 | 12 | TRIG\_MASK\_2 | trigger mask for neighbor cluster #2 |
| 19 | 13 | TRIG\_MASK\_3 | trigger mask for neighbor cluster #3 |
| 20 | 14 | TRIG\_MASK\_4 | trigger mask for neighbor cluster #4 |
| 21 | 15 | TRIG\_MASK\_5 | trigger mask for neighbor cluster #5 |
| 22 | 16 | TRIG\_MASK\_6 | trigger mask for neighbor cluster #6 |
| .. |  |  | not used |
| 125 | 7D |  |
| 126 | 7E | FW\_REVL | Firmware Revision, bits 7..0 |
| 127 | 7F | FW\_REVH | Firmware Revision, bits 15..8 |

## Register Access

It is recommended to do the 1PPS delay adjustment (register PPS\_DEL @ address 07) as a very first step, because it affects the FPGA internal clocks (PLL outputs).

## Register Description

|  |  |
| --- | --- |
| **attribute** | **explanation** |
| RW | Read / Write |
| RO | Read Only |
| RWC | Read / Write Clear (writing a ‘1’ clears the bit) |

**CTRL** @ address 00h, 8 bit RW, power\_on\_value = 0 (00h)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 3..0 | RW | Trigger type select, 0 = 3NN, 1 = 1\_of \_7, 2 = 2\_of\_37, 4 = 1\_of\_37 |
| 4 | RW | LED\_ENABLE, ‘0’ switches off all LEDs |
| 5 | RW | ‘1’ clears the 1PPS-error counter, see reg. PPS\_ERR\_CT |
| 6 | RW | reserved |
| 7 | RW | in local clock mode ‘1’ disables the loop back of the up going trigger to generate L1A |

Use bits 0..3 to choose the trigger algorithm. After power on the 3NN trigger is functional immediately. The trigger window size is about 3ns. It can be changed by accessing the TRIG\_WIN register.

The **trigger 3NN** generates a trigger, if within the 37 pixel area do exist 3 connected pixel.

The **trigger 1\_of\_7** generates a trigger, if one of the central cluster pixel fires.

The **trigger 2\_of\_37** can be used for L0 delay calibration. First the delay of the central pixel (reg. PIXEL\_SEL = 03h) should be set to 7Bh , which corresponds to 4ns delay. Then, one of the surrounding 36 pixel can be selected by using the PIXEL\_SEL register. By varying the L0 delay value (L0\_DEL reg.), e.g. from 00h up to FBh and analyzing the trigger rate one can find the optimum delay value for the chosen pixel. This can be done for each pixel. It might be useful to adjust the trigger window size to 1 ns before.

The **trigger 1\_of\_37** can be used to check, if any of the 37 L0 signals is available. The PIXEL\_SEL register must be used to select the pixel to be checked.

**STAT** @ address 01h, 8 bit RO, RWC

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 0 | RO | PPS\_DELAY\_BUSY |
| 1 | RO | L1A\_DELAY\_BUSY |
| 2 | RO | L0\_DELAY\_BUSY |
| 3 | RO | PPS\_DELAY\_CAL\_BUSY |
| 4 | RO | PPS\_ERROR |
| 7..4 | ‘0’ | Reserved, read value is ‘0’ |

The L0\_DELAY\_BUSY reflects the delay status for the pixel, selected by the PIXEL\_SEL register. The successful delay adjustment requires the availability of the selected signal. If the L0\_DELAY\_BUSY stays on, it means there was no L0 pulse to be delayed so far. Possible reasons: L0-threshold to high, broken wire, ... . If a L0 delay value is written while the L0\_DELAY\_BUSY is on, the delay adjustment restarts with the latest value.

The L0\_DELAY\_BUSY is inactive, if one (accidently) tries to adjust the L0 delay for none existing pixels, e.g. when the cluster has no neighbor (outer cluster ring).

PPS\_ERROR means, the register PPS\_ERR\_CT is not equal to zero.

**L1\_SC\_WIN** @ address 02h, 8 bit RW, power\_on\_value = 64h (1000 ms)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 7..0 | RW | L1 scaler window size in multiples of 10 ms, writing 00h results in used / read back value of 01h, range is 10ms to 2.55 s |

**TRIG\_PULS** @ address 04h, 4 bit RW, 4 bit RO, power\_on\_value = 5 (40 ns)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 3..0 | RW | up going (to CTDB) trigger signal, when 0 no pulse shaping of trigger signal !!! when 1..15, trigger pulse length in multiples of 8 ns |
| 7..4 | RO | ‘0’ |

Only for test purposes, programmable width of the up going trigger pulse.

**TRIG\_DTIM**  @ address 05h, 8 bit RW, power\_on\_value = 12 (0Ch)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 7..0 | RW | trigger dead time in multiples of 8 ns |

Trigger dead time in multiples of 8 ns (DTB system clock), default is 96ns.

**TRIG\_WIN** @ address 06h, 3 bit RW, 5 bit RO, power\_on\_value = 2 (02h)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 2..0 | RW | when 0 no pulse shaping of the L0 signals !!! when 1..7, pulse length of the shaped L0 signal, being used for the trigger. The trigger window = 2\*x-1 ns |
| 7..3 | RO | ‘0’ |

Defines a trigger window for the leading edges of the L0 signals. This is achieved by pulse shaping the L0 (TOT) signal before they are entering the trigger fabric. Use a zero value for no pulse shaping.

**PPS\_DEL** @ address 07h, 8 bit RW, power\_on\_value = 0 (00h)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 7..0 | RW | 1PPS input delay in multiples of 37 ps, max. range=5ns (87h) |

Do the 1PPS delay adjustment as the **very first step**. It affects the DTB systems clock PLL.

**L1A\_DEL** @ address 08h, 8 bit RW, power\_on\_value = 0 (00h)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 7..0 | RW | L1A input delay in multiples of 37 ps, max. range=5ns (87h) |

**PIXEL\_SEL** @ address 09h, 3 bit RW, power\_on\_value = 0 (00h)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 2..0 | RW | 0..6,to select one of the pixel\_0..\_6 |
| 3 | RO | ‘0’ |
| 6..4 | RW | 0..6,to select one of the cluster\_0 .. \_6 |
| 7 | RO | ‘0’ |

Before adjusting the L0 delay, the appropriate pixel has to be selected, according to figure 1.

Also needed for the 1\_of\_37 trigger option

**L0 \_DEL** @ address 0Ah, 5 bit RW, power\_on\_value = 0 (00h)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 4..0 | RW | L0 input fine delay in multiples of 37 ps, pixel selected by reg. PIXEL\_SEL , max. range=1ns (1Bh), additive to the coarse delay |
| 7..5 | RW | L0 input coarse delay in multiples of 1ns, pixel selected by reg. PIXEL\_SEL , max. range = 7ns |

Adjust the L0 delay for any of the 37 pixel, entering the trigger fabric. Use the PIXEL\_SEL register first. Concerning bits 4..0 (fine delay), the L0\_DELAY\_BUSY (STAT-reg. bit\_2) must be checked for readiness. Note that the delay procedures for a value of n (1..31) needs about 2..64 L0-pulses to get ready (L0\_DELAY\_BUSY = ‘0’). To get 1ns the useful max. value is 1Bh. Higher values results in some additional delay.

For bits 7..5, the coarse delay, the L0\_DELAY\_BUSY polling is **not necessary** ! It is functional immediately after the L0\_DEL register write operation.

The delay setting is **identical for all clusters**. An extra offset for the central cluster is **not needed** anymore.

*L0 \_DEL \_OFFS @ address 0Bh, 3 bit RW, power\_on\_value = 0 (00h)*

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 2..0 | RW | L0 input coarse delay offset in multiples of 37 ps, pixel selected by reg. PIXEL\_SEL , max. range=7ns |
| 7..3 | RO | ‘0’ |

L0 delay offset register, reserved, will be implemented, if required. This register can be used for rough equalizing of the L0 delay of all 37 pixels, just once after power on. This results in an equal delay range of +/-4 ns for each pixel, using the L0\_DEL register.

**L1\_SCALER\_L** @ address 0Ch, 8 bit RO, power\_on\_value = 0 (00h)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 7..0 | RO | binary frequency in Hz, lower 8 bit |

**L1\_SCALER\_H** @ address 0Dh, 8 bit RO, power\_on\_value = 0 (00h)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 7..0 | RO | binary frequency in Hz, upper 8 bit |

**PPS\_ERR\_CT** @ address 0Eh, 8 bit RO, power\_on\_value = 0 (00h)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 7..0 | RO | amount of consecutive 1PPS mismatches with respect to the DTB system clock, when overflow it stays at FFh |

Presently, the 10MHz provided by the TIB are converted to 50MHz at the L2 crate and distributed to the DTBs, to be used as common system clock. Note, that the 1PPS delivered by the TIB must be synchronous to the 10MHz !

The counter increments, if the amount of DTB system clock (50 MHz) cycles between consecutive 1PPS signals is not exactly 50 Mio. When overflowing it stays at FFh.

Use CTRL-reg. bit\_5 to clear the PPS\_ERR\_CT.

**PPS\_DEL\_CAL** @ address 0Fh, 8 bit RO, power\_on\_value = 0 (00h)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 7..0 | RO | 1PPS delay value after calibration |

Trigger masking takes place directly at the FPGA inputs. Writing a ‘0’ to the appropriate bit position of the trigger mask register enforces a zero level for the incoming L0 signal. When writing FFh, the read back value corresponds to the pixel (numbers), which can get masked. The trigger mask applies for all trigger modes.

**TRIG\_MSK\_0** @ address 10h, 7 bit RW, 1 bit RO, power\_on\_value = 127 (7Fh)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 6..0 | RW | trigger mask for the central cluster, write ‘0’ to disable the selected pixel |
| 7 | RO | ‘0’ |

**TRIG\_MSK\_1** @ address 11h, 5 bit RW, 3 bit RO, power\_on\_value = 62 (3Eh)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 0 | RO | ‘0’ |
| 5..1 | RW | trigger mask for cluster #1, pixel #5..1 |
| 7..6 | RO | ‘0’ |

**TRIG\_MSK\_2** @ address 12h, 5 bit RW, 3 bit RO, power\_on\_value = 124 (7Ch)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 1..0 | RO | ‘0’ |
| 6..2 | RW | trigger mask for cluster #2, pixel #6..2 |
| 7 | RO | ‘0’ |

**TRIG\_MSK\_3** @ address 13h, 5 bit RW, 3 bit RO, power\_on\_value = 121 (79h)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 0 | RW | trigger mask for cluster #3, pixel #0 |
| 2..1 | RO | ‘0’ |
| 6..3 | RW | trigger mask for cluster #3, pixel #6..3 |
| 7 | RO | ‘0’ |

**TRIG\_MSK\_4** @ address 14h, 5 bit RW, 3 bit RO, power\_on\_value = 107 (6Bh)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 1..0 | RW | trigger mask for cluster #4, pixel #1..0 |
| 2 | RO | ‘0’ |
| 3 | RW | trigger mask for cluster #4, pixel #3 |
| 4 | RO | ‘0’ |
| 6..5 | RW | trigger mask for cluster #4, pixel #6..5 |
| 7 | RO | ‘0’ |

**TRIG\_MSK\_5** @ address 15h, 5 bit RW, 3 bit RO, power\_on\_value = 79 (4Fh)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 3..0 | RW | trigger mask for cluster #5, pixel #3..0 |
| 5..4 | RO | ‘0’ |
| 6 | RW | trigger mask for cluster #5, pixel #6 |
| 7 | RO | ‘0’ |

**TRIG\_MSK\_6** @ address 16h, 5 bit RW, 3 bit RO, power\_on\_value = 127 (h)

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 4..0 | RW | trigger mask for cluster #6, pixel #4..0 |
| 7..5 | RO | ‘0’ |

**FW\_REVL** @ address 7Eh, 8 bit RO

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 7..0 | RO | read back of the firmware revision, bits 7..0 |

**FW\_REVH** @ address 7Fh, 8 bit RO

|  |  |  |
| --- | --- | --- |
| **Bit** | **Attr.** | **Usage** |
| 7..0 | RO | read back of the firmware revision, bits 15..8 |