Ethernet

LED-enable

F2_blown

FEB_24V

F1_blown

1.6 MHz switching by RT

Vout = (R13/R3+1)*0.79V = 3.06V

put text in blue on PCB

1PPS calibration

L1A calibration

put text in blue on PCB

+ TIMEPPS -

+ L1A -

mount next to J11-A4/B4-AB4

Backplane connector 1

Backplane connector 2

+24V GND by power rail

24V by L2

R17 not used

R30 not used

R19, R20 not used

J13_CLK_EXT_P/N used as CLK_PPS_24V_in

mount on bottom side, next to J13

EXT_CLK

+ L1_OUT -

C5, R11, R12 not used

- EXT_CLK +

GCLK - second LVDS input at FPGA simplifies the PPS extraction

J13, J8 : PCB-LIB !! (pin mubers)

R15, R16 not used

J24 parrallel to J16, 2.54mm

TEST_IO

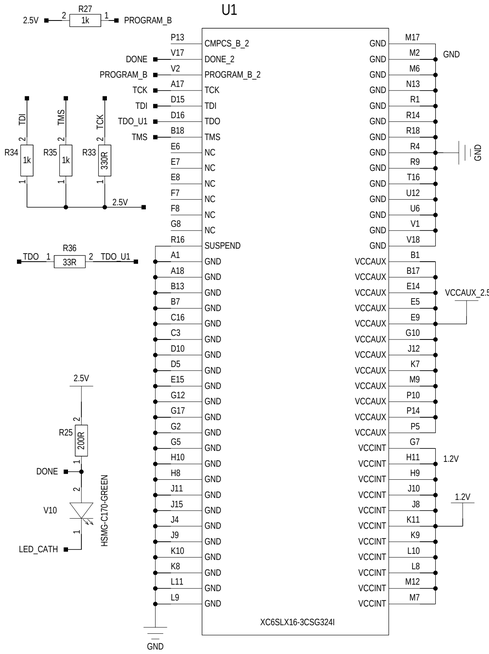
JTAG

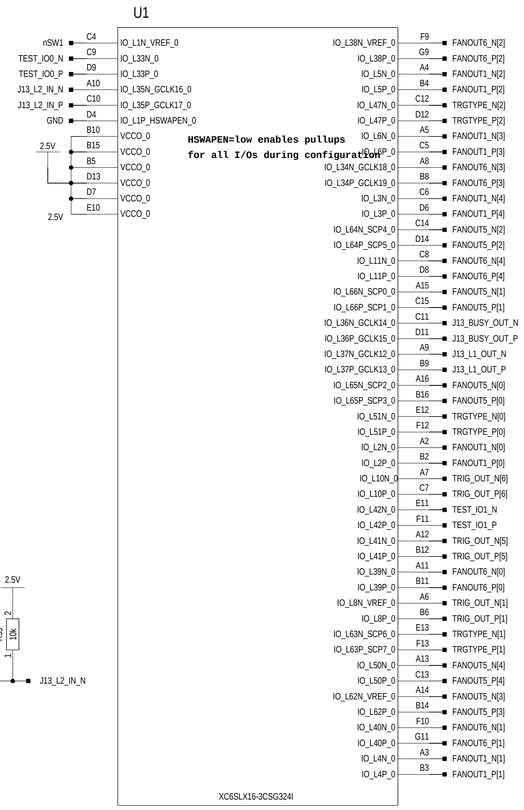
24AA08, addr=1010xB1B0

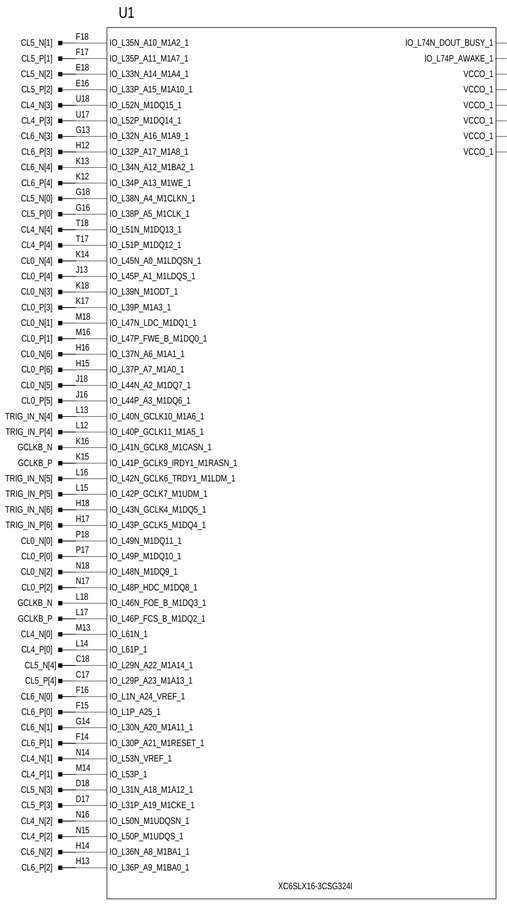
ADDR=GND -> addr=1001001

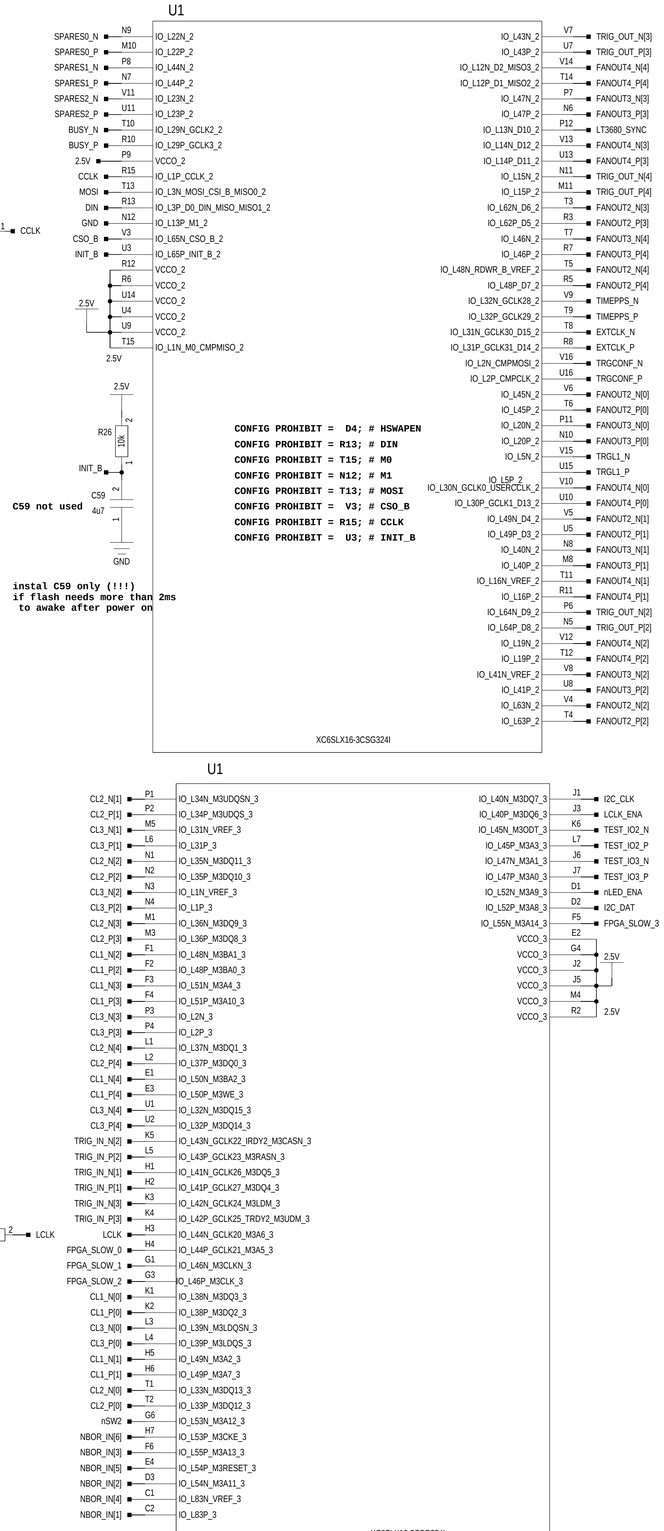
TE CONNECTIVITY 6469025-1

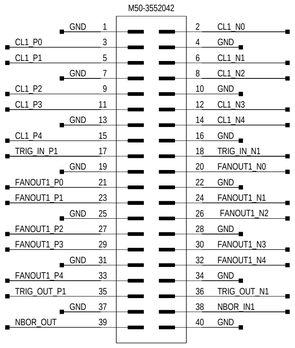
Developer: Karl-Heinz Sulanke	Project: CTA, Digital Trigger Backplane		
	Schematic: DTB4		
Drawn by: Karl-Heinz Sulanke	Sheet:		
Layouter: Carola Rueger	DESY- Platanenallee 6, D-15738 Zeuthen		
Changed of sch:			
Date Changed: 17/02/2018:18:29	PCB No: 9151-02	Rev:	Size: A3
Date of prod. data:	PCB name: DTB4.2	Sheet: 1 of 2	

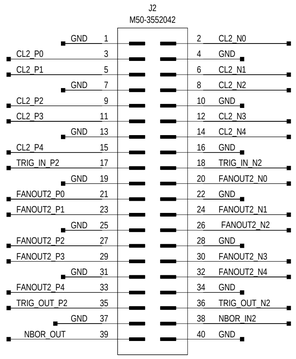


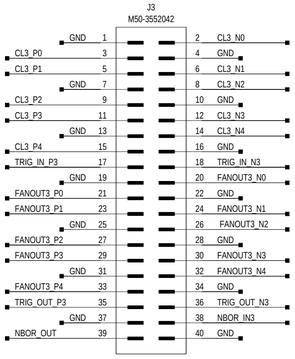


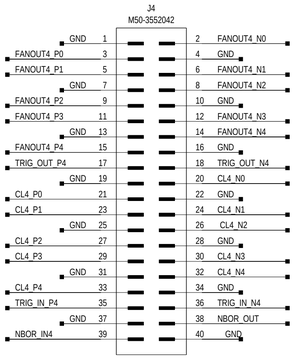


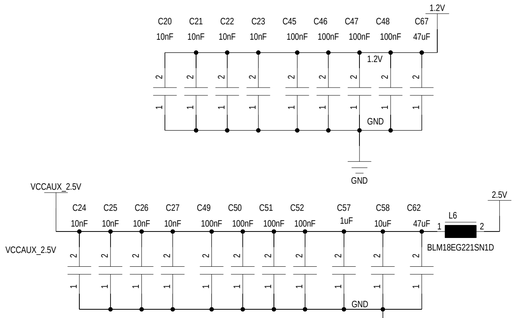


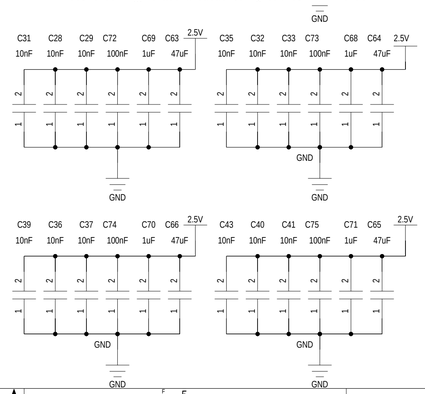












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		Schematic:	DTB4
Drawn by:	Karl-Heinz Sulanke	Sheet:	
Layouter:	Carola Rueger	DESY-	Platanenallee 6 D-15738 Zeuthen
Changed of sch:			
Date Changed:	04/01/2018:10:12	PCB No: 9151-02	Rev: / Size: A3
Date of prod. data:		PCB name: DTB4.2	Sheet: 2 of 2