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| **Digital Trigger Backplane, Firmware** |

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| **Author** | *Laboratory* |  | **Approved by** | *Laboratory* |
| **Karl-Heinz Sulanke DESY** |  |   |
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| **List of Abbreviations** |
| ATBP | Analog Trigger Backplane | PLL | Phase Locked Loop |
| DTB | Digital Trigger Backplane |  |  |
| FEB | Frontend Board |  |  |
| SPI | Serial Peripheral Interface |  |  |
| FPGA | Field Programmable Gate Array |  |  |
| TIB | Trigger Interface Board |  |  |
| CTDB | Clock & Trigger Distribution Board |  |  |
| 1PPS | 1 Pulse Per Second |  |  |
| TOT | Time Over Threshold |  |  |

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| **History** |
| Version | Date | Observation |
| 01 | 18/05/2020 | Draft |
| 02 | 18/10/2020 | final |
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| **Distribution** |  |

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# Introduction

This document describes the basic functionality of the DTB’s firmware, valid for firmware Rev. **DTB4\_3nn\_015.**

# FPGA

The FPGA of the type Xilinx XC6SLX16-3CSG324I is the heart of the Digital Trigger Backplane. After power on, it gets loaded from a serial Flash (AT45DB081E-SSHN). The latter can be updated via a JTAG connection, controlled by the FEB or external Xilinx programming hardware (e.g. Platform Cable USB II).

# Firmware Description

## Clock and FEB-1PPS Generation

The FPGA receives a 50MHz clock, provided by one of the CTDBs, being plugged to the L2-Crate. Every second exactly one clock pulse is modulated by the 1PPS signal. The modulation is achieved by changing the clocks duty cycle from 50/50 to 25/75. The duty cycle change is not affecting the FPGA internal PLL, being synchronized by the leading edge of the clock. A phase shifted clock output of the PLL is used to recover the 1PPS signal, needed by the FEB.

The trigger logic is driven by a 125MHz clock (PLL output).

## Register Block

24 8-Bit register allow various control and calibration procedures. The address range is 7bit. If needed, up to 104 registers can be added. These register can be accessed via the FEB using the SPI bus. Implemented is a SPI slave interface. For details, see the DTB\_user\_manual\_xx.pdf .

## L0 Delay Tuning

The trigger logic processes the L0 (TOT) signals of 37 pixels. An accurate delay tuning for each of the pixels is required. The presently used Firmware (Rev. 015) allows to program a coarse delay between 0 to 7ns in steps of 1ns and a fine delay of 0 to 1ns in steps of 37ps.

## Trigger Logic

The trigger factory receives the delay-tuned, possible masked and according to the trigger window size extended L0 signals. Presently, the CTRL register allows the selection of one of four trigger algorithms:

The **trigger 3NN** generates a trigger, if 3 connected pixels do exist within the 37 pixel area.

The **trigger 1\_of\_7** generates a trigger, if one of the central cluster pixel fires, useful for FEB-tests.

The **trigger 2\_of\_37** can be used for L0 delay calibration. First the delay of the central pixel is set to a medium delay of 4ns. Then, one of the surrounding 36 pixels can be selected, using the PIXEL\_SEL register. By varying the L0 delay value and analyzing the trigger rate one can find the optimum delay value for the chosen pixel. This can be done for each pixel. It might be useful to adjust the trigger window size to 1ns before.

The **trigger 1\_of\_37** can be used to check, if any of the 37 L0 signals is available. The PIXEL\_SEL register must be used to select the pixel to be checked.

The trigger logic consists out of 8 identical blocks, each processing a time slice of 1ns. The synchronous trigger output signal, generated by an OSERDES stage has a time resolution of 1ns.

## DTB, Trigger Firmware, Block Diagram


## FPGA Occupancy, Firmware Rev. 015

Copied from the ISE Place and Route Report

Device Utilization Summary:

Slice Logic Utilization:

 Number of Slice Registers: 4,272 out of 18,224 23%

 Number used as Flip Flops: 4,272

 Number used as Latches: 0

 Number used as Latch-thrus: 0

 Number used as AND/OR logics: 0

 Number of Slice LUTs: 8,822 out of 9,112 96%

 Number used as logic: 8,604 out of 9,112 94%

 Number using O6 output only: 7,009

 Number using O5 output only: 181

 Number using O5 and O6: 1,414

 Number used as ROM: 0

 Number used as Memory: 84 out of 2,176 3%

 Number used as Dual Port RAM: 0

 Number used as Single Port RAM: 28

 Number using O6 output only: 0

 Number using O5 output only: 0

 Number using O5 and O6: 28

 Number used as Shift Register: 56

 Number using O6 output only: 56

 Number using O5 output only: 0

 Number using O5 and O6: 0

 Number used exclusively as route-thrus: 134

 Number with same-slice register load: 124

 Number with same-slice carry load: 10

 Number with other load: 0

Slice Logic Distribution:

 Number of occupied Slices: 2,278 out of 2,278 100%

 Number of MUXCYs used: 256 out of 4,556 5%

 Number of LUT Flip Flop pairs used: 8,873

 Number with an unused Flip Flop: 5,027 out of 8,873 56%

 Number with an unused LUT: 51 out of 8,873 1%

 Number of fully used LUT-FF pairs: 3,795 out of 8,873 42%

 Number of slice register sites lost

 to control set restrictions: 0 out of 18,224 0%

## Timing Constraints

#Copied from the file dtb4\_3nn\_015.ucf

#

# setting the pass-through delay for the 7 pixel-fanout of the central cluster

#

PIN CL0\_\* TNM=center\_pixel;

PIN FANOUT\*\_\* TNM=fanout\_pixel;

TIMESPEC TS\_fanout = FROM "center\_pixel" TO "fanout\_pixel" 10.6 ns;

#

# 25MHz local clock, used at the FEB test setup

#

NET "LCLK" TNM\_NET = "lclk";

TIMESPEC "TS\_lclk" = PERIOD "lclk" 40 ns HIGH 50%;

#

# 50MHz global clock, distributed by the L2-crate via CTDB

#

NET "GCLKB\_P" TNM\_NET = "gclkb";

TIMESPEC "TS\_gclk" = PERIOD "gclkb" 20 ns HIGH 50%;