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| **CTDB-L2Crate Interface Definition** |

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| **List of Abbreviations** | | | |
| CTDB | Clock & Trigger Distribution Board |  |  |
| DTB | Digital Trigger Backplane |  |  |
| FEB | Frontend Board |  |  |
| L2BP | L2 Crate Backplane |  |  |
| LVDS | Low Voltage Digital Signalling |  |  |
| MISO | master in slave out |  |  |
| MOSI | master out slave in |  |  |
| PPS | Pulse Per Second |  |  |
| SPI | Serial Peripheral Interface |  |  |

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| **History** | | |
| Version | Date | Observation |
| 01 | 21/10/2020 | Draft |
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| **Distribution** |  |

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# Introduction

See the block diagram below. The CTDB has to fulfil the following tasks:

* FEB (+DTB)-power switching, including electronic fuse and current monitoring
* Clock and PPS distribution to fifteen FEBs via the DTB
* Collecting the trigger signals (L1\_xxx) of fifteen 7-pixel clusters (controlled by the FEB) and propagating them to the L2CB
* Reception of the camera trigger (L1A) and propagating it (fanout) to the fifteen FEBs
* Collecting the BUSY signals of fifteen FEBs and propagating the ORed BUSY to the L2CB

This document describes the mechanical and the electrical interface between the CTDB and theL2Crate. The timing of the signal is defined by the timing requirements (B-TEL-1265, B-TEL-1410, etc). The CTDB has been carefully designed, to meet these requirements. E.g. in case of the PCB design, by enforcing the trace length for signal groups, to be equal within +/- 1mm.

Related interfaces, see in the block diagram below the

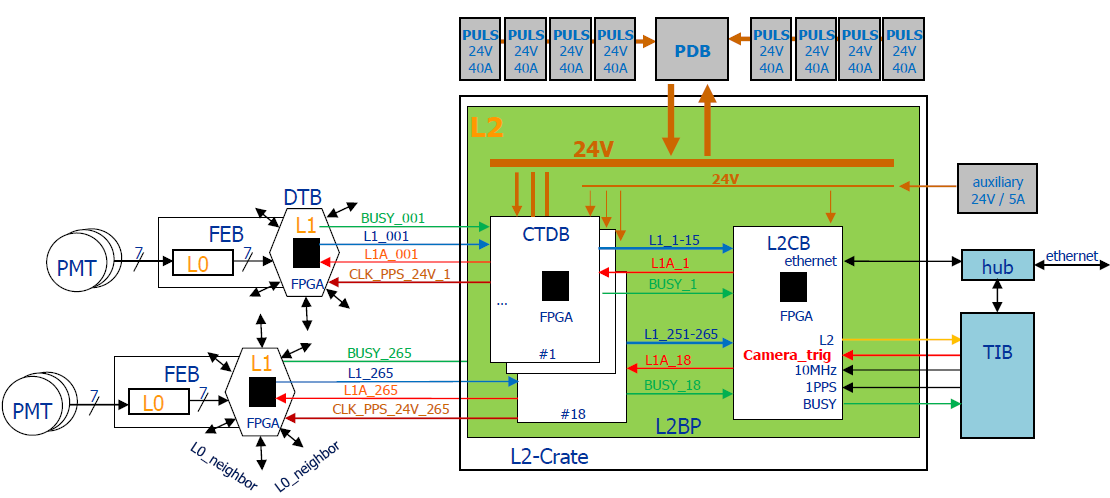


Figure 1 Digital Trigger, Block Diagram

# CTDB Mechanics

The CTDB is a 6U standard size card, 160 x 233.3 mm, arranged in the L2Crate at a grid of 20.32mm.

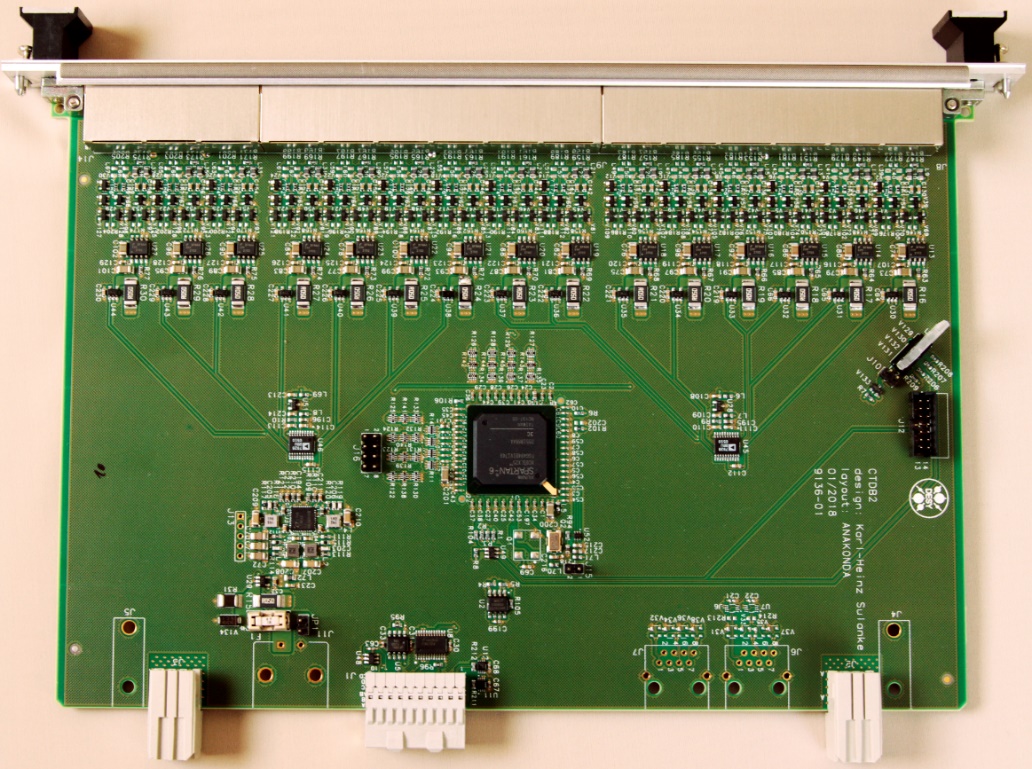


Figure 2 CTDB

## CTDB Front Panel

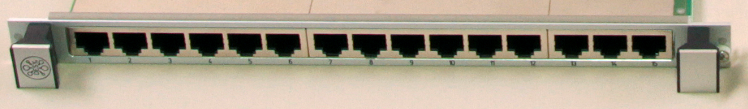
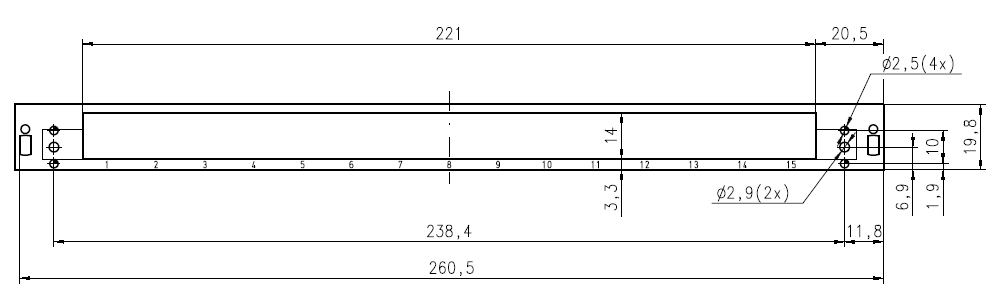
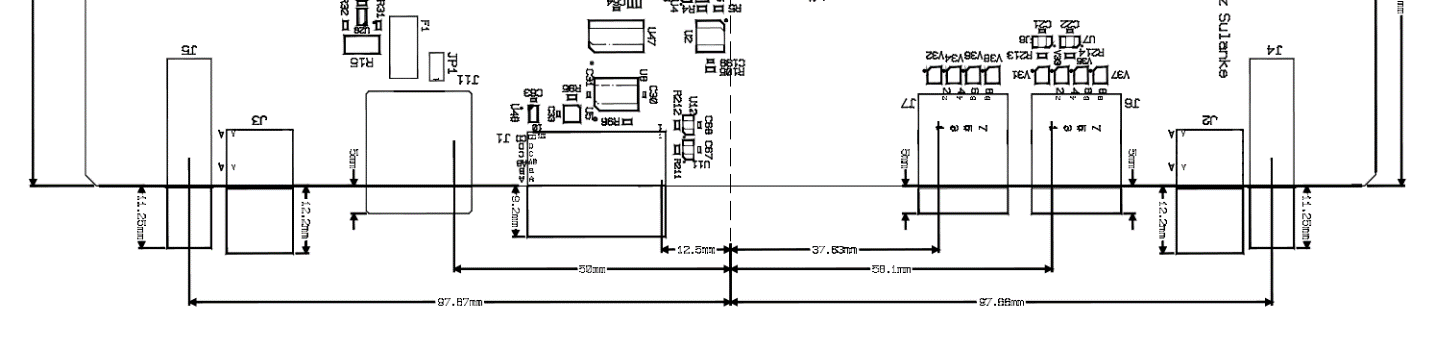


Figure 3 CTDB front panel

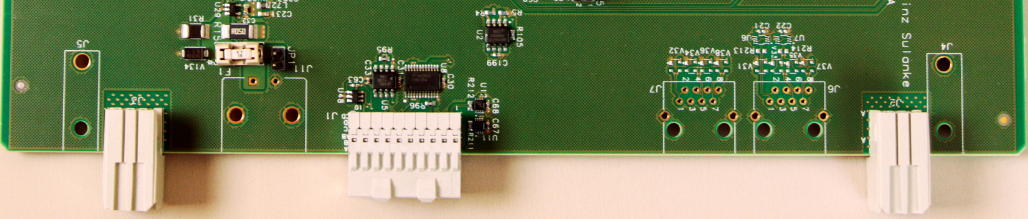
## Connector Arrangement

Two connectors at the back side of the card establishing the L2BP connections. J2 is the 24V power-, J3 is the GND connector. J1 carries the L2BP signals, like trigger, busy, clock and SPI. All other below shown connectors and guide pins are not used.



**J2**

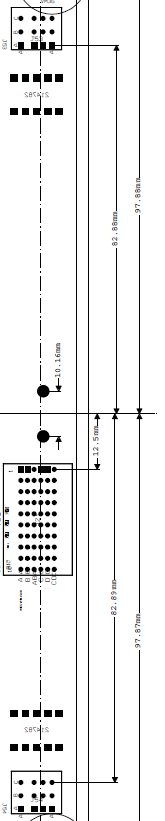
**J1**



**J3**

**CTDB**

Figure 4 CTDB connectors at backplane end



**J117**

**J118**

**J1**



**L2BP**

Figure 5 L2-crate backplane, corresponding CTDB connectors

# Connector Types

Press fit types, current rating of 30A (10A per blade, optional 16A )

|  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- |
| **side** | **connector type** | **manufacturer** | **man.-ID** | **usage** |  |
| CTDB | Z-Pack, right angle | TE Connectivity | 5-5223961-1 | power |  |
| CTDB | Z-Pack, right angle | TE Connectivity | 6469028-1 | signal |  |
| L2BP | Z-Pack, straight | TE Connectivity | 5223955-2 | power |  |
| L2BP | Z-Pack, straight | TE Connectivity | 6469025-1 | signal |  |

Figure 6 L2-crate backplane side, connectors used

# Connectors, Pin Usage

## Power connectors

|  |  |  |  |
| --- | --- | --- | --- |
| **side** | **connector** | **signal** | **schematic** |
| CTDB | J2 | +24V |  |
| CTDB | J3 | GND |  |
| L2BP | J117  J119  … | +24V |  |
| L2BP | J118  J120  … | GND |  |

## Signal Connector J1

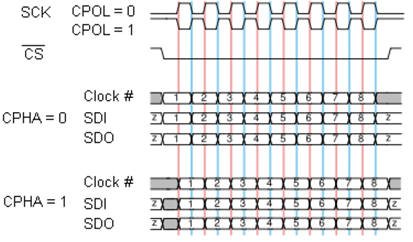
Except BP\_ADDR(0..4), all input signals are driven by the L2CB.

|  |  |  |
| --- | --- | --- |
| **Pin** | **CTDB - Signal name** | **Description** |
| A1 | DTB\_CLK\_P | input, LVDS, clock, to be distributed to the FEB via DTB |
| B1 | DTB\_CLK\_N |
| AB1 | GND |  |
| A2 | DTB\_PPS\_P | input, LVDS, PPS, to be distributed to the FEB via DTB |
| B2 | DTB\_PPS\_P |
| AB2 | GND |  |
| A3 | not connected |  |
| B3 | not connected |
| AB3 | GND |  |
| A4 | L2\_TRIG\_P | input, LVDS, down going trigger (L1A) |
| B4 | L2\_TRIG\_P |
| AB4 | GND |  |
| A5 | SPI\_MOSI\_P | input, LVDS, L2CB-data, SPI bus, |
| B5 | SPI\_MOSI\_N |
| AB5 | GND |  |
| A6 | SPI\_SCLK\_P | input, LVDS, SPI bus clock |
| B6 | SPI\_SCLK\_N |
| AB6 | GND |  |
| A7 | SPI\_MISO\_P | output, LVDS, CTDB-data, SPI bus |
| B7 | SPI\_MISO\_N |
| AB7 | GND |  |
| A8 | SPI\_SYNC\_P | input, LVDS, SPI bus frame signal |
| B8 | SPI\_SYNC\_N |
| AB8 | GND |  |
| A9 | P2V5 | output, +2.5V, generated by CTDBs local DC/DC  output, 2.5V, low-active, can cause an interrupt at the L2CB |
| B9 | BP\_INTn |
| AB9 | GND |  |
| A10 | BP\_P24V | input, +24V by L2Crate auxiliary power supply |
| B10 | BP\_P24V |
| AB10 | not connected |  |

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| --- | --- | --- |
| **Pin** | **Signal** | **Remark** |
| C1 | L1\_TRIG(1) | output, 3.3V with 51ohm serial resistor, L1 trigger signal, driven by CTDBs FPGA |
| D1 | L1\_TRIG(2) |
| CD1 | GND |  |
| C2 | L1\_TRIG(3) |  |
| D2 | L1\_TRIG(4) |
| CD2 | GND |  |
| C3 | L1\_TRIG(5) |  |
| D3 | L1\_TRIG(6) |
| CD3 | GND |  |
| C4 | L1\_TRIG(7) |  |
| D4 | L1\_TRIG(8) |
| CD4 | GND |  |
| C5 | L1\_TRIG(9) |  |
| D5 | L1\_TRIG(10) |
| CD5 | GND |  |
| C6 | L1\_TRIG(11) |  |
| D6 | L1\_TRIG(12) |
| CD6 | GND |  |
| C7 | L1\_TRIG(13) |  |
| D7 | L1\_TRIG(14) |
| CD7 | GND |  |
| C8 | L1\_TRIG(15) | output, driven by CTDBs FPGA, OR from 15 incoming FEB-Busy signals |
| D8 | L1\_BUSY |
| CD8 | GND |  |
| C9 | BP\_ADDR(0) | inputs, at L2BP hard encoded binary slot number, 1..9, 13..21. The CTDB has pullups. At the L2BP there are GND-connections for the ‘0s’. |
| D9 | BP\_ADDR(1) |
| CD9 | not connected |  |
| C10 | BP\_ADDR(2) |  |
| D10 | BP\_ADDR(3) |
| CD10 | BP\_ADDR(4) |  |

# SPI Bus

All slow control is achieved, by using the L2BP-SPI bus, driven by the L2CB.



SPI Bus Modes. The used SPI Bus mode is of the type CPOL = 0, CPHA = 1

|  |  |
| --- | --- |
| **L2 Backplane, SPI Bus signals** | |
| **SPI\_SCLK** | L2CB output that provides 32 clock cycles at each slow control access. The frequency of the clock it is 6.25 MHZ . The electrical standard for this signal is LVDS. Other frequencies are possible. |
| **SPI\_SYNCn** | L2CB output , low during the slow control access and else high. Electrical standard for this signal is LVDS. |
| **SPI\_MOSI** | Master output / slave input data line. A 32-bit word is transmitted at each slow  control access. Electrical standard for this signal is LVDS.  The most significant bit is transmitted first. The format of the 32-bit word is shown in table 1. |
| **SPI\_MISO** | Master input / slave output data line. Electrical standard for this signal is LVDS.  A 16-bit word is transmitted at each slow control access. The most significant bit is transmitted first. Active at a read access, else tristated. This line provides the information of the addressed CTDB register. |

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| **Bit range** | **Usage** |
| 31 | RD = ‘0’, WR = ‘1’ |
| 30..29 | ‘0’, not used |
| 28..24 | slot address 4..0 (1..9, 13..21) |
| 23..16 | CTDB register address 7..0 |
| 15..0 | CTDB register data 15..0 |

Bit-31 (MSB) is sent first

## SPI Bus Timing

Measured SPI bus cycles are illustrated below. The Bus cycle time is about 5.4 us. Higher rates can be achieved by adapting the L2CB firmware accordingly.

|  |  |  |  |
| --- | --- | --- | --- |
| SPI\_SYNC | | write_0x1234_slot2_rg_addr_0x20  Figure 7 Measured, SPI write cycle of 1234h to address 20h of CTDB at slot 2 | |
| SPI\_SCLK | |
| SPI\_MOSI | |
| SPI\_MISO | |
|  | |
|  | | | |
|  | | | |
| SPI\_SYNC | | read_0x1234_slot2_rg_addr_0x20  Figure 8 Measured, SPI read of 1234h from address 20h of CTDB at slot 2 | |
| SPI\_SCLK | |
| SPI\_MOSI | |
| SPI\_MISO | |
|  | |
|  | | | |

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