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| **Digital Trigger Backplane, Firmware** |

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| **List of Abbreviations** | | | |
| L2CB | L2-crate Controller Board | PLL | Phase Locked Loop |
| DTB | Digital Trigger Backplane | L1A | L1 trigger Accepted |
| FEB | Frontend Board |  |  |
| SPI | Serial Peripheral Interface |  |  |
| FPGA | Field Programmable Gate Array |  |  |
| TIB | Trigger Interface Board |  |  |
| CTDB | Clock & Trigger Distribution Board |  |  |
| PPS | Pulse Per Second |  |  |
| L2BP | L2-crate Backplane |  |  |

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| **History** | | |
| Version | Date | Observation |
| 01 | 18/05/2020 | Draft |
| 02 | 18/10/2020 | final |
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| **Distribution** |  |

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# Introduction

This document describes the basic functionality of the CTDB’s firmware, valid for firmware Rev. ctdb2\_001**.**

# FPGA

The FPGA of the type Xilinx XC6SLX25-2FGG484I is the heart of the CTDB. After power on, it gets loaded from a serial Flash (AT45DB081E-SSHN). The latter can be updated via a JTAG connection, using Xilinx programming hardware (e.g. Platform Cable USB II).

# Firmware Description

## Clock and 1PPS Distribution to FEBs

The FPGA receives a 50MHz master clock and PPS, provided by the L2CB via the L2-crates backplane (L2BP).

To generate the 15 DTB clocks, to be distributed, the 50MHz gets modulated with the 1PPS signal, resulting in a changed duty cycle from 50/50 to 25/75 for one clock period. Finally this modulated clock gets fan out to the 15 RJ45 connectors. Programmable output delay stages allow the minimizing of the channel to channel skew.

## L1\_Up Trigger and BUSY\_Up Propagation

The 15 L1 trigger signals and the 15 FEB-BUSY signals, received from the DTBs, are passing programmable output delay stages, before being sent to the L2CB via the L2BP. This way systematic delay differences, caused by the FPGA internal routing, are compensated.

## L1A Trigger Fanout

The camera trigger, delivered by the TIB and passed through the L2CB to the L2BP gets fan out and according to the systematic skew, corrected by delay stages, before passing them to the 15 RJ45 connectors.

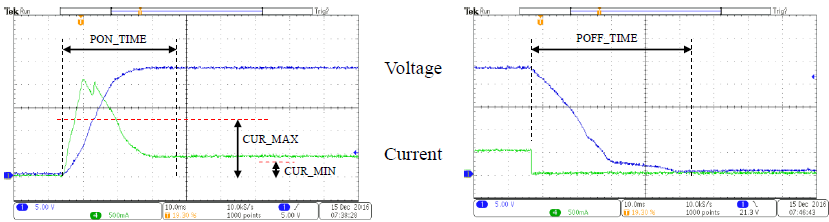
## Register Block

26 16-Bit register are being used for FEB-power on/off control, current monitoring, current limits and debugging. The address range is 8bit, leaves plenty of room for registers to be added. These register access takes place via the, by all CTDBs shared, SPI bus, located on the L2BP. Implemented is a SPI slave interface. The L2CB is the bus master.

## FEB Power on/off Control, Current Monitoring and Firmware Fuse

The15 bits of the power on/off register are being used to switch the 24V for the 15 FEBs. Two eight channel serial (SPI) ADCs are continuously read out, to monitor the FEBs currents. 15 state machines in the background are checking every 44us (period programmable) if the FEB current is within its predefined (register) window. If not, the appropriate channel gets shutdown, the status, to be read out by software, is stored in a status register. Toggling of the appropriated power-on bit clears the failure status.

## Power on/off State Diagram



POWER

OFF

POWERING

ON

POWER ON

POWERING

OFF

POWER

OFF

POWERING ON

24V=ON

Software

power-on

power-on

timer exp.

Over\_cur. or

Under\_cur.

Software

power-off

Software

power-off

POWER ON

24V=ON

POWER FAIL

24V=OFF

POWERING OFF

24V=OFF

power-off

timer exp.

POWER OFF

24V=OFF

## CTDB Firmware, Block Diagram

L1\_up from DTB

L1A to DTB

CLK\_PPS to DTB

PON\_1..15

SEL\_and\_TEST

L1\_up to L2CB

L2 from L2CB

CLK from L2CB

PPS from L2CB

SLOT\_ADR

L2CB\_SPI

ADC\_SPI

delay

delay

fanout

PLL

encoder

delay

fanout

SPI

ctrl

Register

block

Local CLK

PLL

SPI

ctrl

FEB-

CUR

STM

debug

BUSY from DTB

BUSY to L2CB

delay

## FPGA Occupancy, Firmware Rev. 01

Copied from the ISE Place and Route Report

Device Utilization Summary:

Slice Logic Utilization:

Number of Slice Registers: 744 out of 30,064 2%

Number used as Flip Flops: 744

Number used as Latches: 0

Number used as Latch-thrus: 0

Number used as AND/OR logics: 0

Number of Slice LUTs: 1,558 out of 15,032 10%

Number used as logic: 1,539 out of 15,032 10%

Number using O6 output only: 1,099

Number using O5 output only: 43

Number using O5 and O6: 397

Number used as ROM: 0

Number used as Memory: 0 out of 3,664 0%

Number used exclusively as route-thrus: 19

Number with same-slice register load: 15

Number with same-slice carry load: 4

Number with other load: 0

Slice Logic Distribution:

Number of occupied Slices: 552 out of 3,758 14%

Number of MUXCYs used: 332 out of 7,516 4%

Number of LUT Flip Flop pairs used: 1,631

Number with an unused Flip Flop: 922 out of 1,631 56%

Number with an unused LUT: 73 out of 1,631 4%

Number of fully used LUT-FF pairs: 636 out of 1,631 38%

Number of slice register sites lost

to control set restrictions: 0 out of 30,064 0%

## Timing Constraints

#Copied from the file CTDB2\_001.ucf

#

# backplane clock from L2CB

#

NET "bp\_clk" TNM\_NET = "bp\_clk";

TIMESPEC "TS\_bp\_clk" = PERIOD "bp\_clk" 20 ns HIGH 50%;

#

# local clock oscillator

#

NET "LOC\_CLK2" TNM\_NET = "loc\_clk2";

TIMESPEC "TS\_loc\_clk2" = PERIOD "loc\_clk2" 40 ns HIGH 50%;

#

NET "lclk2\_gclk2" TNM\_NET = "lclk2\_gclk2";

TIMESPEC "TS\_lclk2\_gclk2" = PERIOD "lclk2\_gclk2" 10 ns HIGH 50%;

#

#defining L1\_up pass through delays

#

PIN TRIG\_IN\_\* TNM=CTDB\_L1;

PIN L1\_TRG\* TNM=L2CB\_L1;

TIMESPEC TS\_l1\_delay = FROM "CTDB\_L1" TO "L2CB\_L1" 11.6 ns;

#

# defining BUSY\_up pass through delays

#

PIN PPS\_BUSY\_\* TNM=BUSYS\_IN;

PIN BUSY\_OUT TNM=BUSY\_OR\_OUT;

TIMESPEC TS\_busy\_delay = FROM "BUSYS\_IN" TO "BUSY\_OR\_OUT" 14.7 ns;

NET "BUSY\_OUT" MAXSKEW = 0.1 ns;

#