Development of a Fast ADC for TTF

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Motivation

- new injector planned with 110ns bunch spacing (9 MHz)
- Replacement of the COMET board (4 channels, 12bit, 2MSample/s, ADC in Hybrid technique --> expensive) by a board with better parameters for single bunch measurements
- only one system for diagnostics and Low Level RF control in future
- easy connection with DSP board for Low Level RF control

Project team

- Jerzy Andruszkow [a] - ADC Controller
- Piotr Jurkiewicz [a] - Analog Design
- Andrej Kholodnyj - Test programms
- Frank Tonisch - VME Design (co-ordination)

a. Henryk Niewodniczanski Institute of Nuclear Physics, Cracow

Design parameters

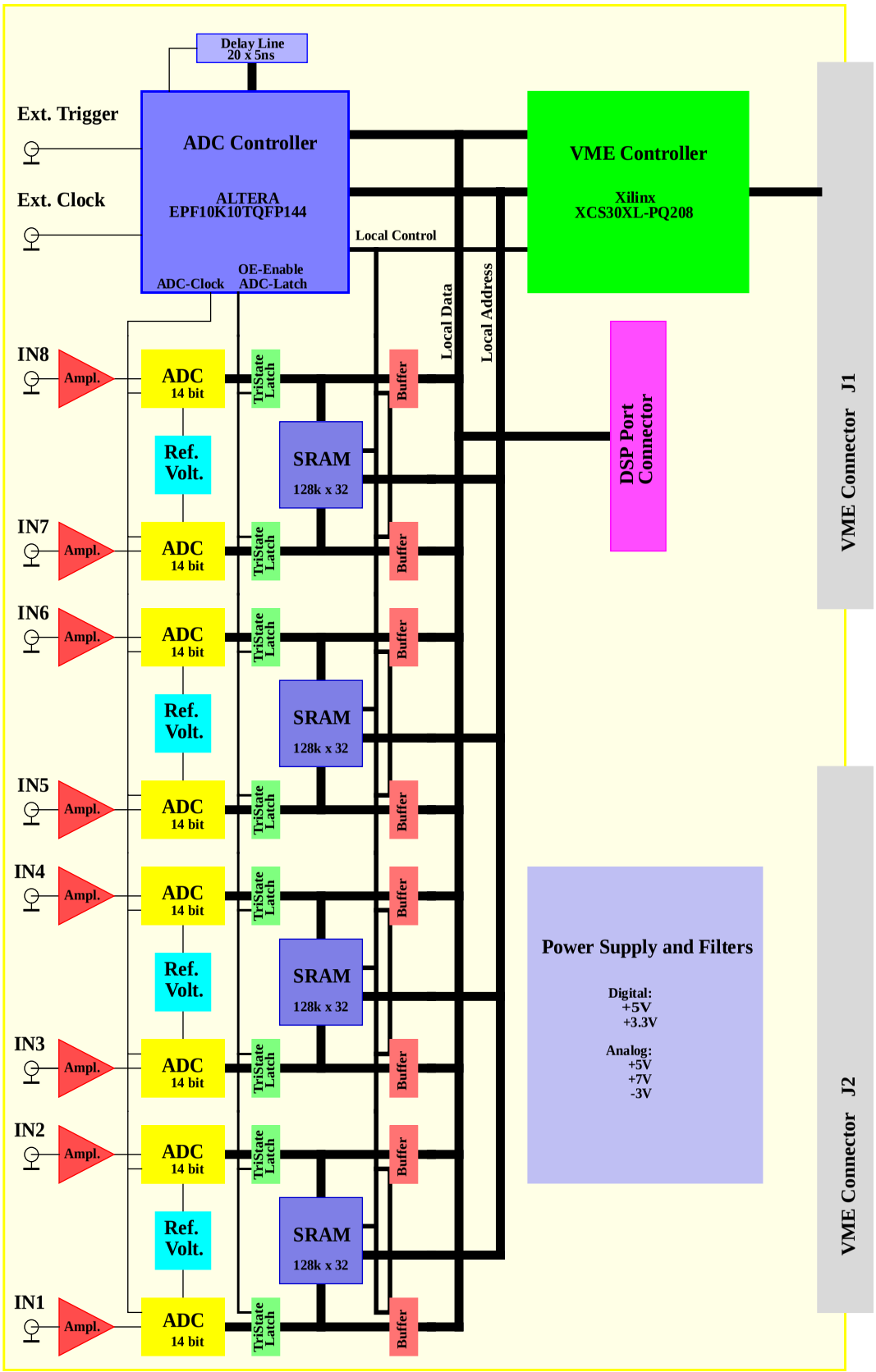
- Resolution: 14 bit
- Sample rate: up to 10 MHz
- variable input range: +/- 1V, +/- 5V
- variable input impedance: 50Ω , High impedance (1kΩ)

Design Parameters

(cont'd)

- Possibility of external and internal triggering
- # of triggers programmable from 1 to 65535
- Possibility of external and internal clocking
- # of samples / trigger programmable from 1 to 65535
- VME Interrupt after conversion complete
- 128k memory / ADC channel

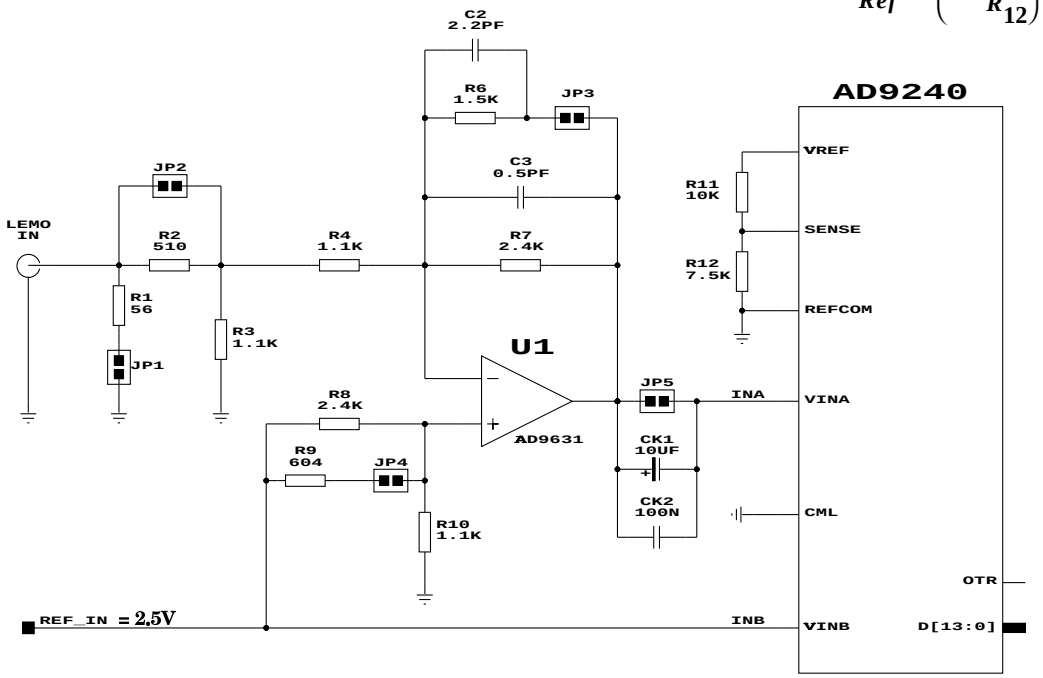
Block diagram

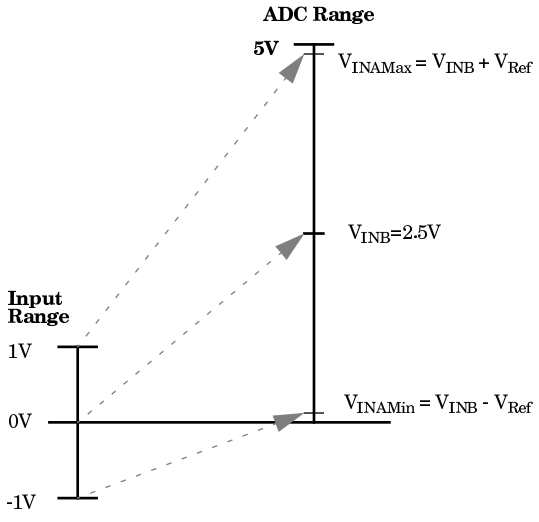


Analog design

schematic diagram

$$V_{Ref} = \left(1 + \frac{R_{11}}{R_{12}}\right) \cdot 1V = 2.333V$$





$$Data = \left(\frac{V_{INA} - V_{INB}}{V_{Ref}} + 1\right) \cdot 2^{13}$$

- AD9240 operates from single power supply
- buffer amplifier adapts selected input range to ADC input range (level shift + gain)

Option		Open	Closed	V_{INA} DC-offset	gain
Input Range:	+/-1V	JP3, JP4	JP2	2.42V	2.18
	+/-5V	JP2	JP3, JP4	2.82V	0.43

- input impedance and coupling mode selectable via jumpers

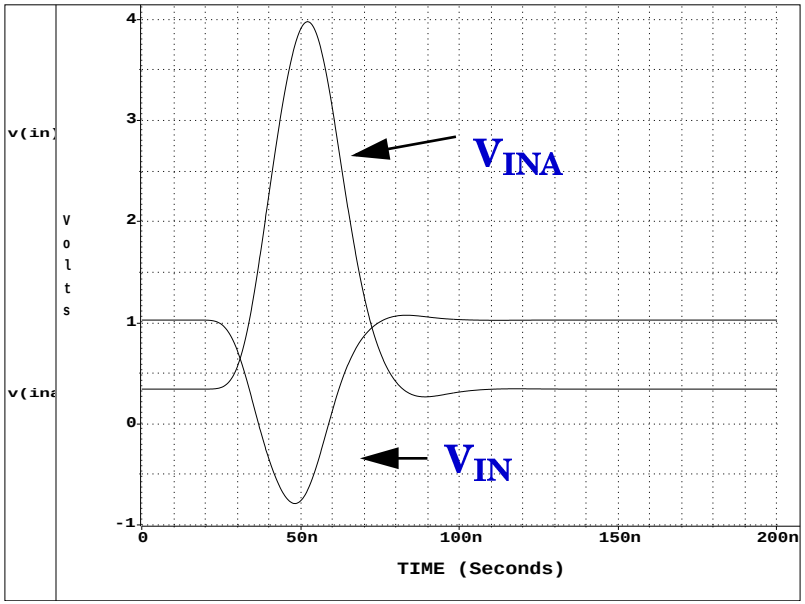
Option		Open	Closed
Input impedance:	50Ω		JP1
	1kΩ	JP1	
Coupling:	DC		JP5
	AC	JP5[(a)]	

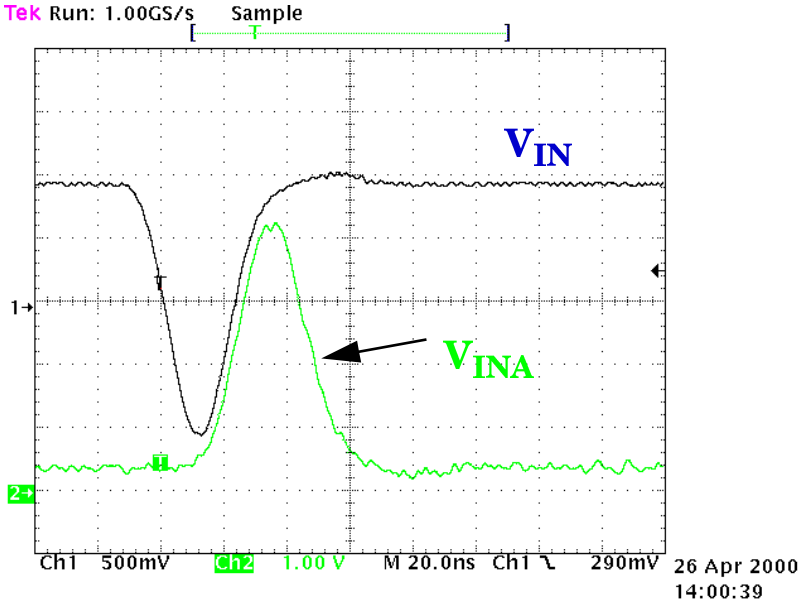
a. V_{INA} DC-Offset = 2.5V

Pulse response

- designed for optimum pulse response (minimum distortion)

HSPICE Simulation





- estimated bandwidth 50 MHz (HSPICE simulation)

ADC Controller

- realized with ALTERA FPGA
  - design completely written in AHDL (ALTERA Hardware Description Language)
- contains all registers controlling the modes of operation
  - ADC Control Register to select operating mode
  - Trigger Register for # of triggers
  - Sample Register for # of samples / trigger
  - Delay register for adjusting ADC clock
  - Clock Divider Register (for internal clocking)

ADC Control Register

	D15	D14	D13	D12	D11		D09	D08	D07		D05	D04	D03	D02		D00
Write	Ch3	Ch2	Ch1	Ch0	x	x	IntTrg	IntClk	x	x	x	HI/LO	DisWr	CMD		
Read	Ch3	Ch2	Ch1	Ch0	0	0	IntTrg	IntClk	0	0	0	HI/LO	DisWr	CMD		

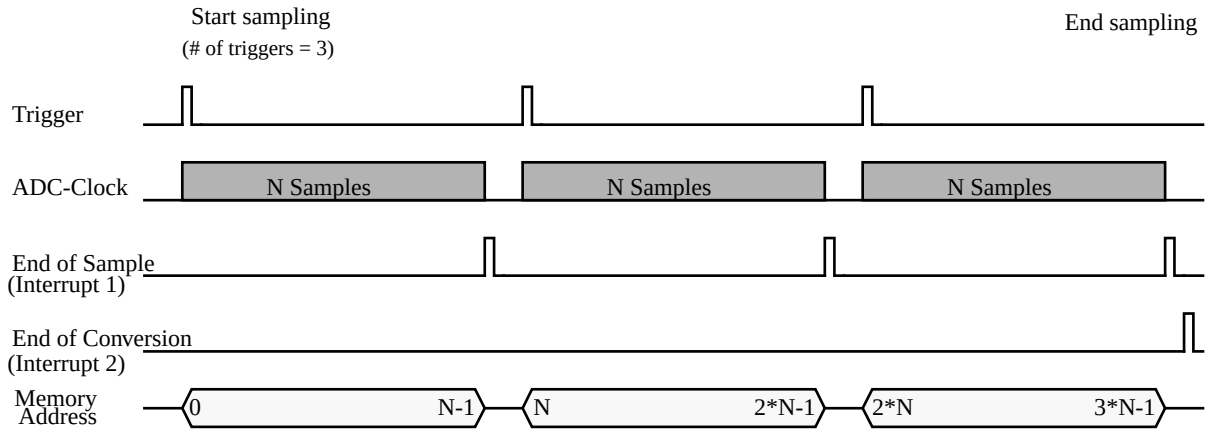
- **CMD** selects mode of operation
  - CMD = 0; Clear (initialize ADC and stop sampling)
  - CMD = 1; Sample Mode
  - CMD = 2; Normal Mode
  - CMD = 4; Stop Mode
- **HI/LO** defines sampling mode
  - HI/LO = 0; low frequency mode (< 2 MHz)
  - HI/LO = 1; high frequency mode (above 2 MHz)

ADC Control Register (cont'd)

- **DisWr** allows to disabe writing to memory during sampling if set (for hardware test purposes only)
- **IntCkl** selects internal clock if set. The clock frequency is defined by Clock Divider Register (f_{ADC_CLK} = 66 MHz / N)
- **IntTrg** selects internal trigger if set
- **Ch3..Ch0** defines data from which ADC channel are send to the DSP port during conversion in high frequency mode (ignored in low frequency mode)

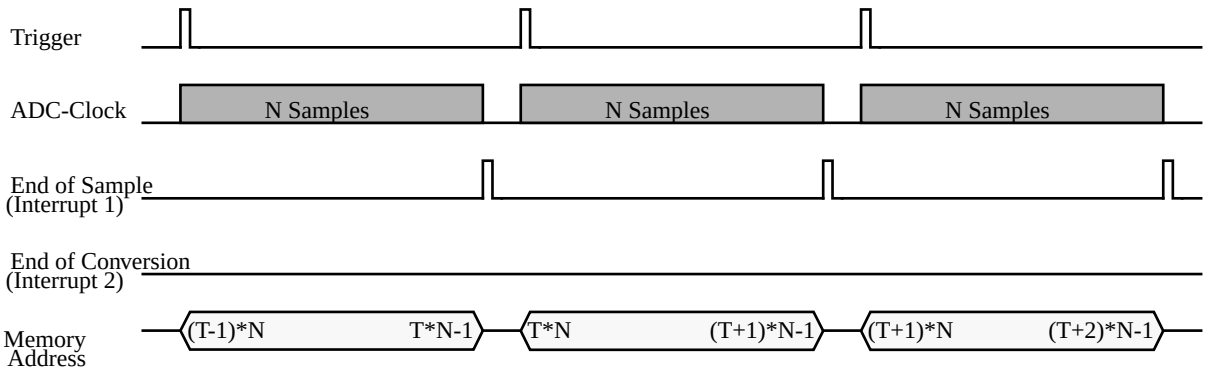
Modes of operation

- Sample mode



Modes of operation (cont'd)

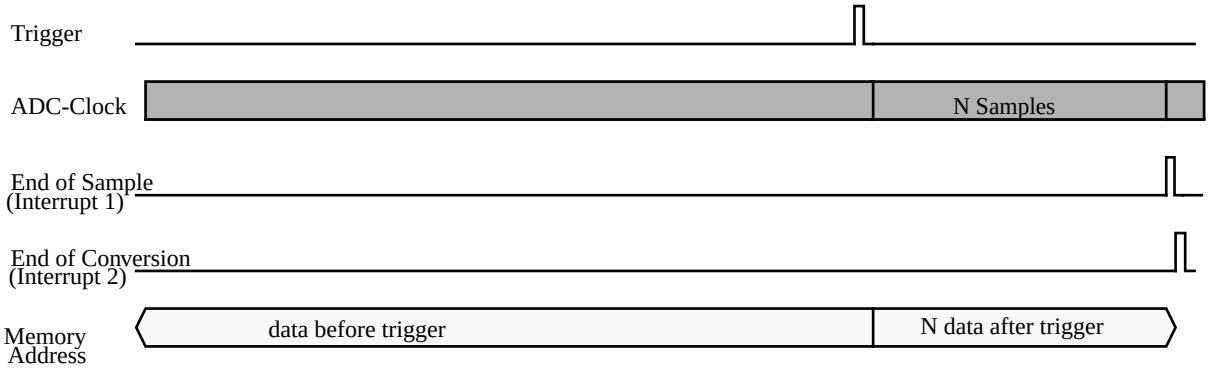
- Normal mode (continuous sampling)



T = # of triggers taken so fare

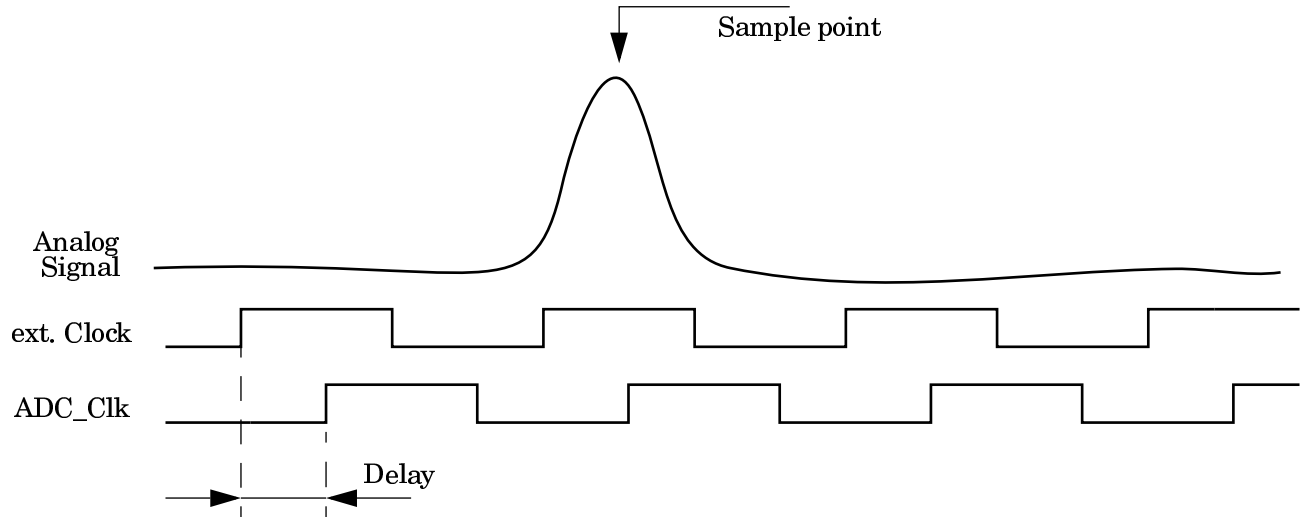
Modes of operation (cont'd)

- Stop mode (free running)



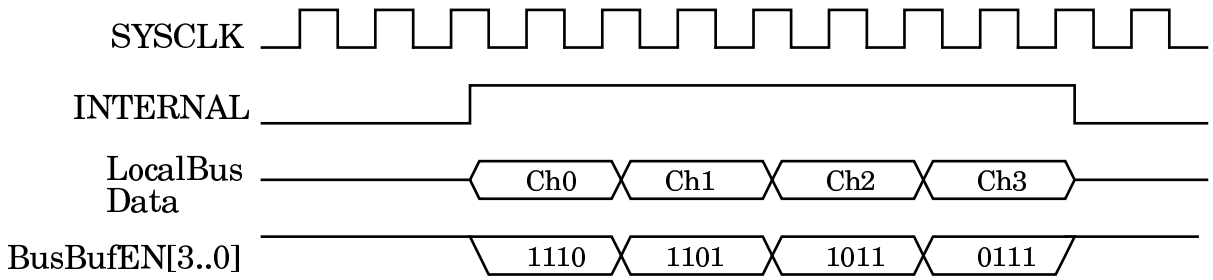
ADC Clock adjustment

- $Delay \approx 40ns$; for Delay Register = 0
- $Delay \approx 5ns \cdot D + 45ns$; for Delay Register = N (1 .. 20)

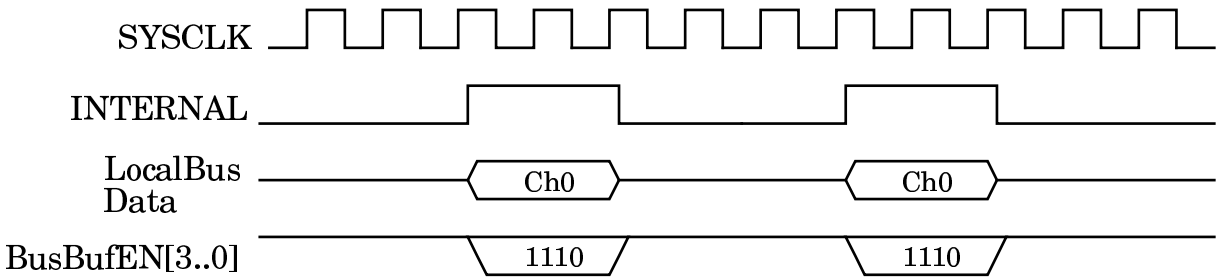


Local bus timing and DSP Output

- in low frequency mode:



- in high frequency mode (CH0 selected in ADC Control Register):



VME Controller

- Standard VME Slave module realized with XILINX FPGA
- Arbitration of Local Bus
  - ADC Controller has highest priority
  - Local Bus Access notified by signal INTERNAL
- VME cycles is executed only if INTERNAL = Low; if an ongoing VME cycle is interrupted by a local bus access from ADC controller it is continued after the bus has been released by the ADC controller

Control Register Address mapping

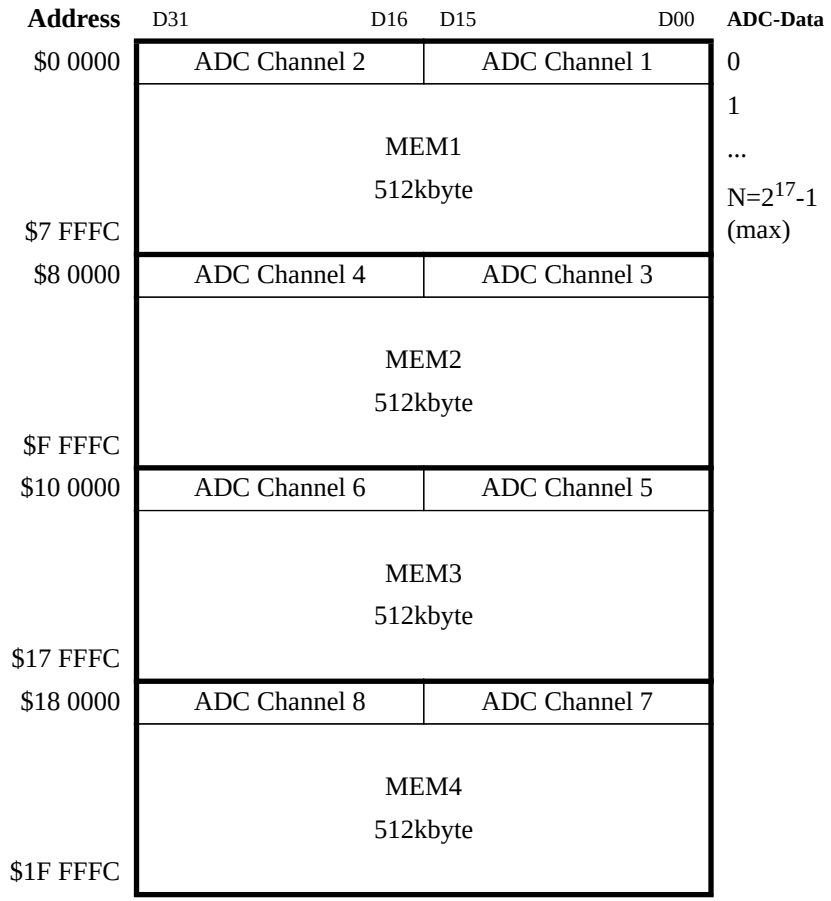
- occupies 256 words within Short Address Range (A16)
- word access (D16) only

Address offset	Register Descrcription
$0	Base Address Register
$2	Interrupt Status Register
$4	CLR Interrupt
$6	Control and Status Register 0
$8	Control and Status Register 1
$A	Read from last memeory location
$C	reserved
$E	reserved
$10	Trigger Register
$12	Sample Register
$14	ADC Control Register
$16	Delay Register
$18	Trigger Counter Register
$1A	Sample Counter Register
$1C	Clock Divider Register
$1E	unused

- base address selected by jumpers

VME Memory address space

- 2MByte within Standard (A24) or Extended (A32) Address space selectable via jumper
- Word (D16) or Long Word (D32) access
- Base Address programmed in Base Address Register (BAR)
- not accessable before initializing BAR



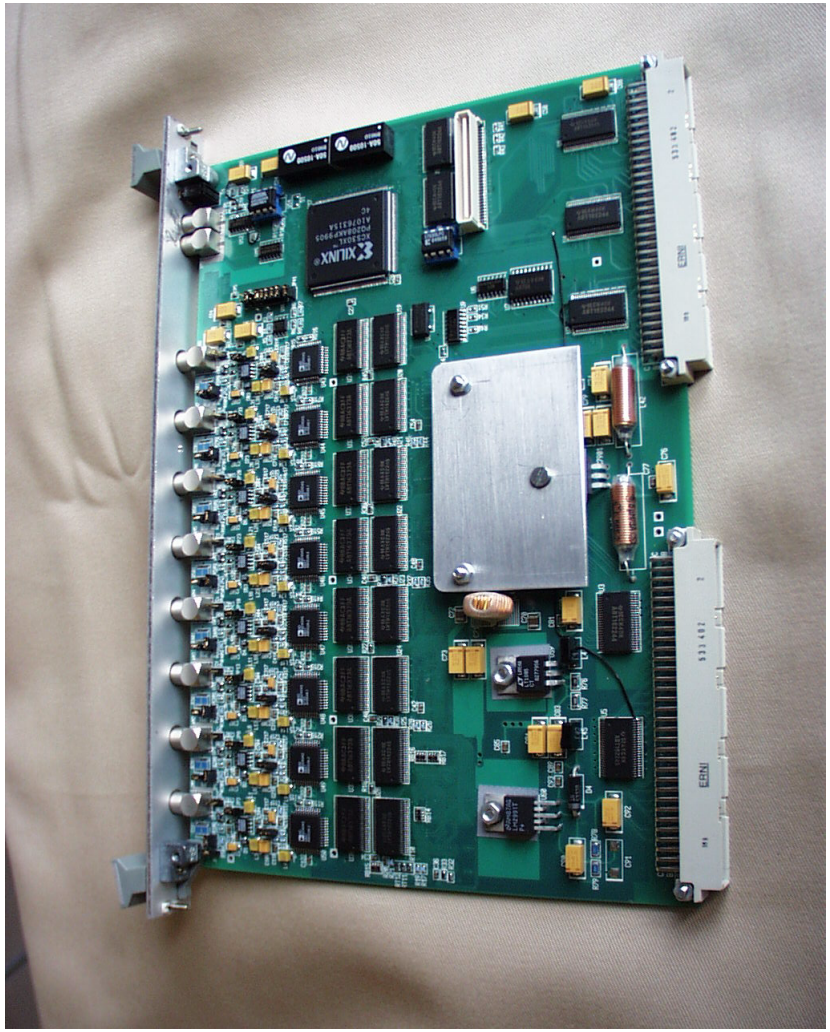
Interrupt Controller

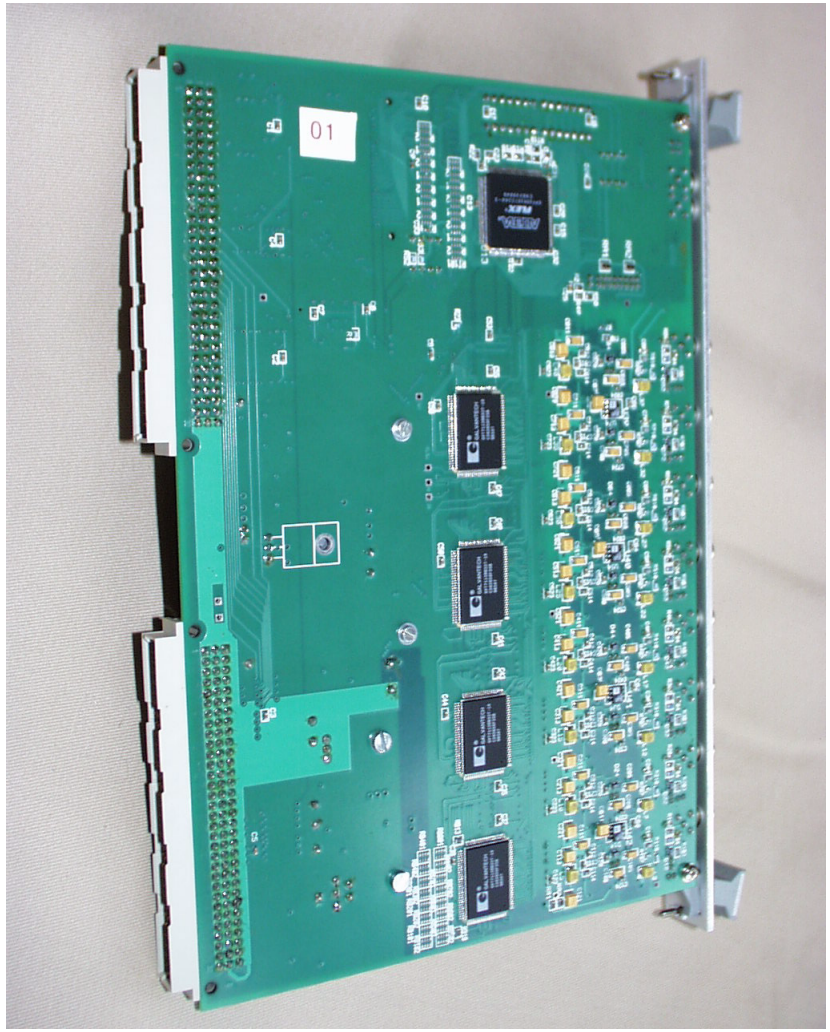
- two interrupt sources:
  - End of Sample (always if Sample Counter = 0)
  - End of Conversion (if Trigger and Sample Counter = 0)
- Programmable Interrupt Level (IRQ7 .. IRQ1)
- Separate Enable for the different Interrupts
- Separate 8 bit ID/Status word
- Programmable as ROAK (Release On Acknowledge) or RORA (Release On Register Access)
- for RORA mechanism write to CLR Interrupt Register

Board layout

- High speed digital design (66 MHz local bus) with high resolution high speed analog design
- 10 layer board
- analog and digital ground on separated layers
- local data bus lines diplaced on 4 layers to guaranty sufficient distance between them to minimize cross-talk, all layers separated either by GDN or VCC planes
- all clock lines, local data and address terminated at the end
- ADC and memory clock in separated layers shielded by ground

top and bottom view of the FastADC

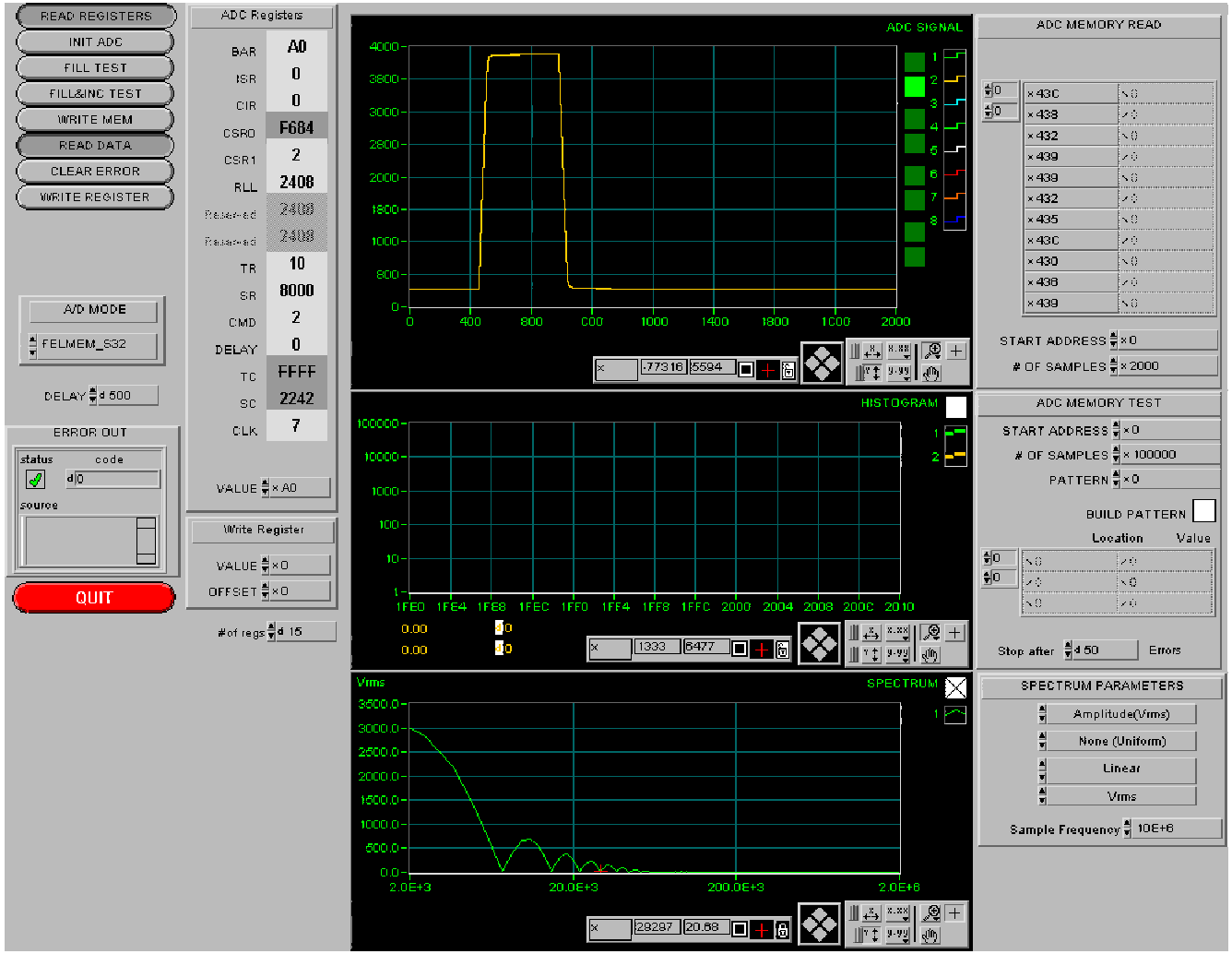




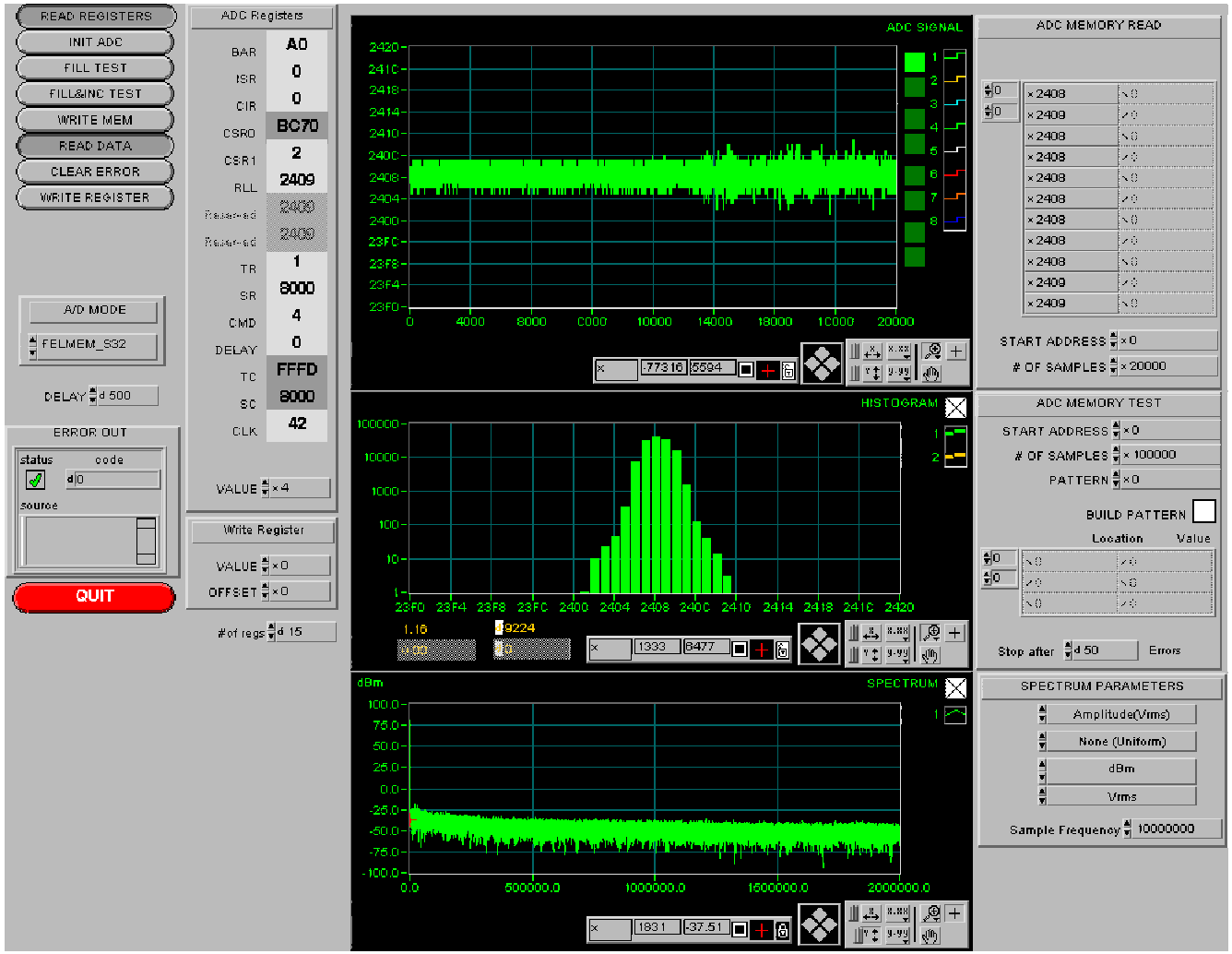
Test program

- Labview used
- read/write register
- memory test
  - filling with predefined pattern
  - incremental filling
- noise measurements
- FFT

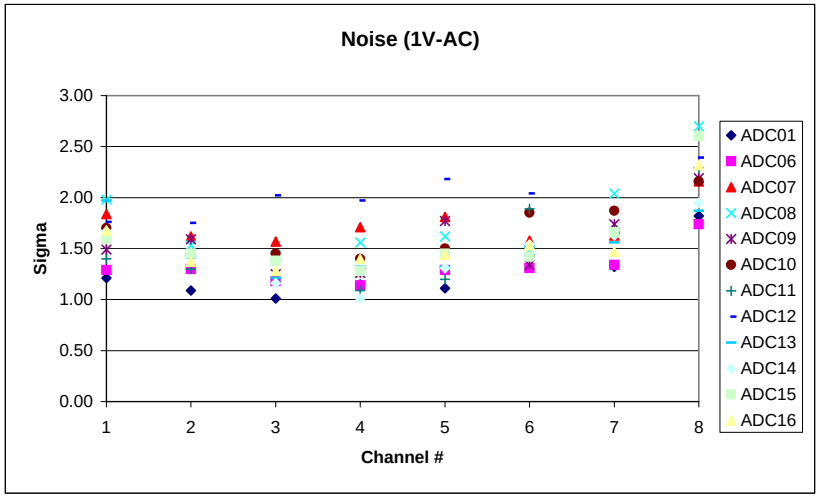
- ADC Test output (+/- 1V range)

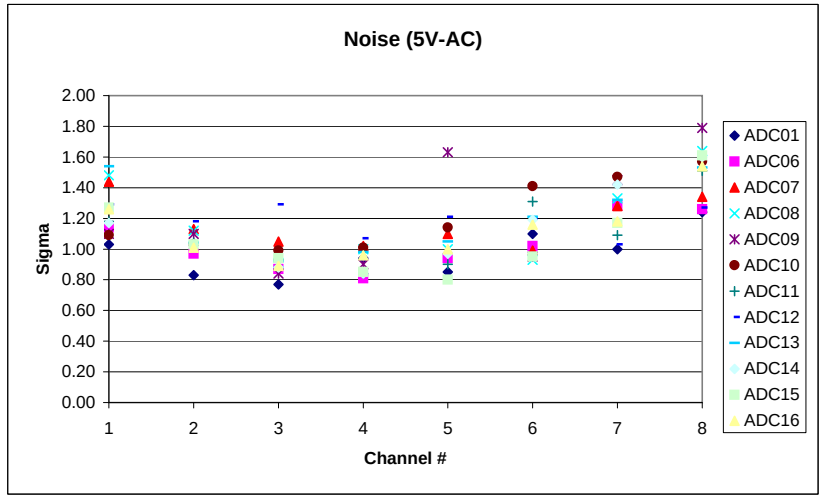


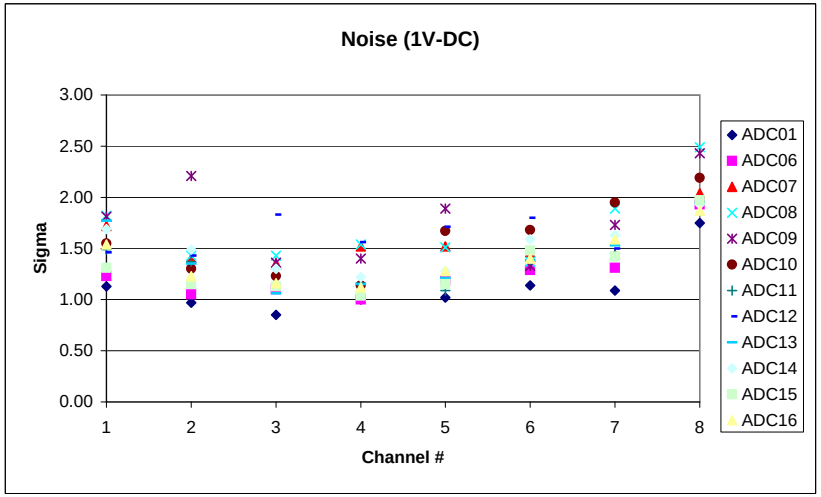
- ADC test output for noise measurement (+/- 5V)

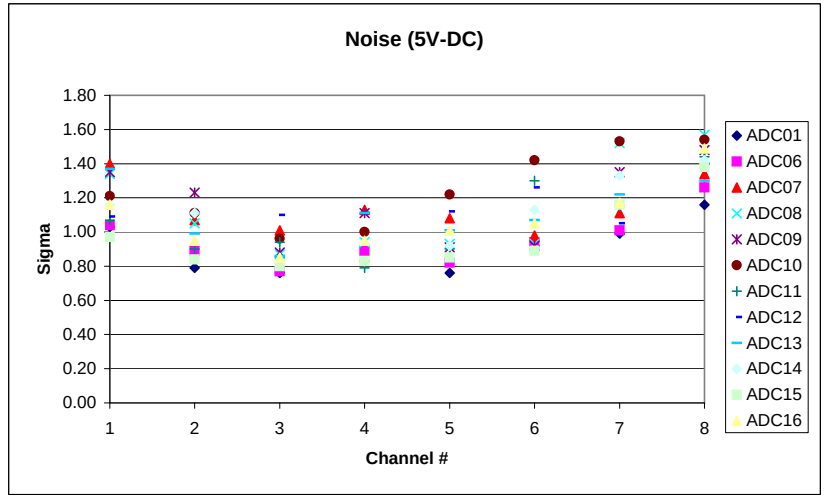


Noise measurements









Outlook

- re-design of analog part
  - realization as piggy-back card to give the customers the possibility to implement the analog input stage according to their own needs
- put ADC and VME control in one FPGA only if possible
- planned to have in next revision an ID-PROM (16 or 32 words)