The PITZ Timing System

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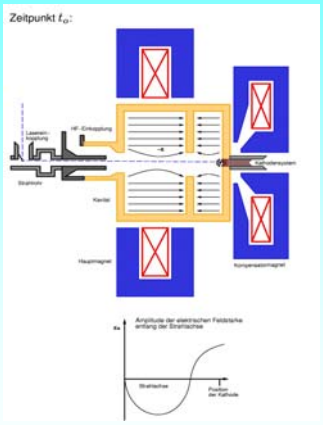
RF-Gun as an Electron Source

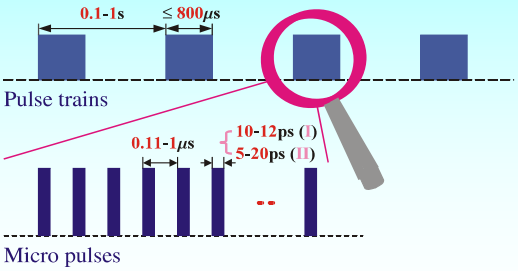


- Laser hits a cathode producing photo electrons
- Electrons are accelerated by a pulsed RF field in the gun cavity
- Laser and RF Source must be synchronized very precisely
- Required Phase Stability $<1ps_{rms}$

Ref: I.Bohnet, Technical Seminar held on 20.Feb.2001, Zeuthen

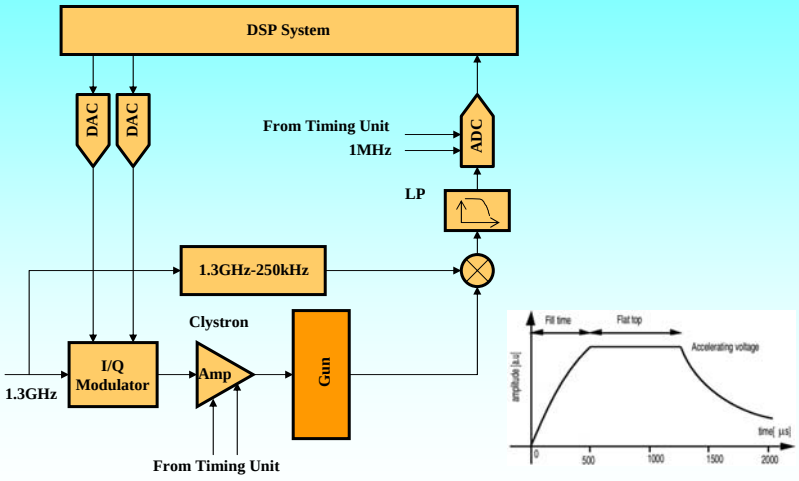
PITZ Timing

- Burst structure
  - Number of pulse up to 800
  - Pulse distance from 110ns (with a future Laser) to 1µs (act. at PITZ)
  - Repetition rate from 1Hz to 10Hz

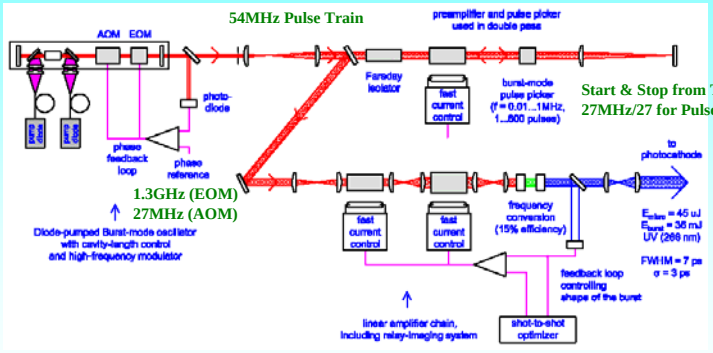


Ref.: I.Will, MBI

Timing for Low Level RF



Timing for Laser Operation

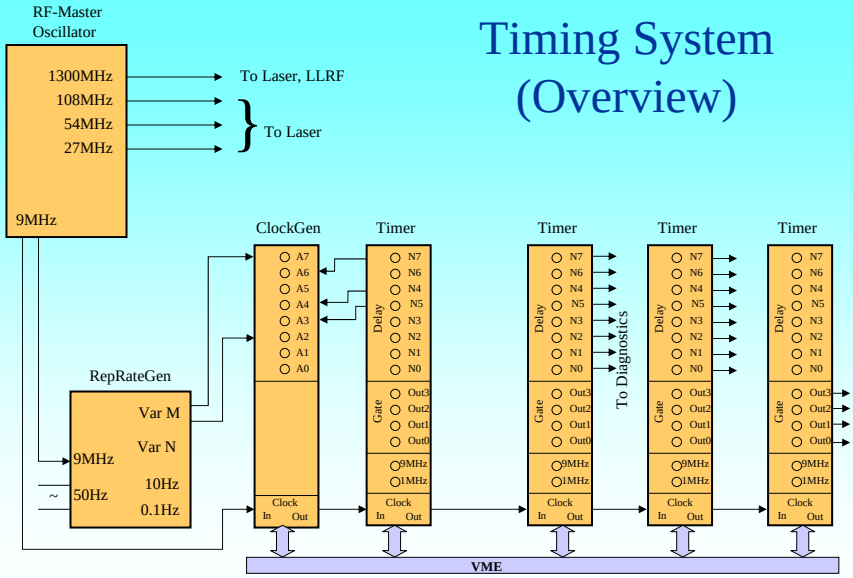


Ref.: I.Will, MBI

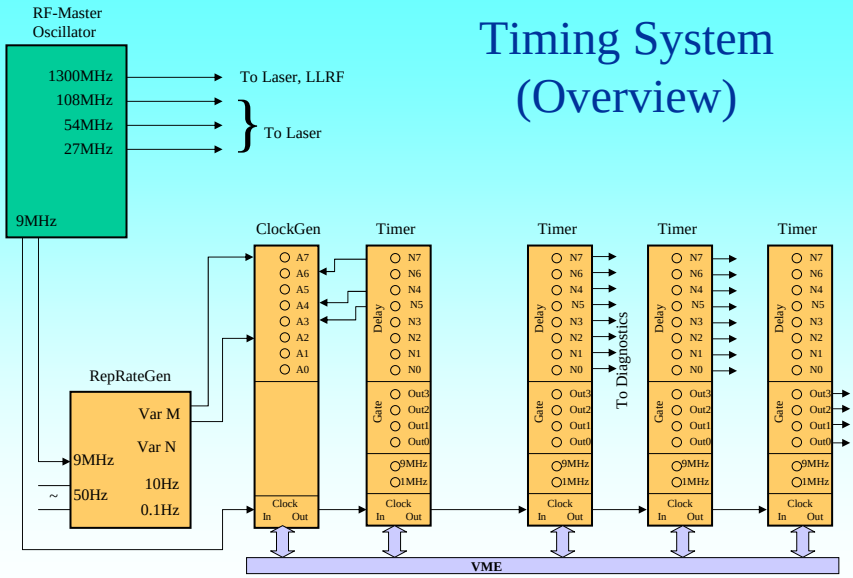
Basic components of the Timing System

- RF Masteroscillator
- Repetition Rate Generator
- Clock Generator (IP-Module)
- Timing Unit (IP-Module)
- Clock Generator and Timing Unit originally where developed at Fermi Lab for the Linac control
- Some modifications for the use at TTF have been done

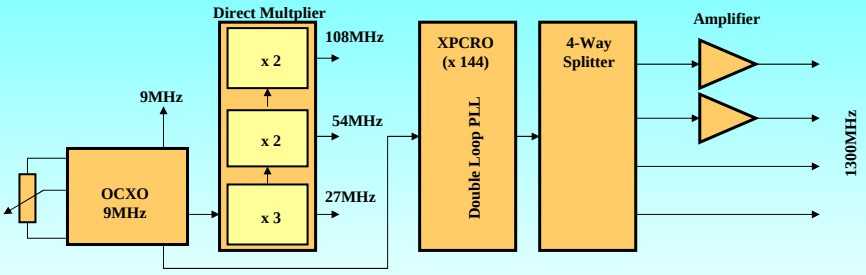
Timing System (Overview)



Timing System (Overview)



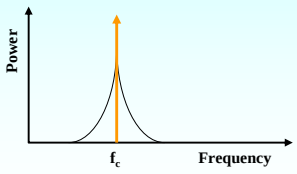
RF Masteroscillator



Masteroscillator:	f_M	9.027775MHz	Timing
	$144*f_M$	1299.999600MHz	RF, Laser
	$12*f_M$	108.333300MHz	Streak Camera
	$6*f_M$	54.166650MHz	Laser
	$3*f_M$	27.083325MHz	Laser

OCXO

- Oven Controlled Crystal Oscillator
- Frequency Stability:
  - Aging Rate/Day: $5*10^{-11}$
  - Aging Rate/Year: $3*10^{-8}$
  - Thermal Stability: $2*10^{-10}$
  - Short Term Stability: $2*10^{-12}$
- Phase Noise (from Specification):
  - 1Hz -90dBc
  - 10Hz -120dBc
  - 100Hz -140dBc
  - 1kHz -155dBc
  - 10kHz -155dBc
  - 100kHz -155dBc



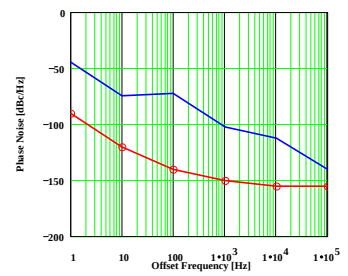
Frequency Multiplier

- Direct Frequency Multiplaction on non-linear devices
  - Phase Noise Deviation: +20*log(N)+3dB
- or with PLL-Devices (Phase Locked Loop)
  - Phase Noise (from Specification):
    - <100Hz +20*log(144)+3dB
    - 100Hz -72dBc
    - 1kHz -102dBc
    - 10kHz -112dBc
    - 100kHz -140dBc

Integrated Phase Jitter

- Can be calculated from Phase Noise:

$$\overline{\Phi_{rms}} = \sqrt{\int_{-f_B}^{+f_B} \frac{P_N(f)}{P_C(f)} df} = \sqrt{2 \cdot \int_{0}^{+f_B} \frac{P_N(f)}{P_C(f)} df}$$



Masteroscillator:

$\Delta\Phi_{MOrms} = 1.881 \cdot 10^{-3}$ ◦deg

$t_{MOjitter} = 5.789 \cdot 10^{-13}$ •s

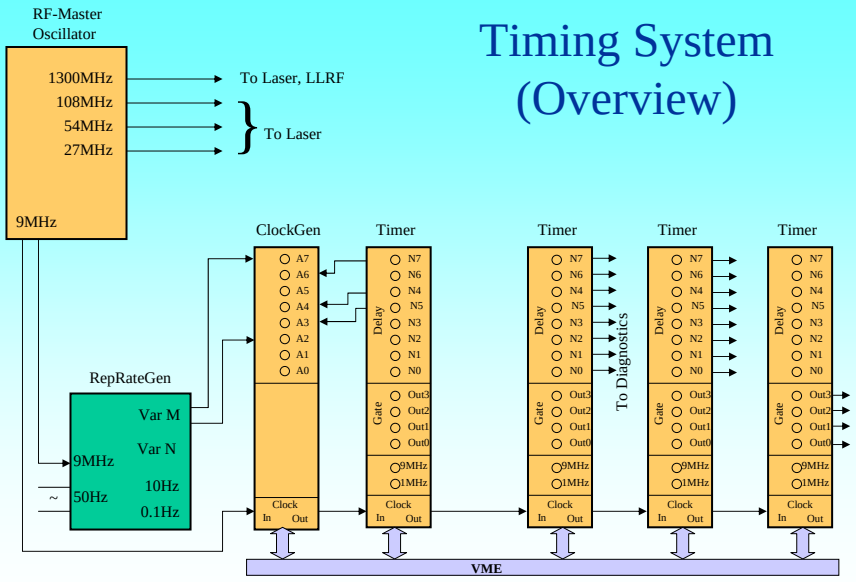
XPCRO:

$\Delta\Phi_{XPCROrms} = 0.428$ ◦deg

$t_{XPCROjitter} = 9.151 \cdot 10^{-13}$ •s

Ref.: W.P.Robins, Phase noise in signal sources, Peter Peregrinus Ltd, London, UK, 1084

Timing System (Overview)

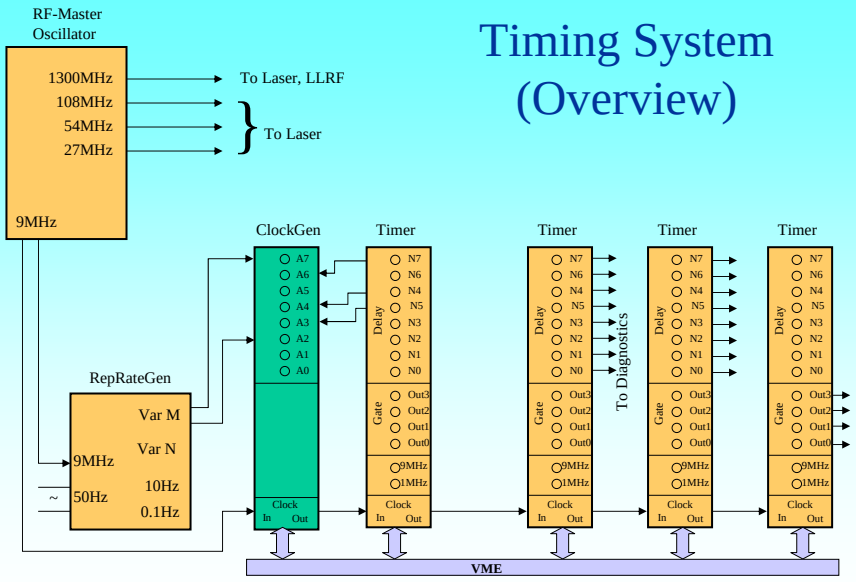


Repetition Rate Generator

- Operates on 50Hz AC line (zero crossing detector)
- Division by 5 gives 10Hz
- Further division

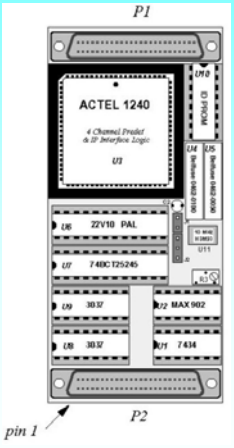
Outputs		
fixed	variable	
	M	N
10Hz	10Hz	M/1
	5Hz	M/2
	2Hz	M/5
	1Hz	M/10
	0.5Hz	M/20
	0.2Hz	M/50
0.1Hz	0.1Hz	M/100

Timing System (Overview)



Clock Generator (I)

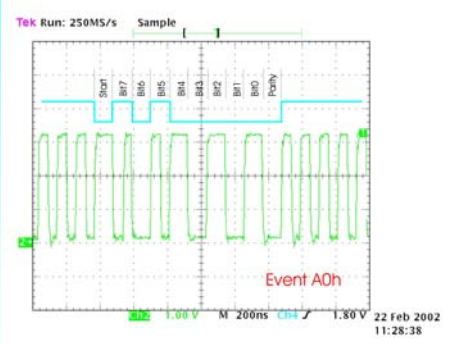
- IP-Module
- Logic (on ACTEL chip) containing:
  - IP Interface logic
  - TCLK Decoder (Tevatron style clock)
  - Serializer & Manchester Encoder
  - Prioritizer for Decoded Events, Input latches & Computer Events
  - Computer Event Latch
  - 8 Input Latches
- Normally one module in the System



Ref: from Users Manual

Clock Generator (II)

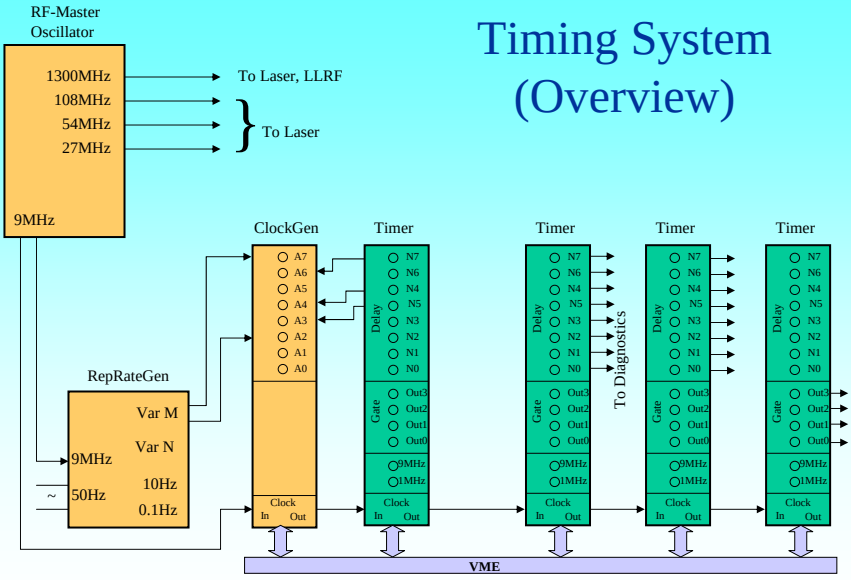
- Manchester Code
  - „0“ no transition in the middle of the bit
  - „1“ transition in the middle of the bit
  - allways transitions on bit bounderies
- allow easily clock recovery



Clock Generator (III)

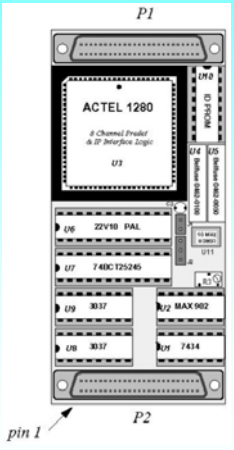
- TCLK Events
  - 0xh; 1xh, 2xh from incoming clock
- Trigger Events
  - A7h-A0h, generated from inputs IN7-IN0
  - B7h-B5h, generated from reference event A6h
    - B7h every 16th A6 with 6µs delay
    - B6h every 32th A6 with 9µs delay
    - B5h every 64th A6 with 12µs delay
- Computer Events
  - C0h-CFh, writing to an internal register

Timing System (Overview)



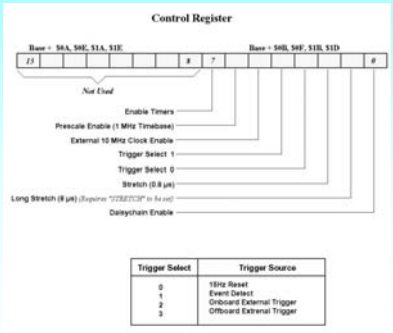
Timing Unit (I)

- IP-Module
- Logic (on ACTEL chip containing:
  - IP Interface Logic
  - TCLK Decoder (Tevatron style clock)
  - Serializer & Manchester Encoder
  - Prioritizer for Events
  - 4 16-bit Event Registers
  - 6 16-bit Delay counters
  - 8 16-bit Delay Registers & Comparators
  - 4 16-bit Control Registers



Timing Unit (II)

- one Event & Control Register for 2 Delay Outputs at a time



Timing Unit (III)

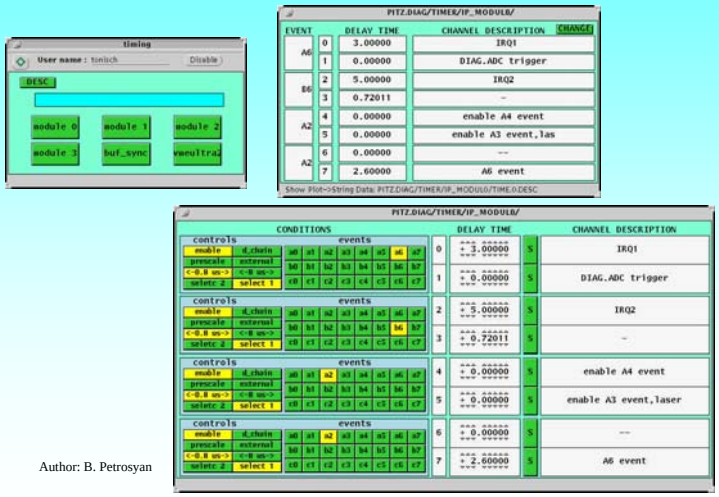
- 8 Delay Outputs
- Timebase 110ns (Prescale bit =0) or 1µs (Prescale bit =1)
- Pulse length control
  - 110ns , 800ns or 8µs
- Daisy Chain Mode
  - Channel 2,3 (6,7) started by Channel 0,1 (4,5) resp. allowing for long pulses

Timing Unit (IV)

- 4 Gate Outputs
  - Gate 0 started with Out0 & removed with Out2
  - Other trigger pairs:
    - Gate 1: 1-3
    - Gate 2: 4-6
    - Gate 3: 5-7

Timing Control Comand

(timingctr at corvus)



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