innovations
for high
performance
microelectronics

Dedicated Processors for Wireless Systems

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New Institute and Cleanroom

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What is the IHP?

- **German National Lab focused on broadband and mobile connectivity**
  - **200 staff, $30M annual base budget**
  - **Core competencies in technology, circuit design, systems**
- **Successor to Institute of GDR Academy of Sciences**
  - **Major role in developing microelectronics technologies**
  - **Winner of 17 GDR national prizes**
- **Refounded 1991 as classic German research institute**
  - **“Application-oriented fundamental research”**
- **Focus on innovation, major re-engineering started 1996**
  - **Prof. Abbas Ourmazd leads the institute with US spirit**
- **Customer base of 30 international companies**
  - **Intel, Motorola, Lucent, Infineon, Alcatel, Siemens, et al.**

IHP in a Nutshell

- **Strategy**

  focus on wireless communication (initially in the 2 - 10 GHz range)

  going up to 60 GHz and RADAR using high performance SiGeC technology

  collaborate closely with strategic industry partners

  core competencies range from system and circuits design to technology and process development

  seek synergy between material physics, process technology, circuit design, systems, and applications (vertical approach)

  prototype forward-looking, system-level solutions with secured migration paths into the market

IHP in a Nutshell

- **Competencies**

  System Activities started 1999 (now 26 people)

  Wireless Internet applications and protocols; Broadband radio LANs (up to 1Gb/s); Body area networks; System on Chip

  Circuits started 1997 (now 10 people)

  CMOS for RF 2.4 GHz level

  Wireless LAN 5.8 GHz, a domain for SiGe technology

  60 GHz components for Gb WLAN

  Radar Circuits for automotive applications (76-124 GHz)

  UWB Frontends for ultra low power systems (e.g. body area networks

  LDMOS Power Electronics (integrated power amplifiers, switches power control circuits)

  Process Technology (86 people)

  SiGe:C HBT module for post-CMOS Integration

  Performance (>200GHz f_t, f_{max}) comparable with IBM with much simpler process

IHP-Structure

Sci. Advisory Council
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Head

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Prof. B. Dietrich
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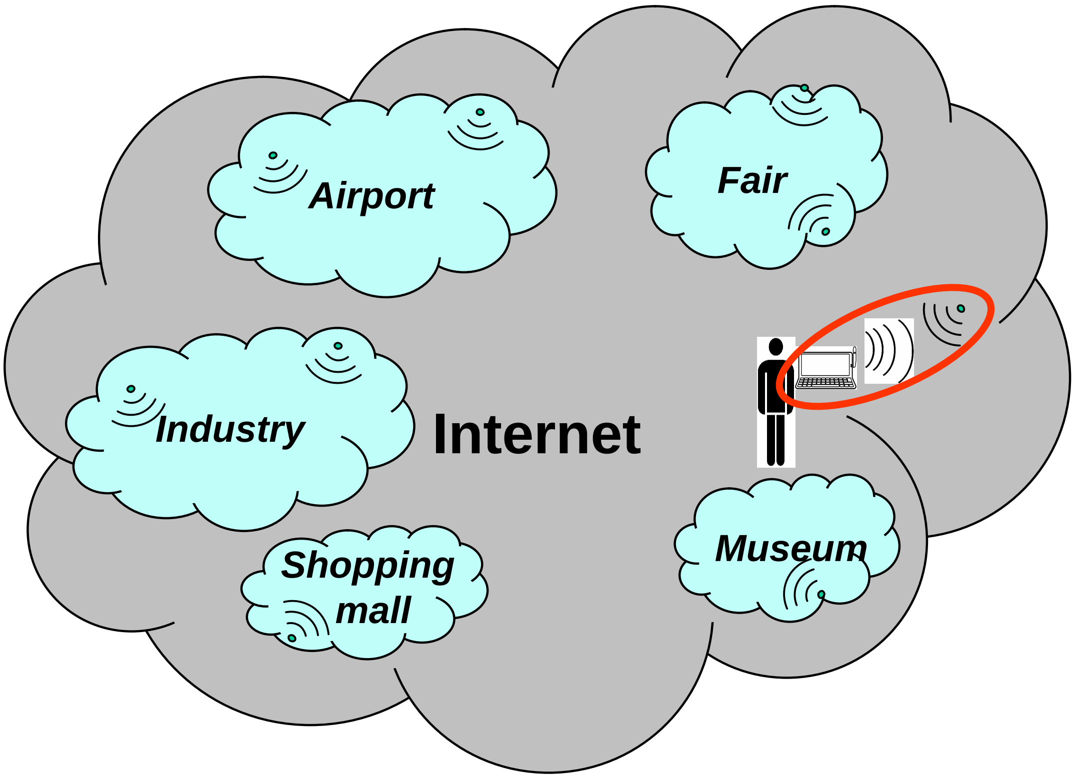
Process Integration & Pilot Line
F. Fürnhammer
Head & Technology Coordinator

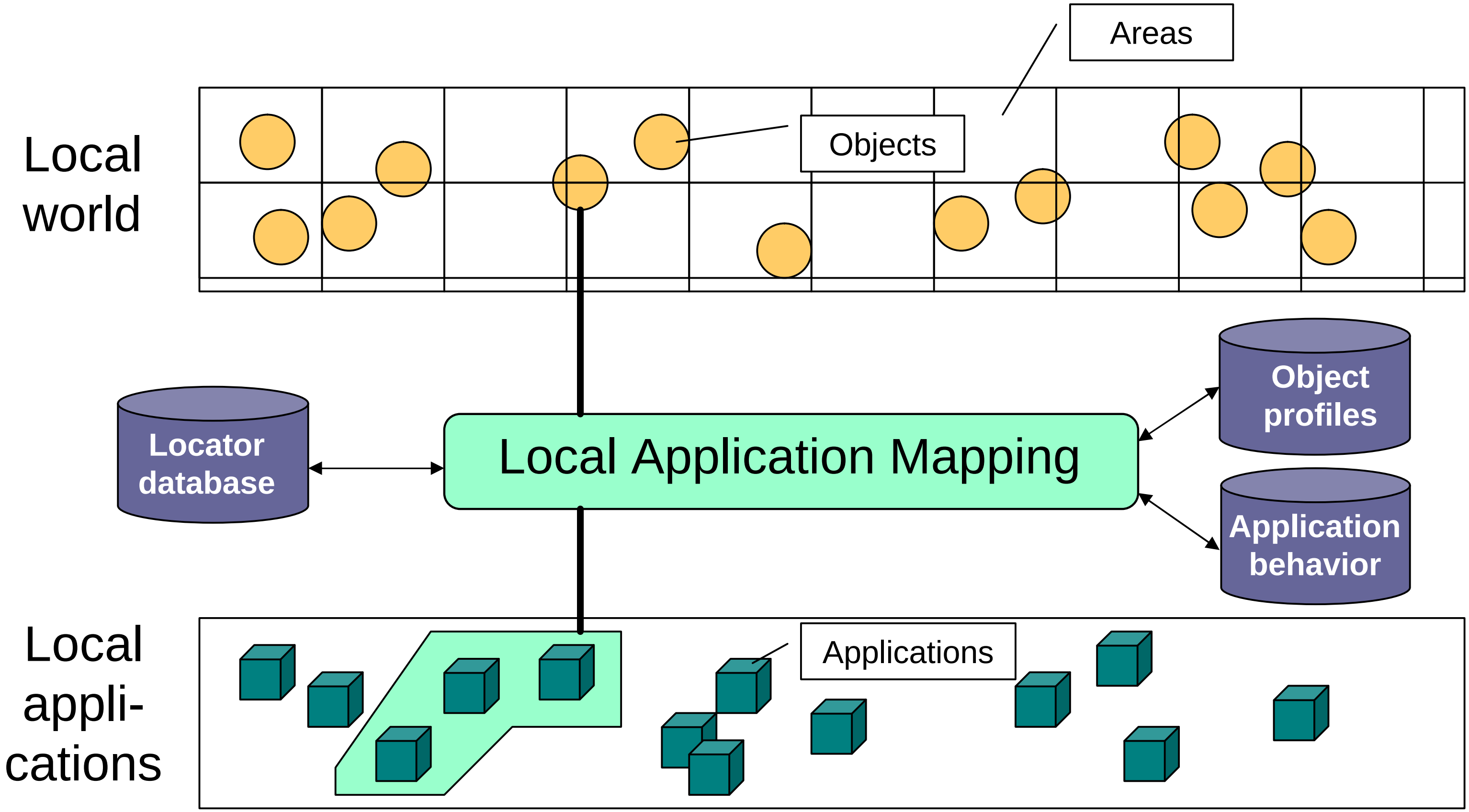
Process Research
Dr. B. Tillack
Head

Materials, Diagnostics, Foundry
Dr. W. Krüger
Acting Head

Wireless Internet



Location-Awareness in Concept



Services

- **Local information delivery**
  Push and pull modes

- **Location-dependent services**
  Train information at the station, etc.

- **Tagging (attachment and selective use of information to objects)**
  Tell me, but not Jane, it is her birthday as she goes by

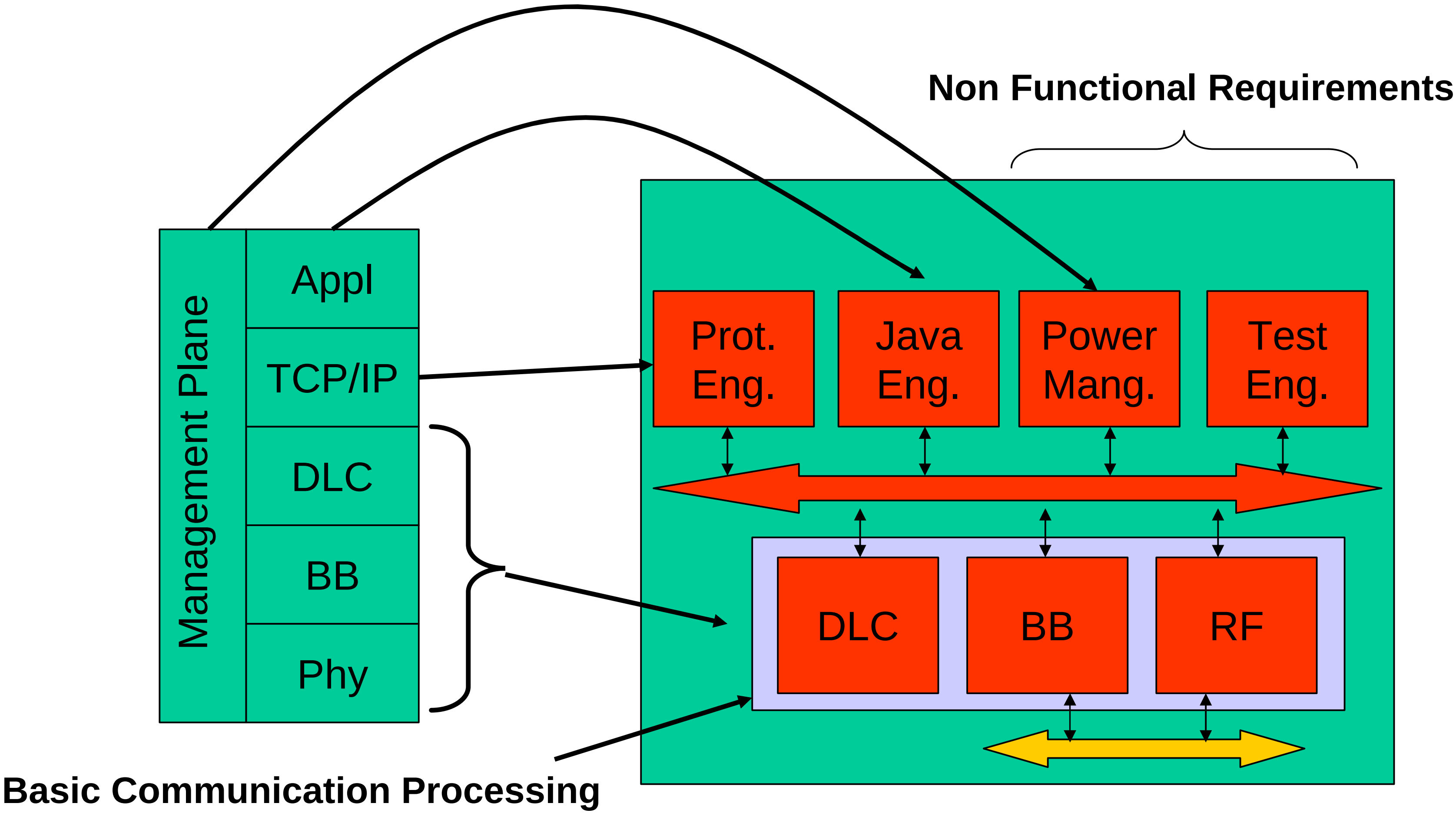
- **Third party notification**
  Your teenage daughter has gone into the disco

- **Location & navigation services**
  Complex, property-based queries

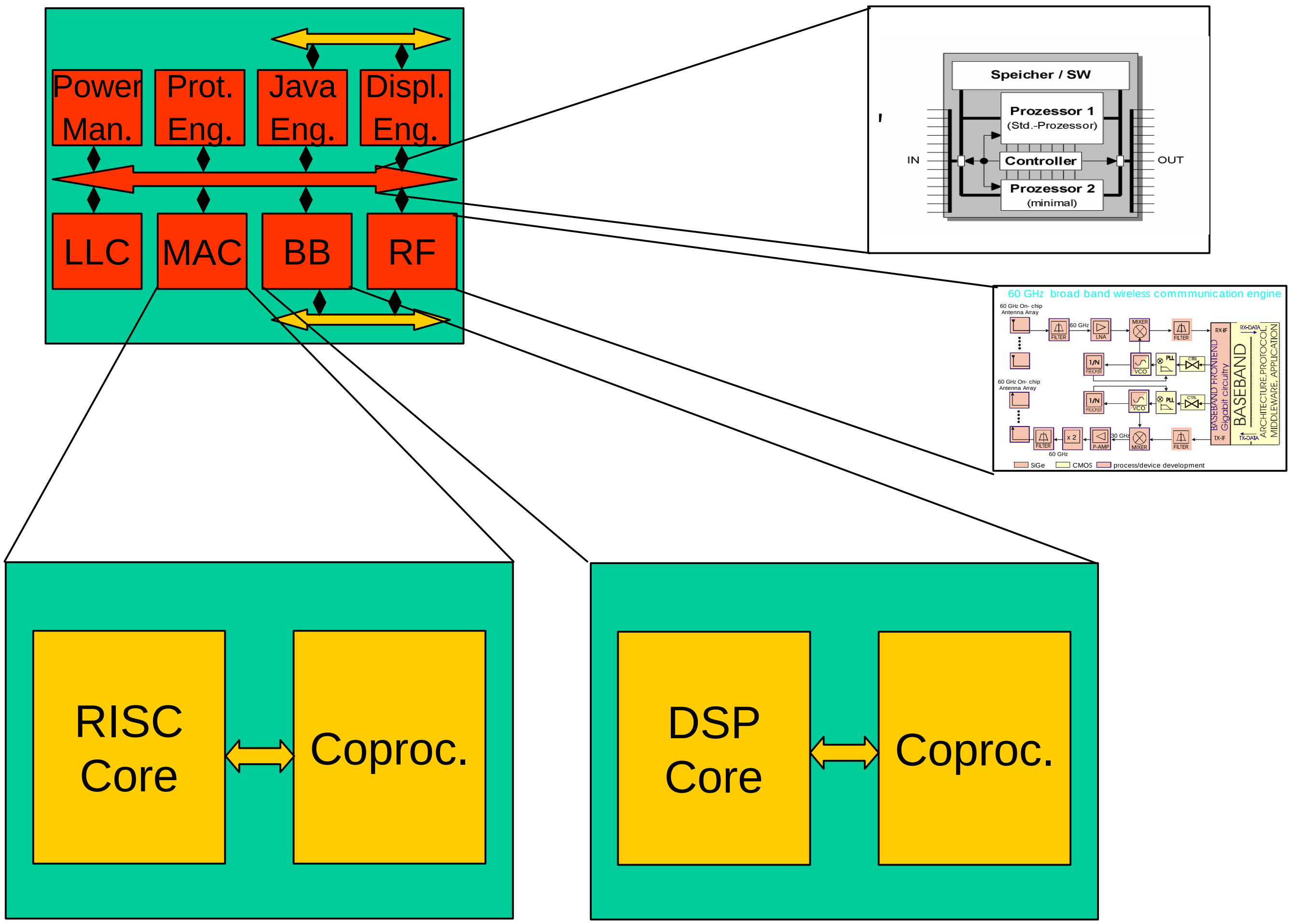
Wireless Internet Challenges

Attribute	Now	Needed	Challenges
Bandwidth	9.6 Kb/s 140Kb/s GPRS	20-50 Mb/s 1Gb/s planned	1000x 10000
Processing	100 MIPS	10,000 MIPS	100x
Power consumption	1 mW/MIPS	0.01 mW/MIPS	100x
No. of chips	10-50	1	Not possible at present
Form factor	Brick	Single chip Distributed	Internal comms., Power distr., Package
Software	Win Ce, PalmOS	Java/Jini	HW independent SW
Services	VOICE+ data	TRANSACTIONS + DATA + voice	Integrated, seamless, secure
Features	Undifferentiated	Location, Context Environment aware	Need platform
Cost	$299	$99	Margin too low for service pricing

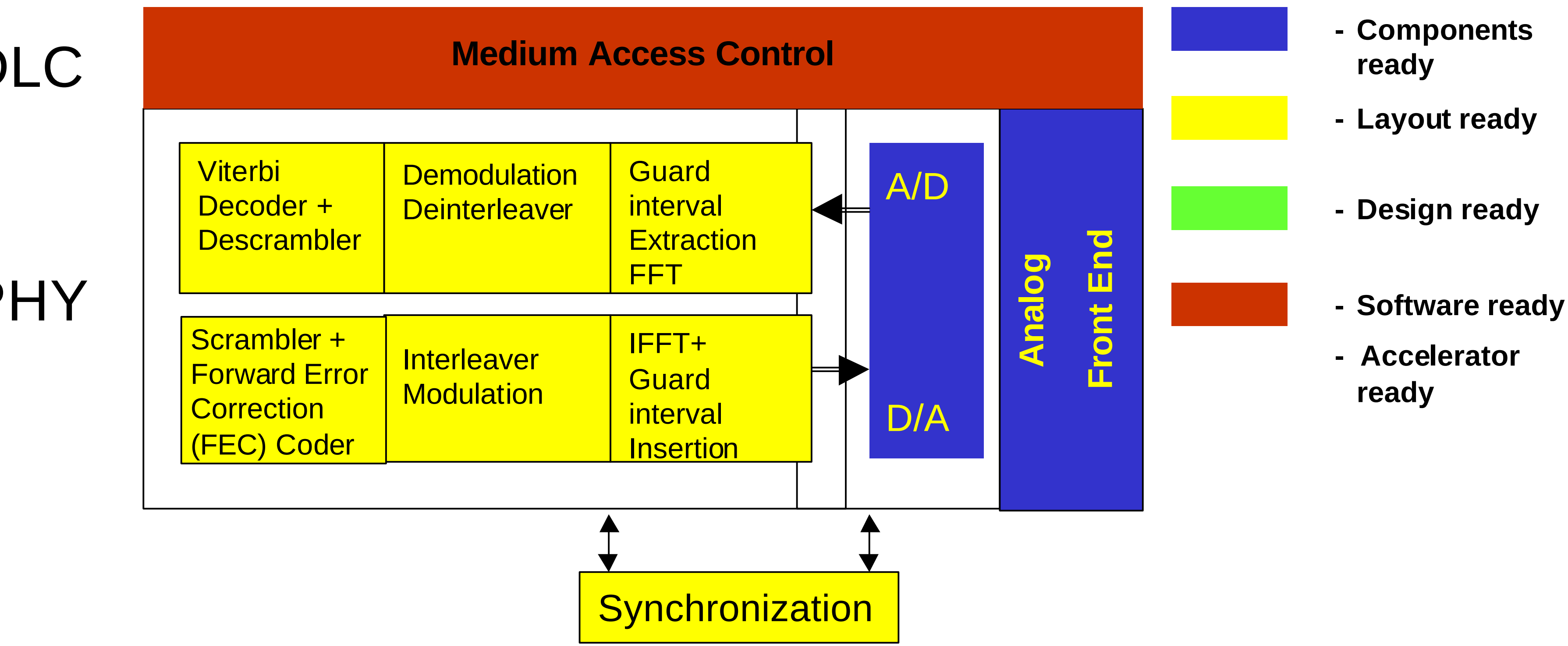
Wireless Engine



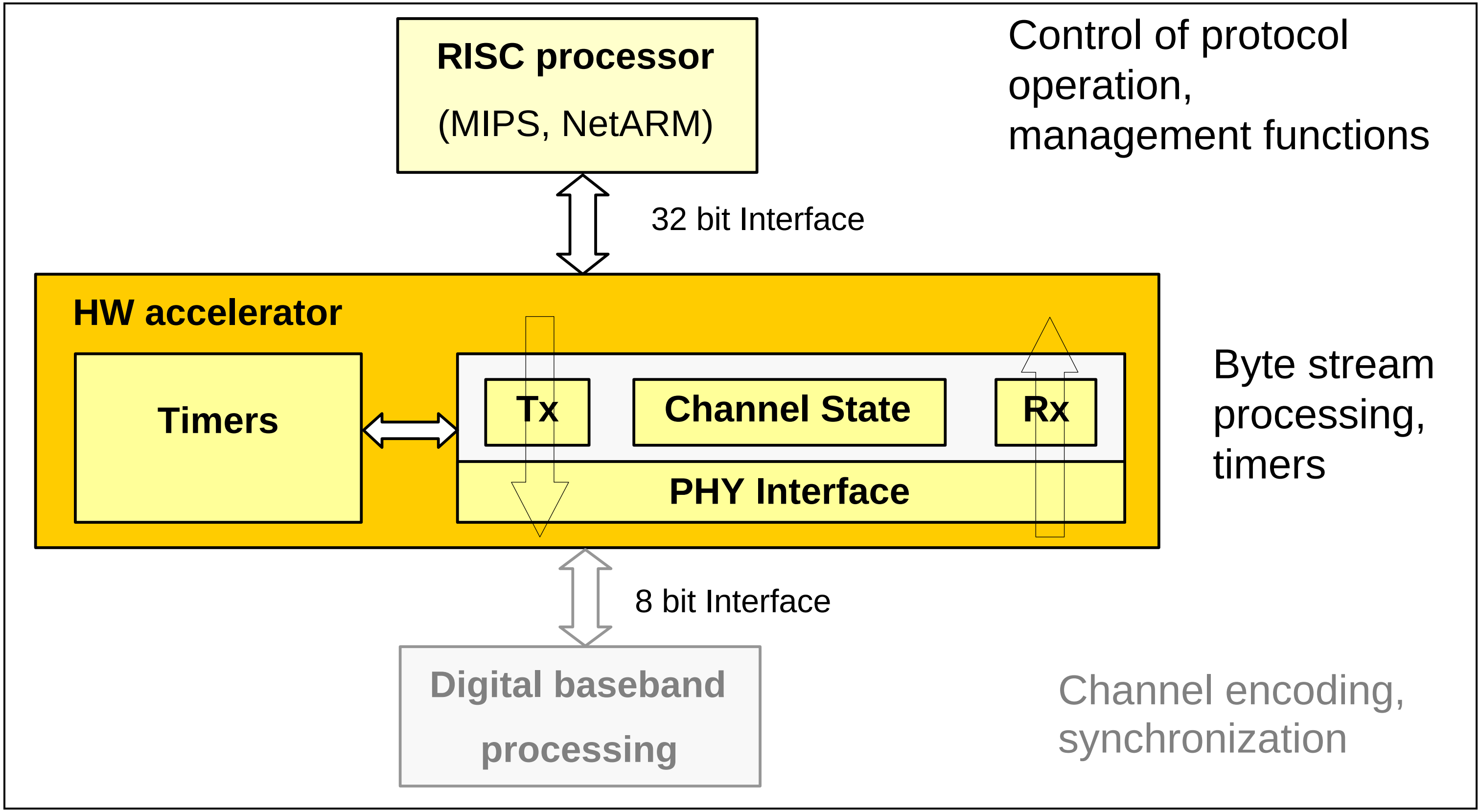
Wireless Engine



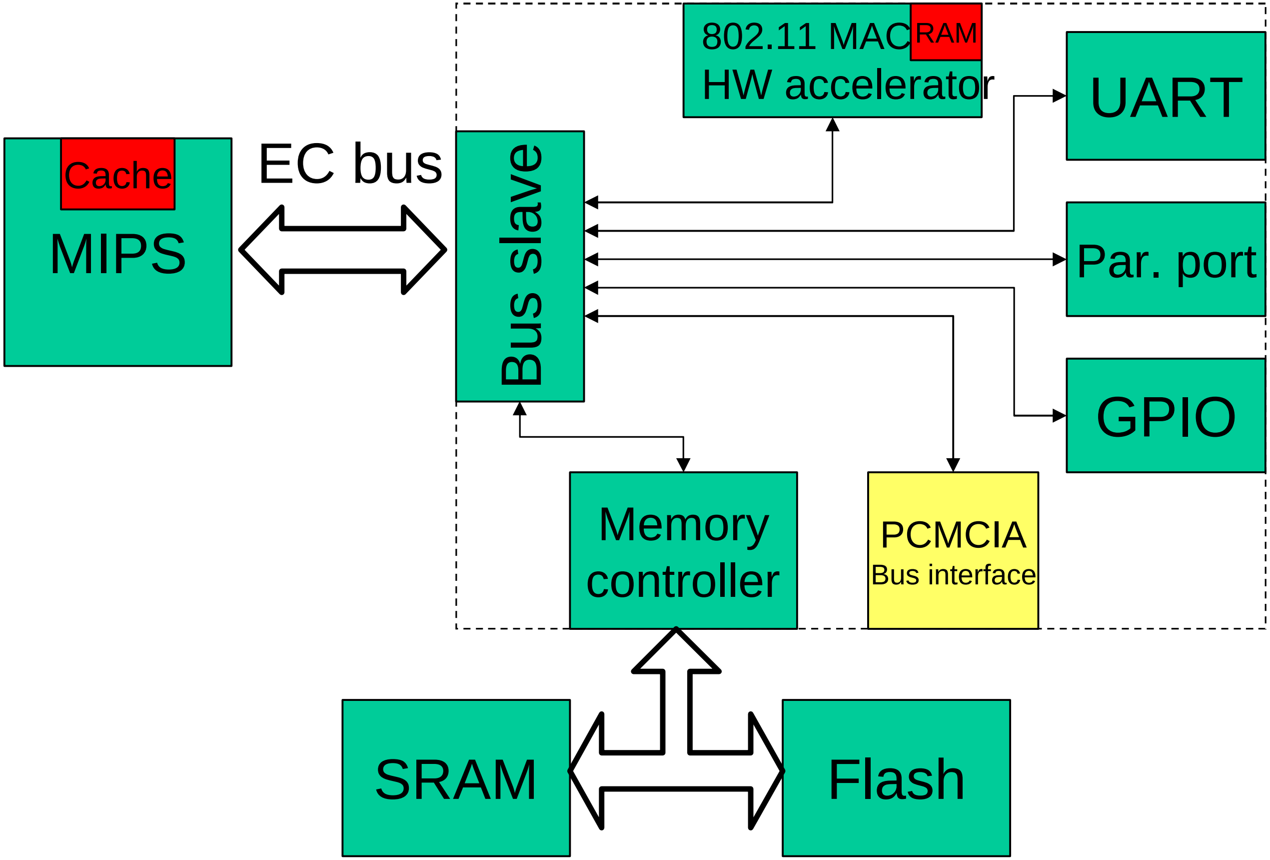
WBN system modules



MAC Accelerator



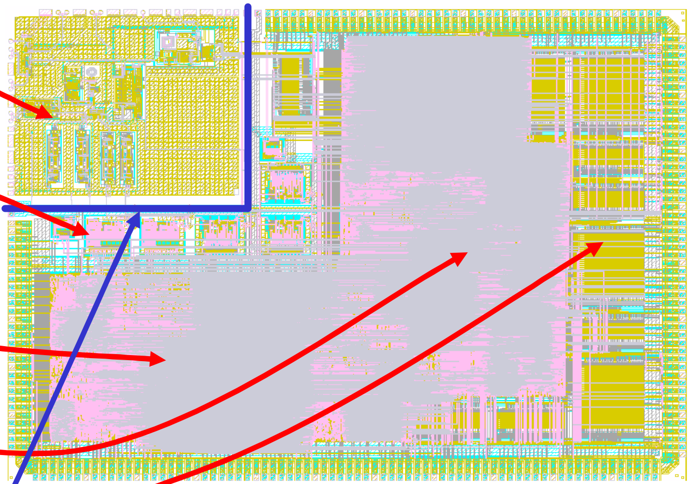
MIPS Target Architecture for 802.11a



World first: 1st Single-Chip 5 GHz Modem

Main Components:

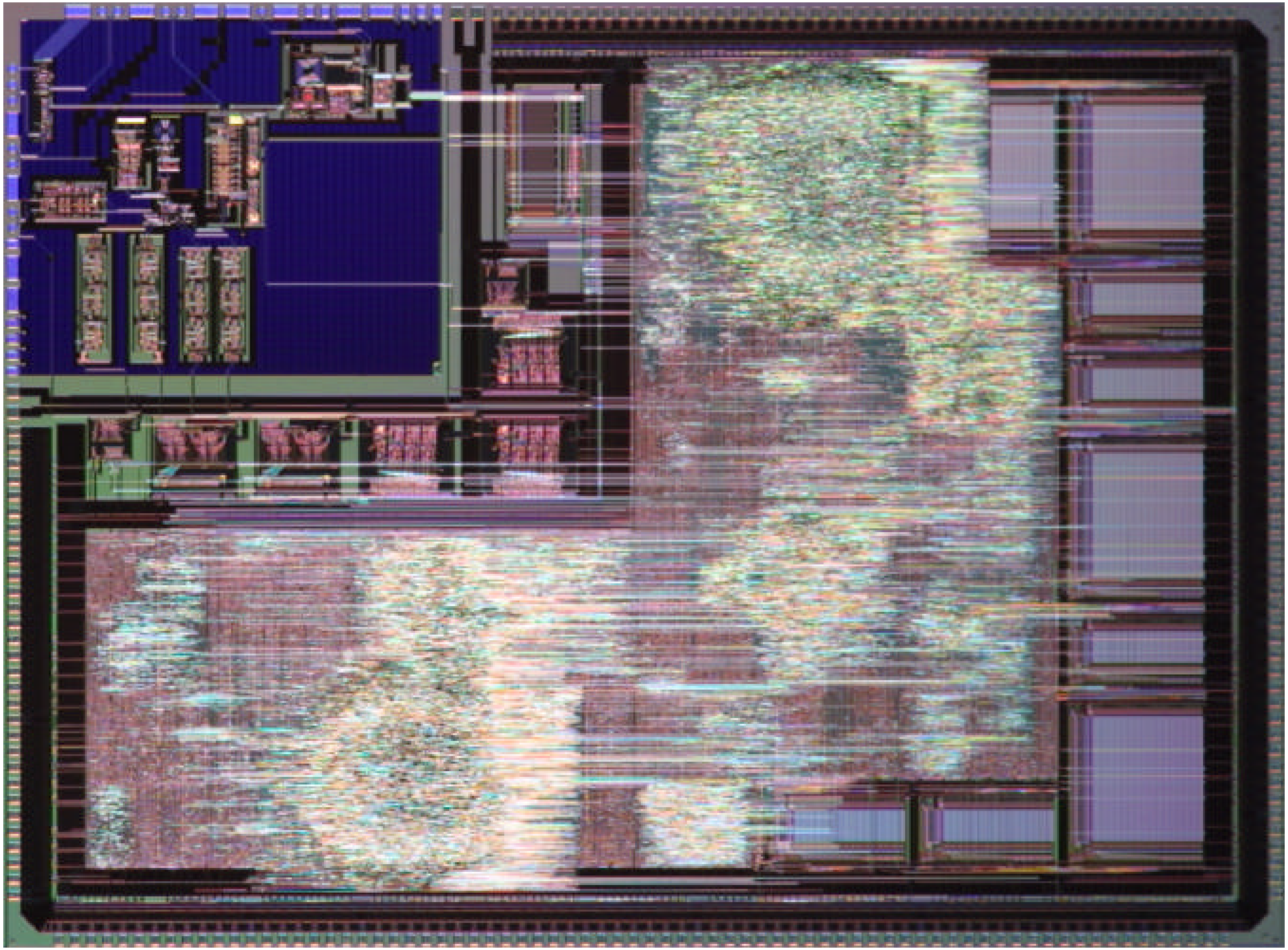
1. **5 GHz Analog Frontend (5,8 GHz Superhet., IF 810 MHz)**
2. **A/D and D/A Converters (7 Instances)**
3. **OFDM Baseband Processor with Synchronisation and Channel Estimation**
4. **MAC-Processor (MIPS-4kE) with Hardware-Accelerator**
5. **PCMCIA (CardBus) Interface plus 2x UART and 1x I²C-Bus Interface**
6. **Cache-Memory for MIPS und Data Buffers (44 kByte in total)**
7. **Built-in Self-Test (BIST) with various specific test-modi**
8. **EMI protection: n-well Ring, GND-Ring, Buried Layer inside AFE**



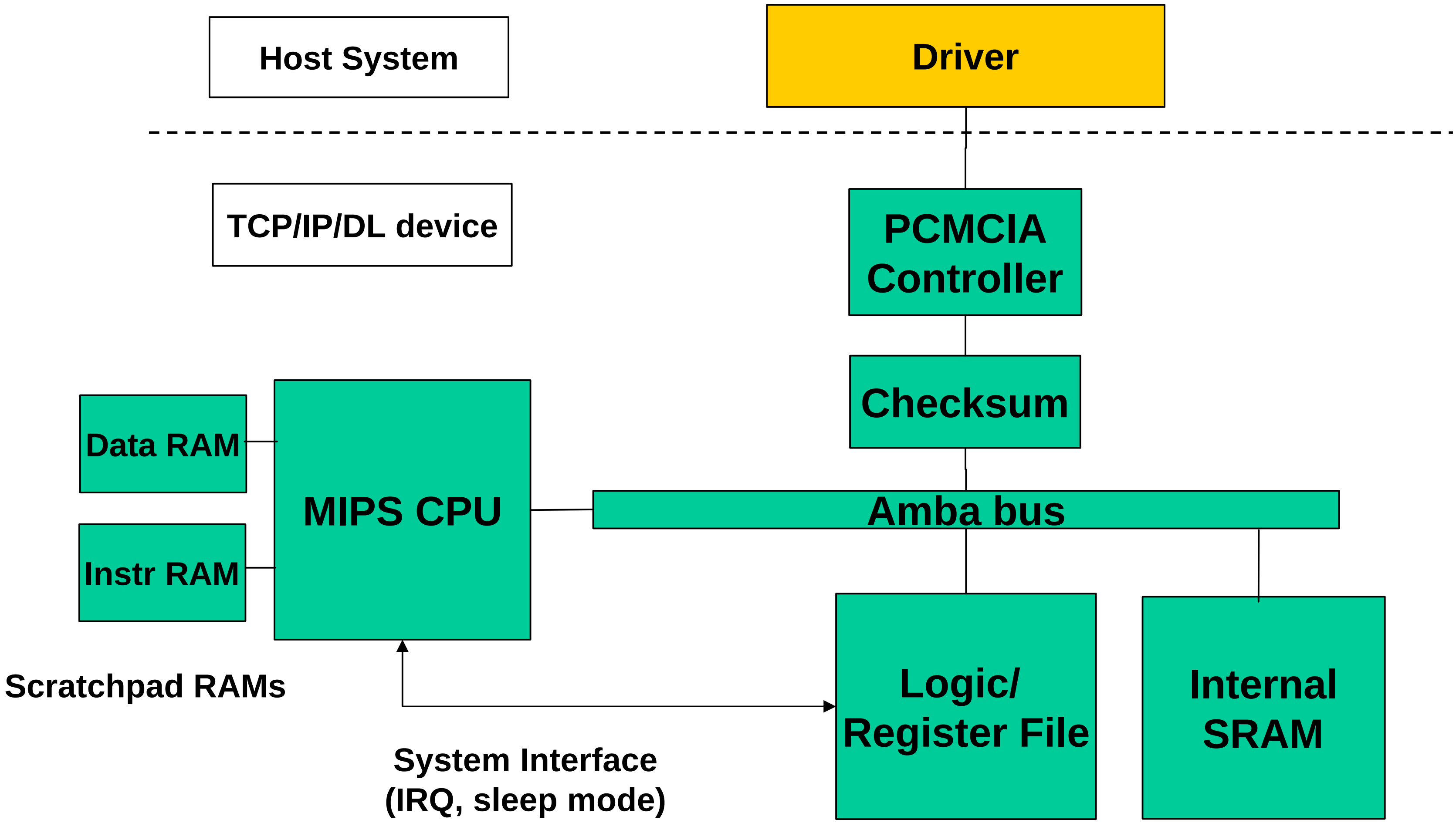
Main Parameters :

- **Chip-Area:** ca. 90 mm²
- **No. of Pins:** 240
- **Power dissipation:** 2W (simulate
- **Clock frequency:** 80 MHz

Single chip 5 GHz IEEE 802.11a Photo



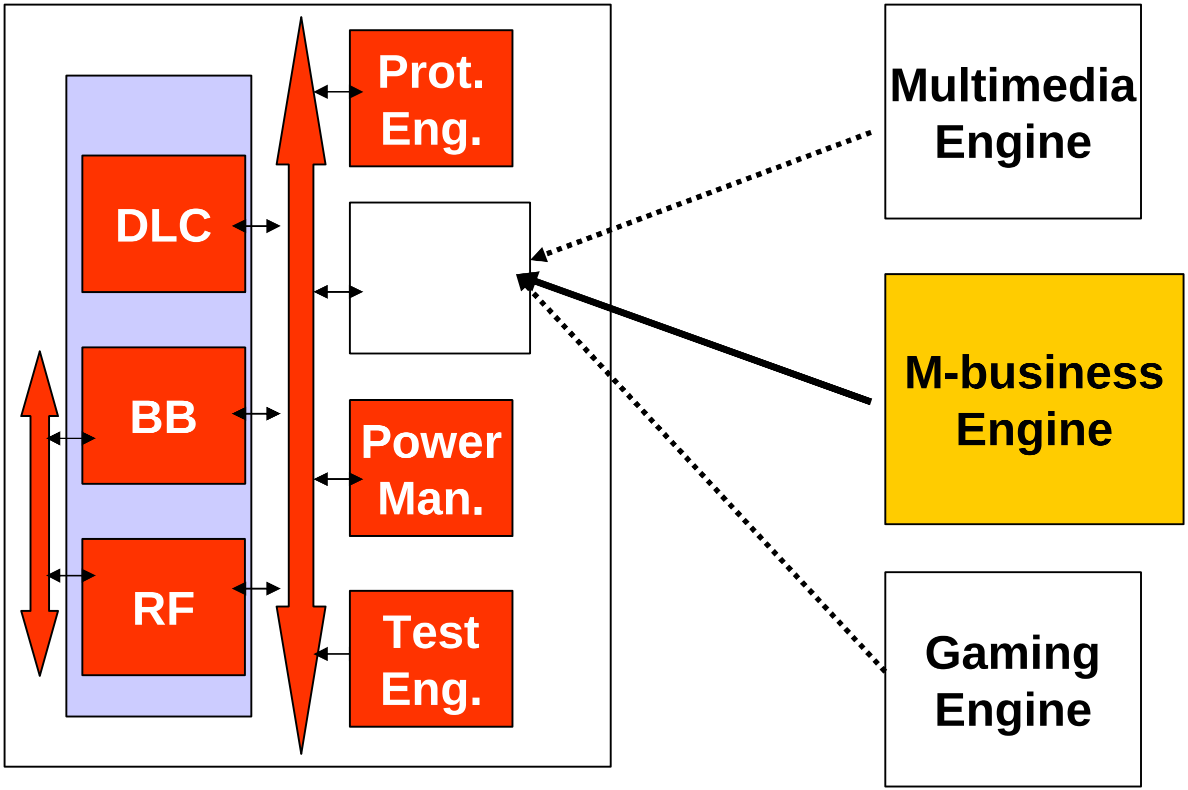
Architecture of TCP/IP/DL Device



Digital Coprocessors

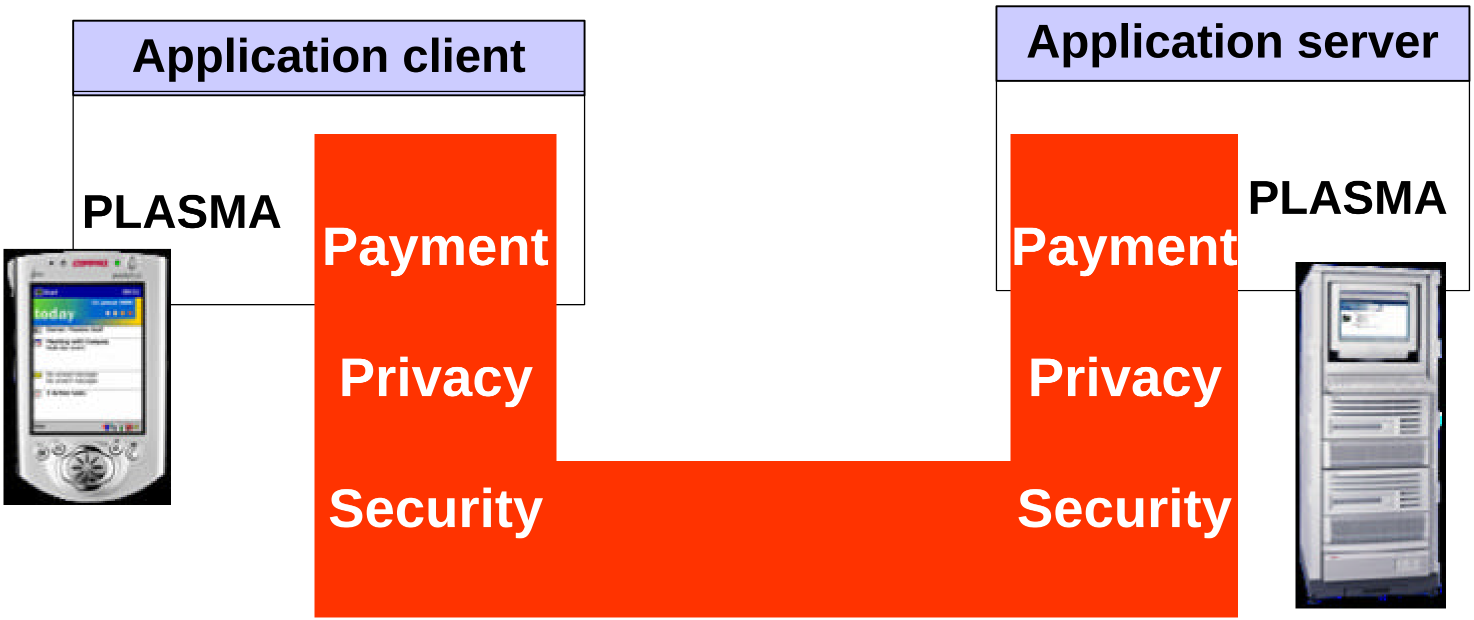
- **Certain basic protocols cost GIPS**
  E.g., Viterbi costs 3.5 GIPS
- **Indicates need for "hardwired" implementation**
  Particularly for frequently used algorithms
- **Hardwired solutions often eaten up by general purpose processors**
  Moore's law is cruel
- **Processors evolve by integrating such functions**
  E.g., floating point accelerators (386 -> 486 transition)
- **Develop accelerators for key functions**
  To work with *standard* processors and DSP's

M-business Engine Project



Overview of the work packages

Architectures: Security, Privacy, Payment

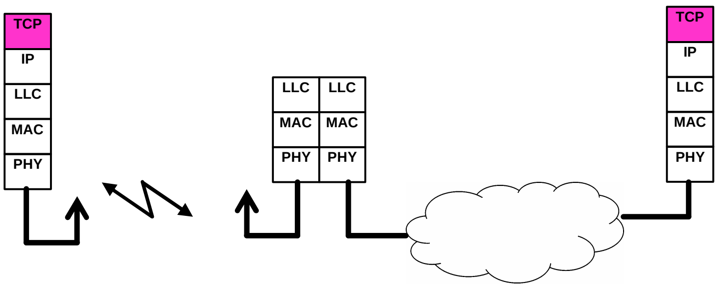


TCP/IP for wireless

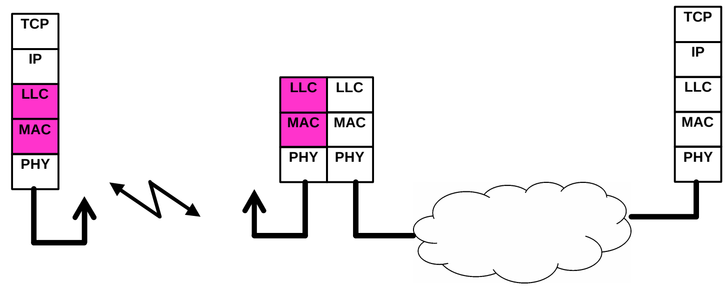
- TCP has been initially designed for wired low error rate communications
- Back-off behaviour after faults often not appropriate for wireless
  - Slow start after faults solves router congestion but not temporary channel interference
- TCP is useful for end-end semantics in Internet application scenarios
  - A chance of TCP semantics requires changes in billions of client and is not feasible
- Other solutions are needed to overcome the problems

Minimal change and maximal use scenarios

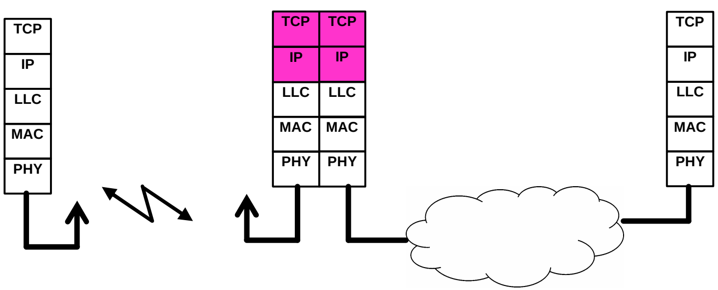
Modified TCP



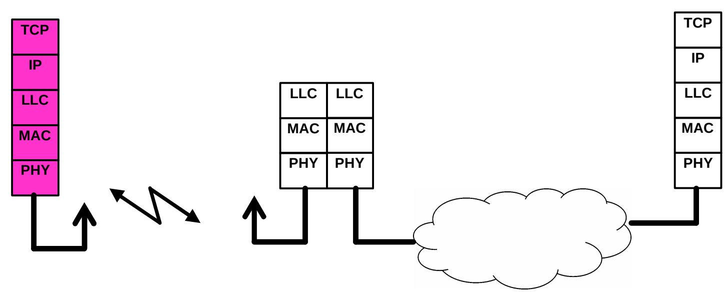
Modified Link Layer



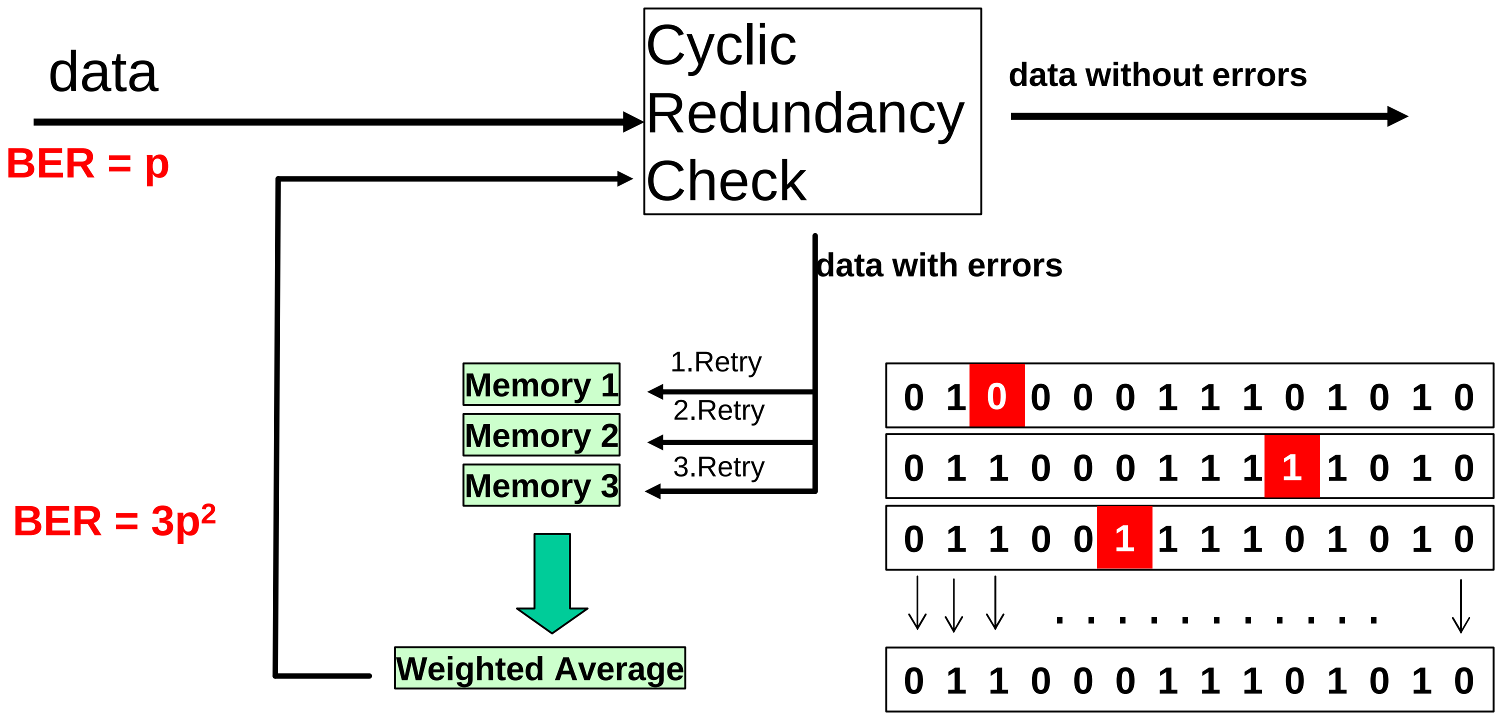
Split Connection



Modified Mobile



Combining Defective Packets: Principle



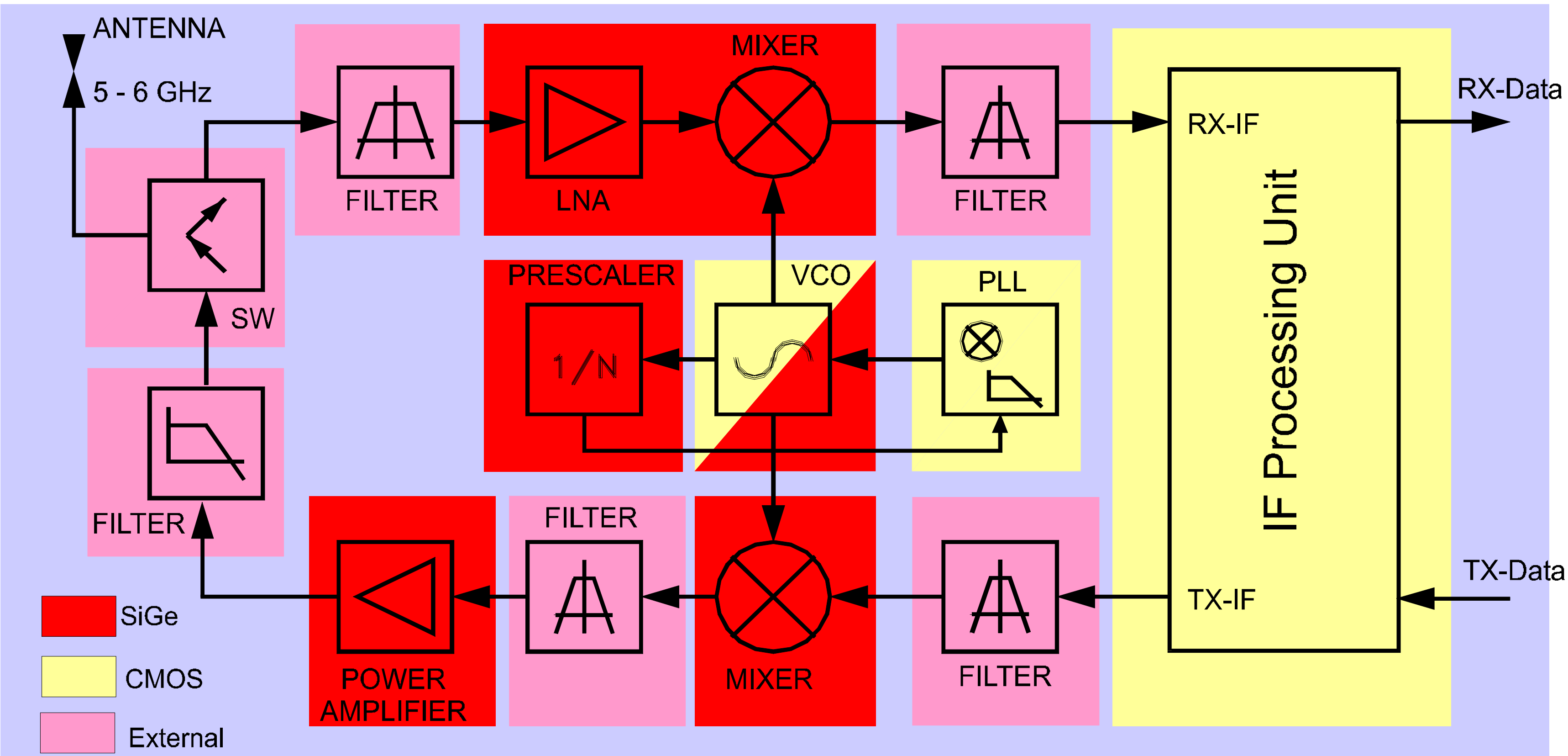
$10^{-3} \Rightarrow 3*10^{-6}$

RF Blocks

- RF I/O one of the biggest challenges
  - RF design is an art
  - RF designers behave like artists
- Large range of frequencies
  - From 2.4 - 60 GHz
- Lots of discussion about new architectures, few results
  - Alcatel direct-conversion phones stink!
- Need library of RF “transceiver macros”
  - Technology dependent, high value
- Must solve cross-talk problem
  - By brute force, or finesse; circuit or technology tricks

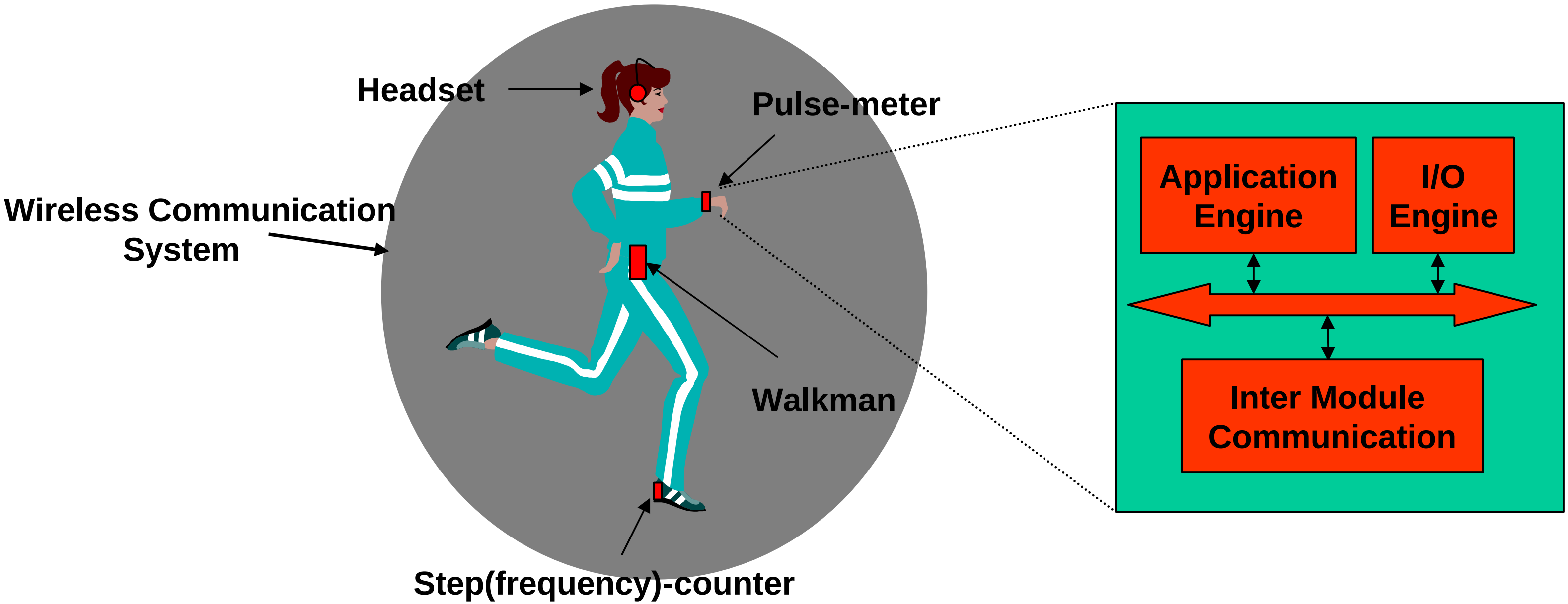
5.8 GHz Transceiver

RF Transceiver Block Diagram

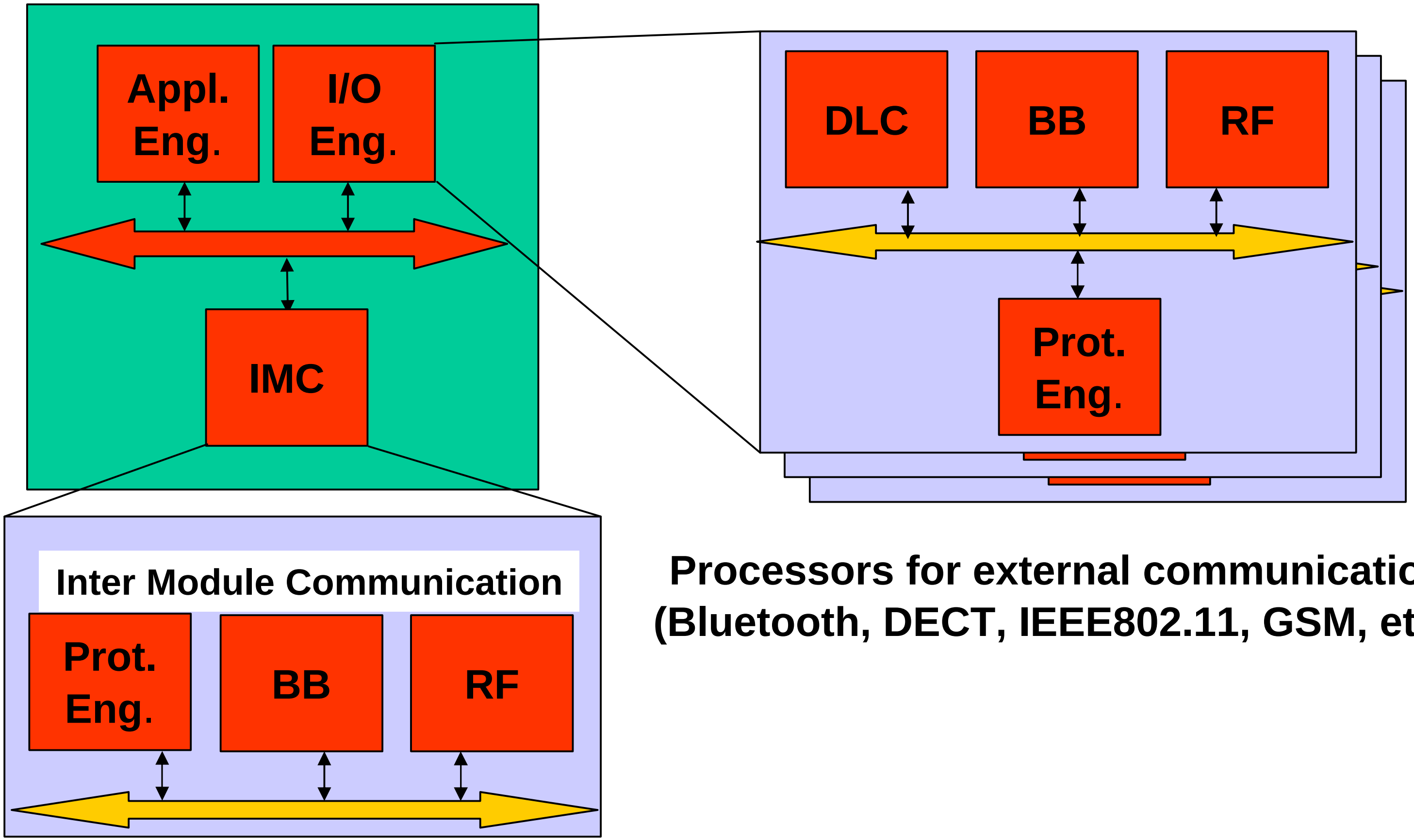


Body Area Networks

- BAN: Assembly of wirelessly connected devices worn on the body
  - All devices share common "BAN engine"
  - All devices share distributed intelligence
  - Enables new applications: e.g. "Personal Trainer"

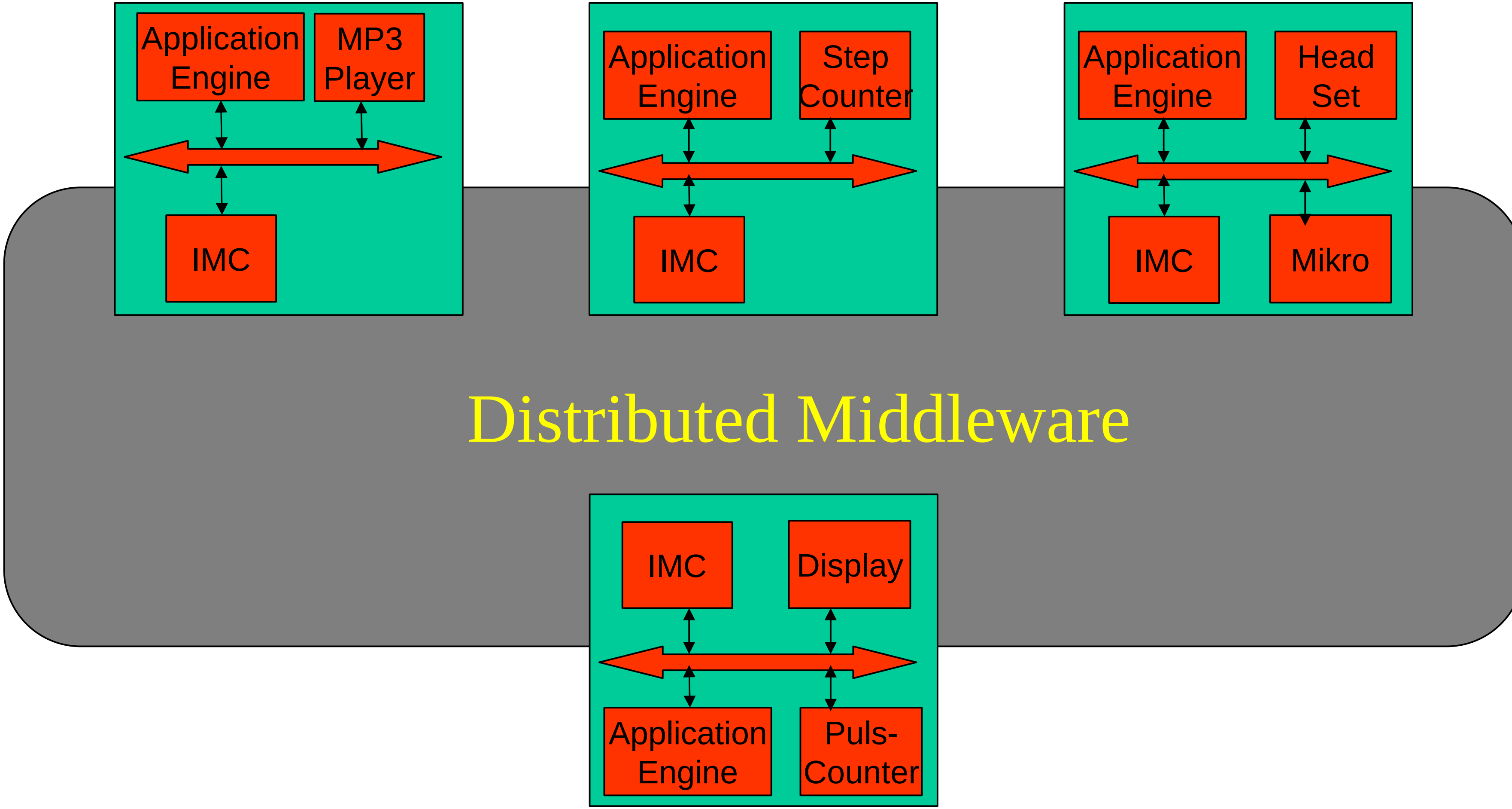


Distributed Wireless Engine (Body Area Networks)

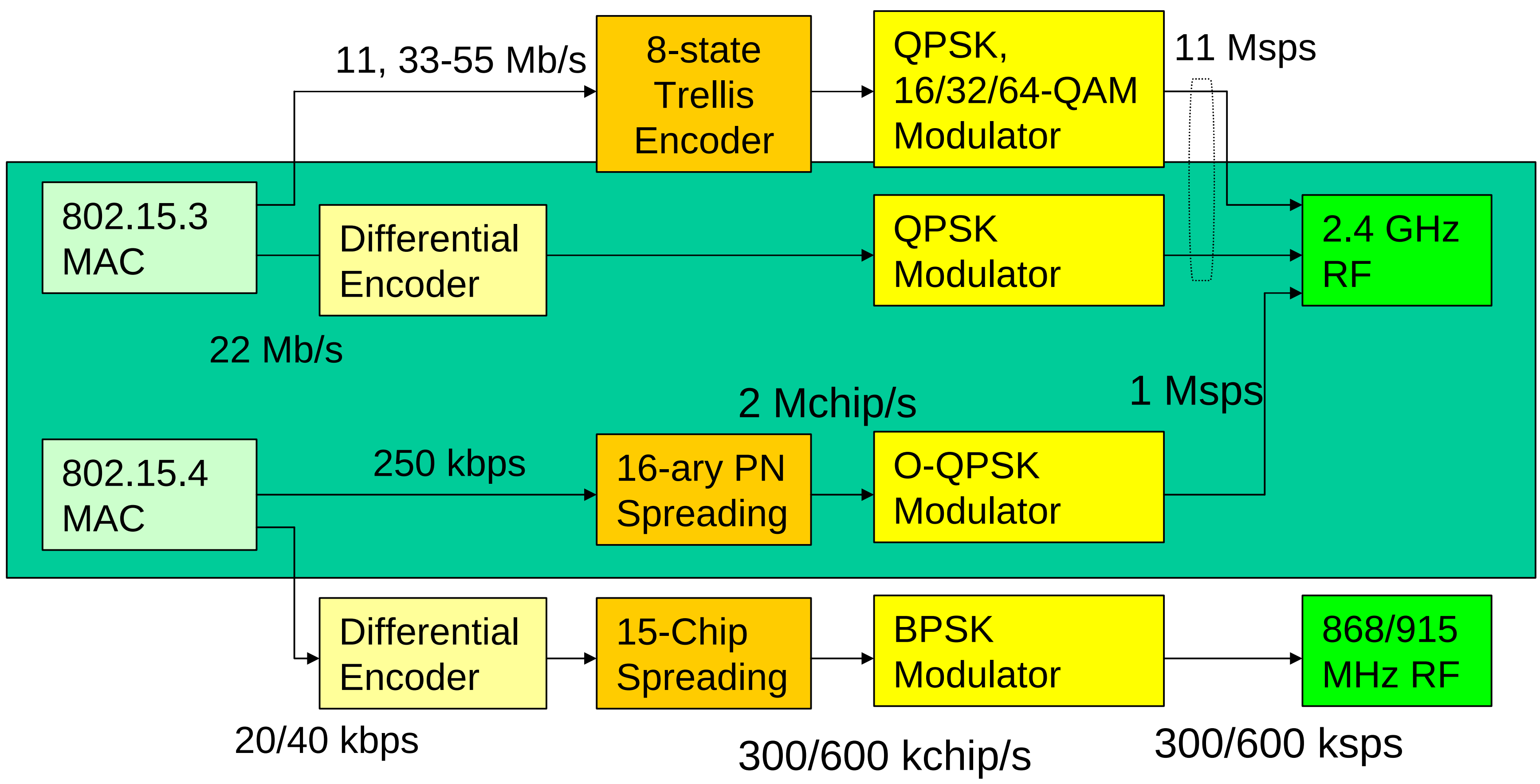


Processors for external communication (Bluetooth, DECT, IEEE802.11, GSM, etc.)

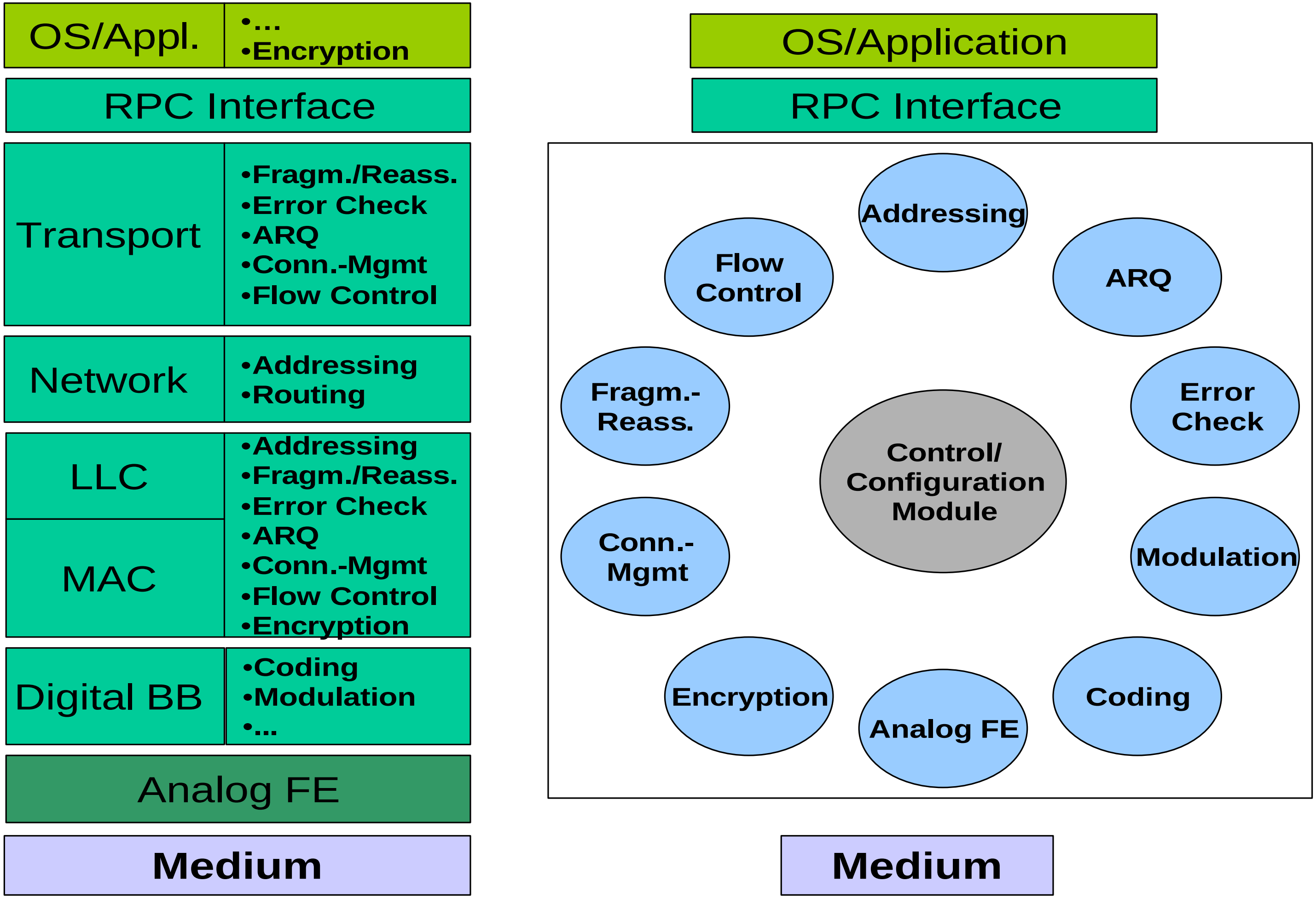
Example of a body area system



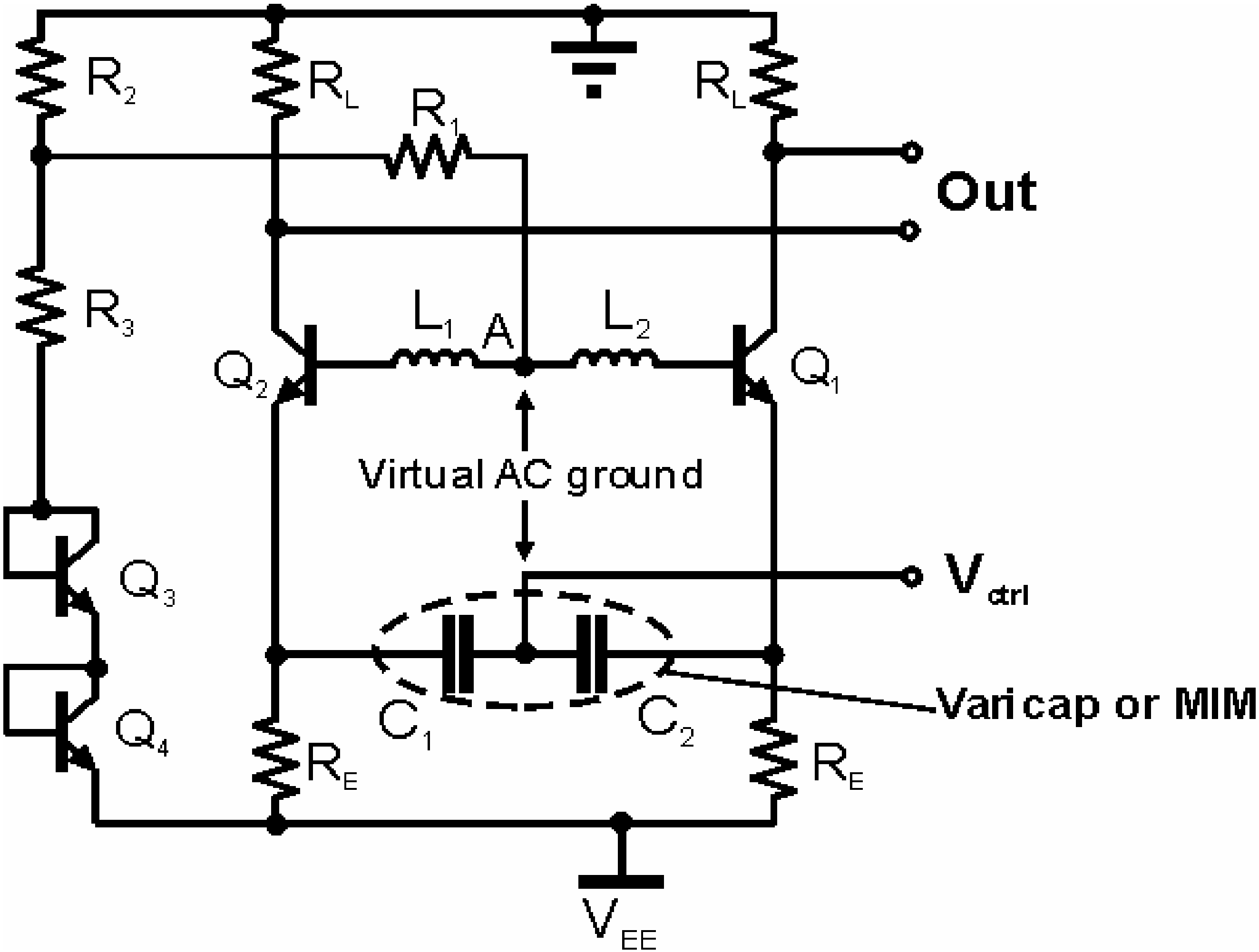
BAN with Wake-up using 802.15.4/4 in 2.4 GHz



From Protocol Stack to Functional Network



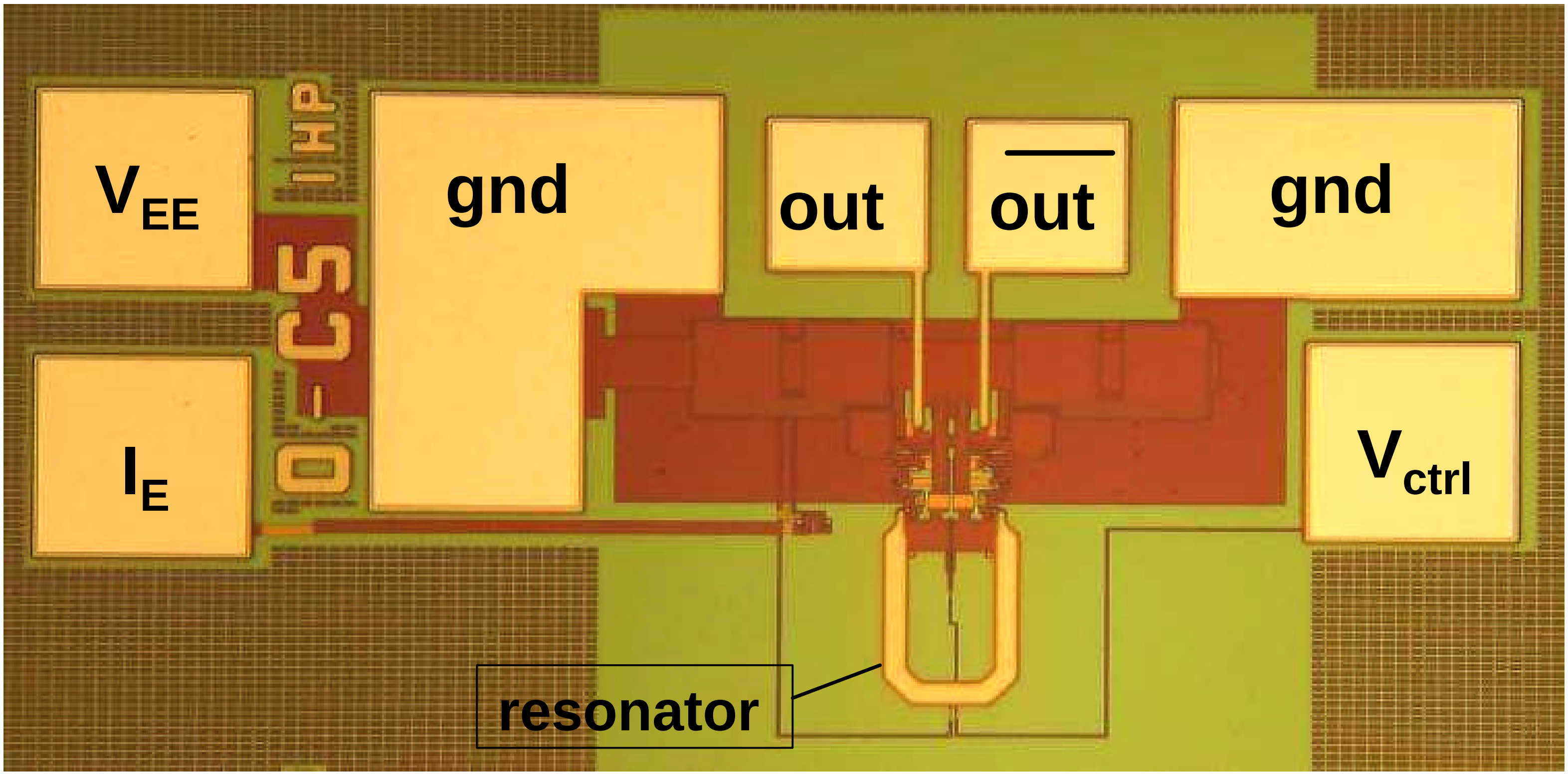
VCO Circuit Principle



Measurement Results

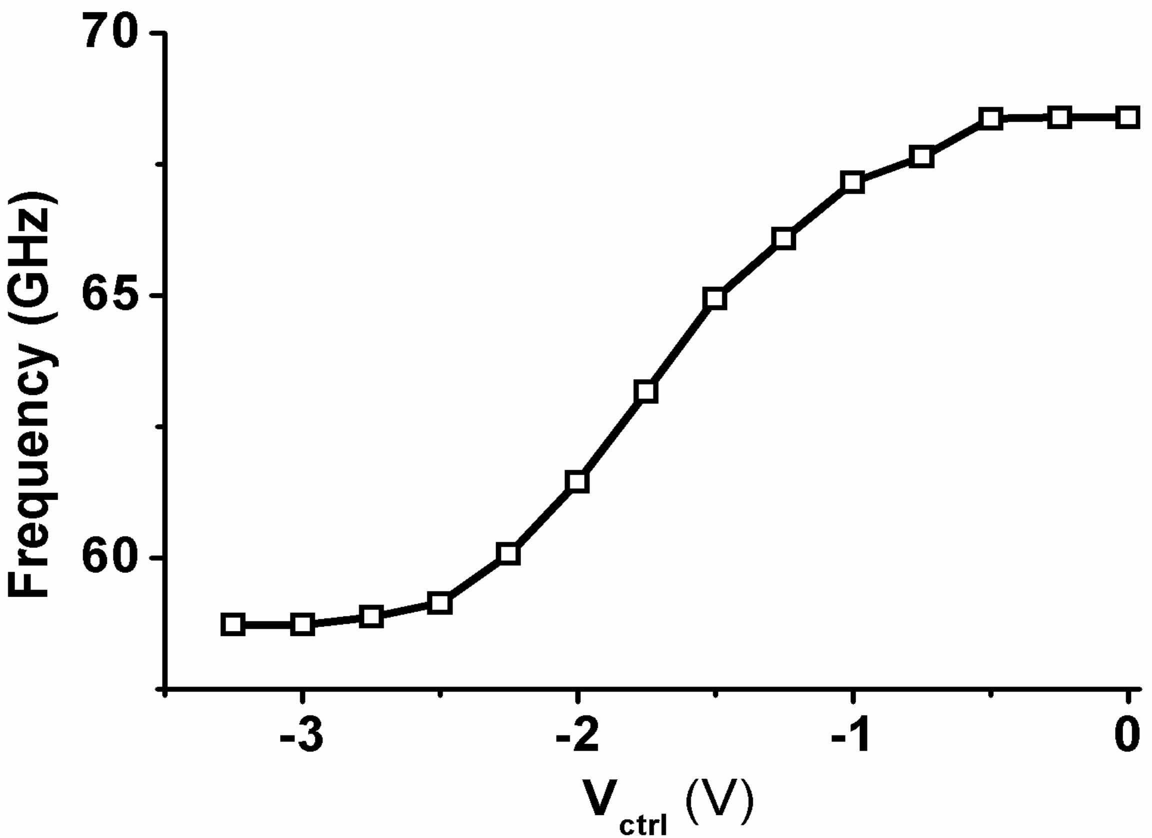
Parameter	60 GHz VCO	76 GHz Oscillator
Supply voltage	-3.0 V	-4.0 V
Supply current	24.6 mA	32 mA
Center frequency	63.6 GHz	76.1 GHz
Tuning range	9.8 GHz	-
Output power	-17dBm	-7 dBm
Phase noise at 1MHz offset	- 87 dBc/Hz - 84 dBc/Hz*	-91 dBc/Hz
Chip size	750x400 μm^2	750x400 μm^2

60 GHz VCO Micrograph

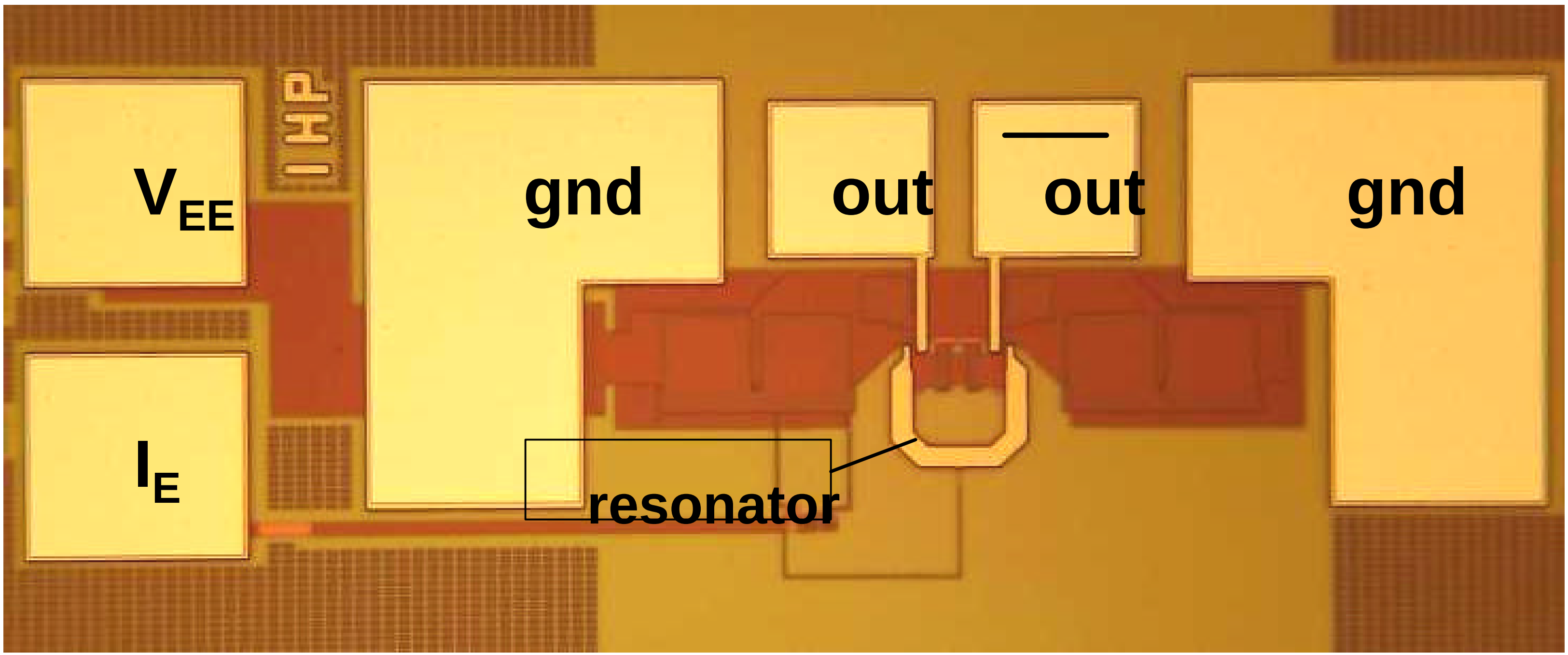


A_{chip}=750 x 400 µm^2, L=126 pH, C_{max}=150 fF

Tuning Range

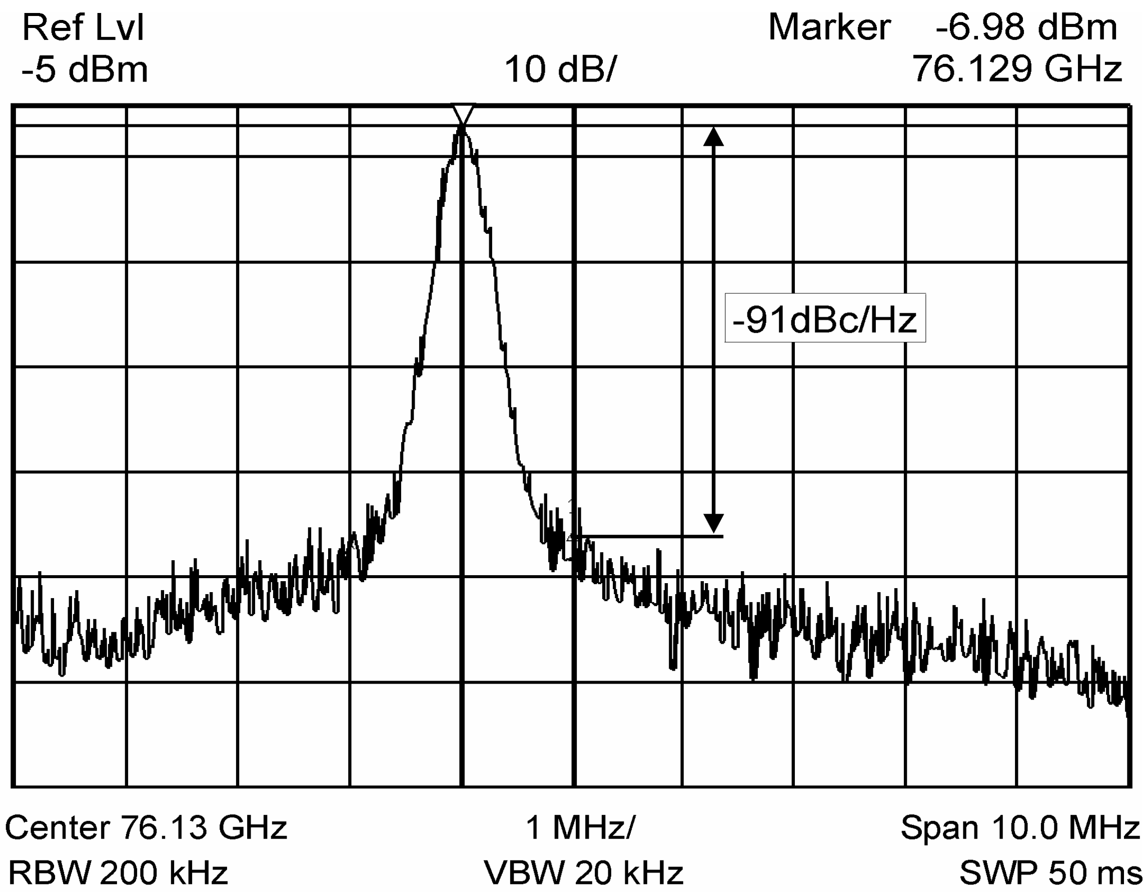


76 GHz Oscillator Micrograph



A_{chip}=750 x 400 µm^2, L=90 pH, C_{MIM}=120 fF

Measured Spectrum



C Suppresses B Diffusion

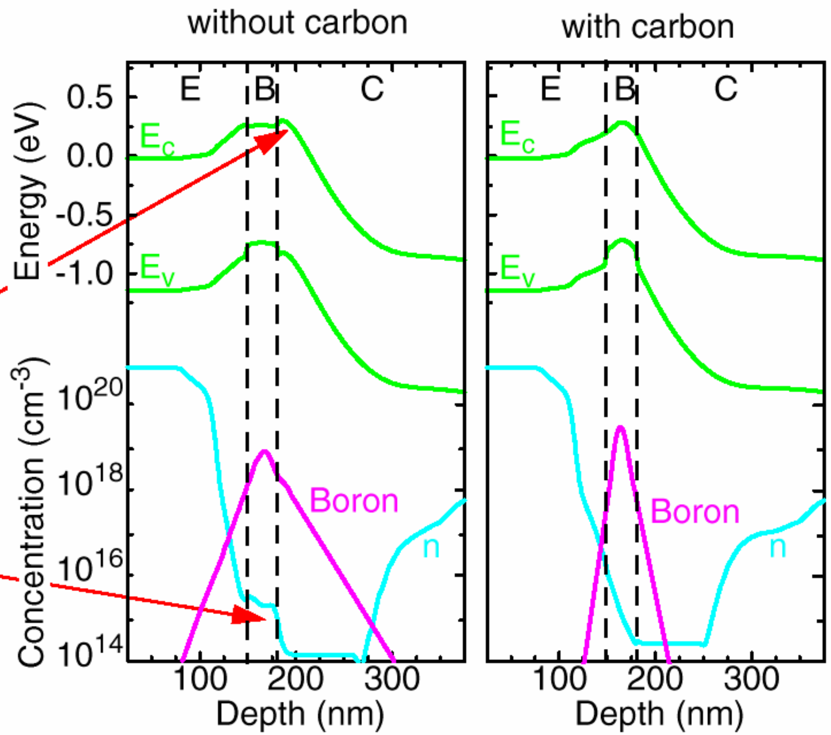
B outdiffusion

↓

Barriers in conduction band

↓

Reduced collector current
Electrons accumulate in base
Reduction of f_T



Conclusions

- IHP is a highly innovative research institute with
  - Vertical structure for full system solutions
  - Modern equipment including class-1 clean-room
  - Highly educated/motivated people
- Start-ups and Spin-offs are part of the strategy to create sustainable jobs in east Brandenburg
- Industrial relations in high end systems, circuits and technology are key to our success