Von AMANDA zu ICECube - die Weiterentwicklung des Detektors

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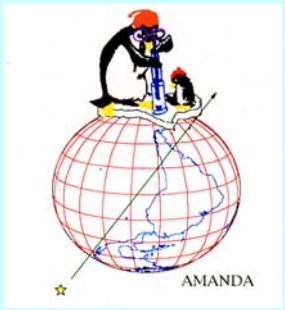
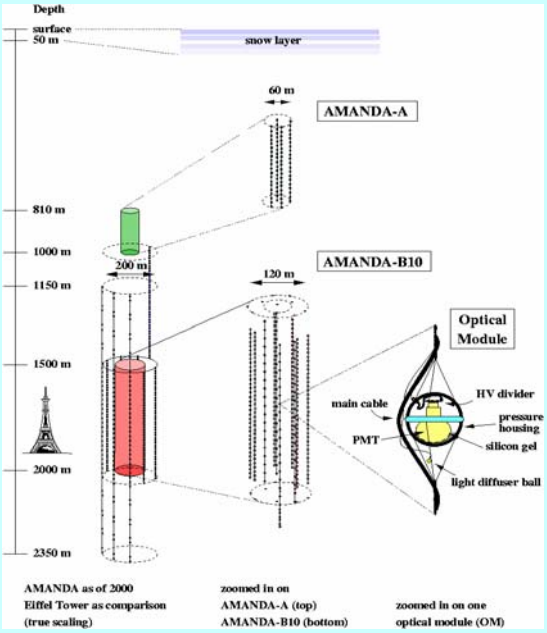


Outline

- The Amanda Experiment
- Optical Module Concepts
- dAOM Architecture
- dAOM Control System at the Surface
- dAOM++
- DOM Architecture
- Possible Contributions to ICECube Hardware Design

The AMANDA detector in the ice at the Southpole

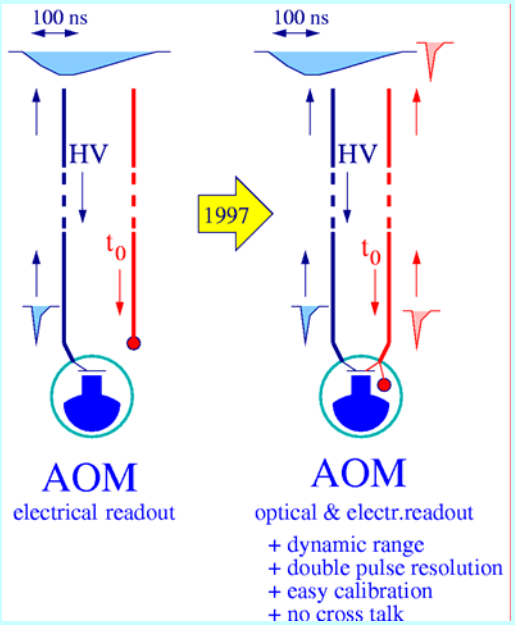


Optical Module Concepts

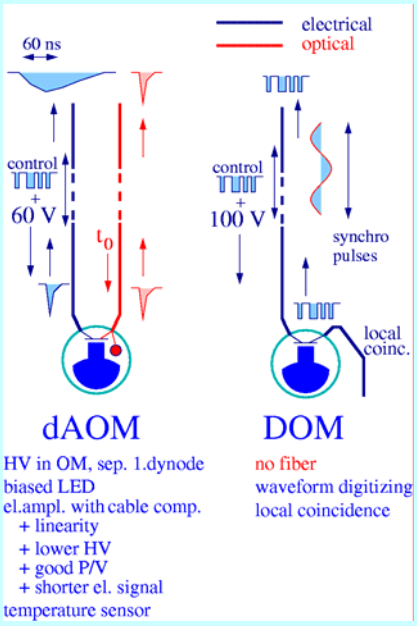
During the lifetime of AMANDA 3 different types of OMs have been developed:

- The Analog Optical Module: AOM
- The digitally controlled Analog Optical Module: dAOM
- The Digital Optical Module: DOM

AMANDA: Analog Optical Modules



Optical Modules with new Technology



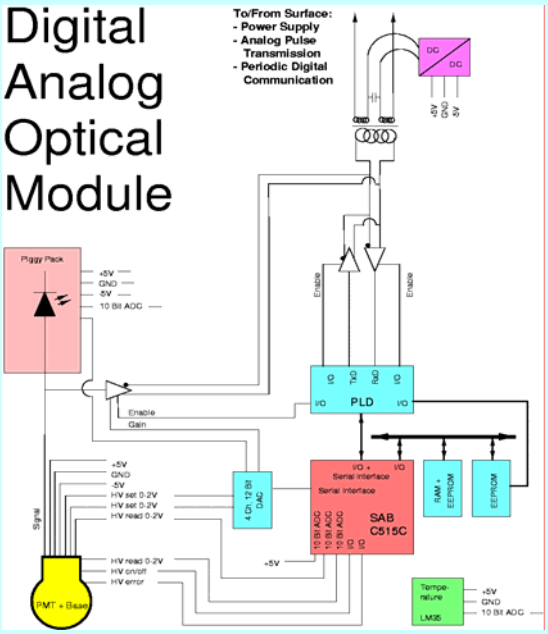
dAOM - Design Motivation:

- Active, analog optical PMT pulse transmission via fiber driven by a LED/laser diode
- Additional active, analog electrical PMT pulse transmission via twisted pair cable in case of fiber damages (at PMT gains ≤ 10^8)
- start with a conservative/'primitive' dAOM deployed in 1999/2000 in small number to check whether inteligent designs are working in the ice at all
- do a transition towards the 'more advanced' dAOM++ later

Design Goals:

- Reliability
- Cost Efficiency, Flexibility
- Easy to deploy and to exploit
- Low power consumption

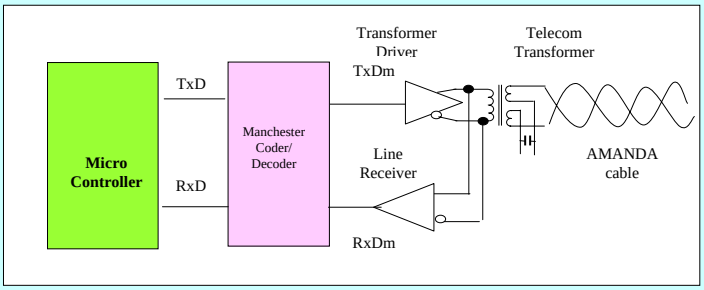
dAOM Architecture



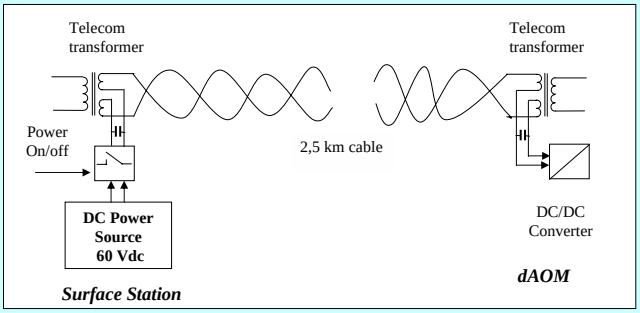
dAOM - Surface Communication

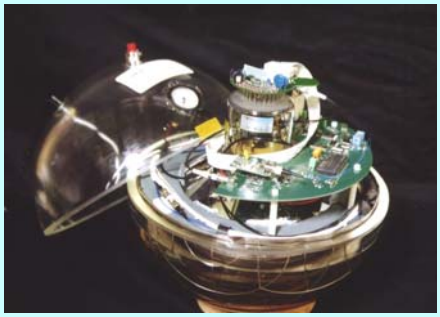
The implemented solution for communication uses the following protocols:

- Physical layer:
  - Manchester coded digital signal transfer based on a carrier of 320 kHz
- Data link layer:
  - self defined ASCII based frame structure protocol
- Network layer:
  - half duplex data transfer with a clear defined master-slave relationship

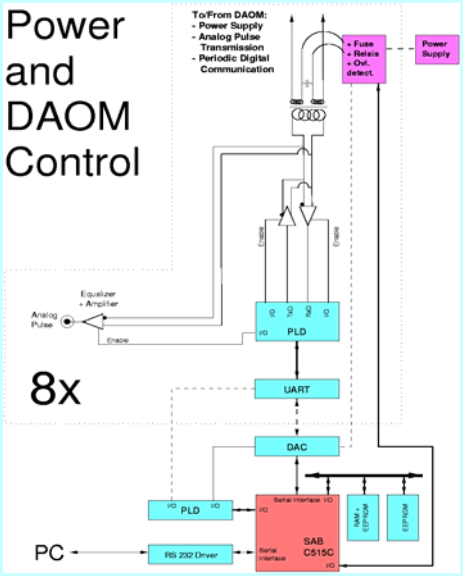


Remote Power Supply & HV





The dAOM Surface DAQ System



Deployed dAOM by numbers:

LED-dAOMs:

11 LED-dAOMs built (six 8 inch PMTs, five 10 inch PMTs)
11 LED-dAOMs tested at Pole for deployment
10 LED-dAOMs deployed at String 17, 18, 19
10 LED-dAOMs are fully operating (except for fiber damages)

LD-dAOMs:

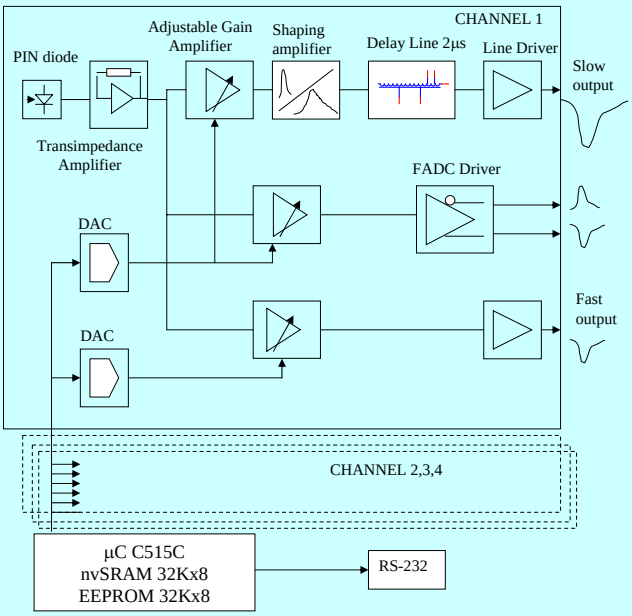
21 LD-dAOMs built
21 LD-dAOMs tested at Pole for deployment
13 LD-dAOMs deployed at String 17, 19
10 LD-dAOMs were fully operating (except for fiber damages)

1 LD-dAOM: anode HV not working ← ???
1 LD-dAOM: dynode/anode HV instable ← sparking ← bad PMT soldering
1 LD-dAOM: no signals, but full functionality ← connection between base and dAOM board damaged

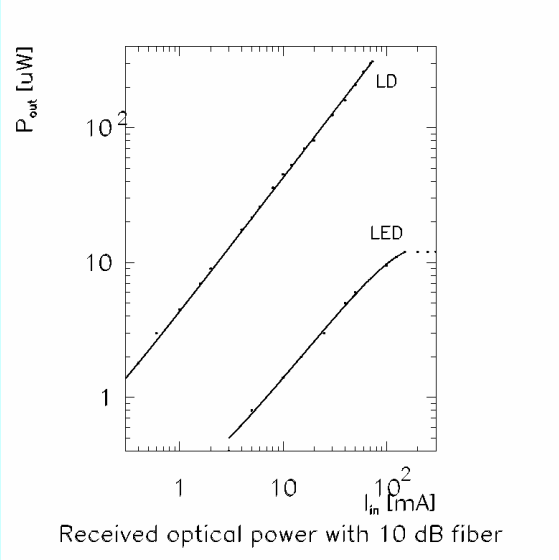
The Optical Receiver Module (ORM):

--> Optical Receiver for LD OMs (but also working with LED)

- Problem: fast LD pulses do not pass the 2 μs delay line
- General rule: $FWHM_{input\ pulse} \approx 10\%$ delay time
- Solution: pulse shaping (not trivial!!!)



Received optical power with 10 dB fiber attenuation using the UW LED Piggy Pack and UCI LD Piggy Pack :



Requirements on IceCube technologies dictated by science

The requirements can be summarized as follows:

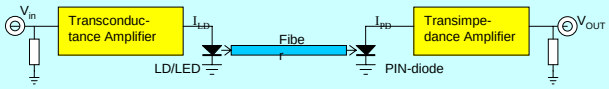
- time resolution of ≤ 5 nsec rms,
- waveform digitization with 200-320 Msps,
- dynamic range of ≥ 200 PE/15 nsec,
- dead time of ≤ 1%,
- gain variation of ≤ 2% per week.

dAOM++ design motivations:

- Extend dynamic/PE range (> 200 PE/15ns)
- Extend dAOM with features for automatic calibration procedures
- calibration of non-linear components
- interstring calibration
- T0-calibration
- Use full duplex standard communication protocol with the possibility of connecting several dAOMs to one twisted pair cable
- Reduce part counts by higher integrated components
- Explore new technologies like VCSELs

The Optical Transmitter Module (OTM):

Fiber optic interface basics:



The max. needed optical power for the transmitter depends on the attenuation of the fiber link and dynamic range and the sensitivity of the receiver:

Fiber attenuation/loss:
- Connector loss: 0.2 dB
- Splice loss: 0.2 dB
- Fiber loss: MM fiber: 3 dB/Km @ 850 nm or 1 dB/Km @ 1300 nm
- SM fiber: 0.4 dB/KM @ 1300 nm

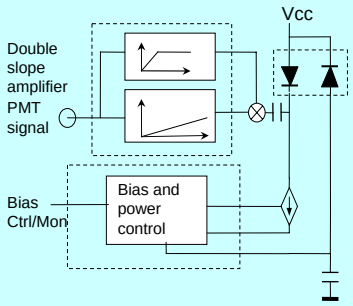
Using a 3 Km fiber with one splice and 4 connectors @ 1300 nm: 4 dB

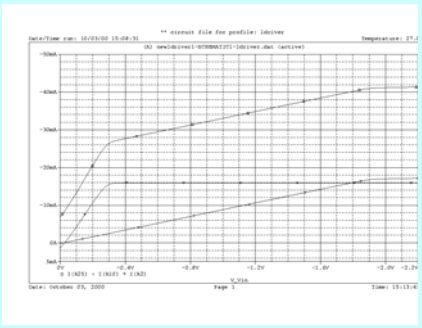
Dynamic range: 1 : 1000 → 30 dB
Sensitivity: > 30 dBm

4 dBm optical trans-mitted power

Parameter	LED Lytel 259012-2	VCSEL HFE 4080-321 XBA	VCSEL HFE 4080-321	LD OECA LQ5 – 1310 – 3.0f with ML725 B8F	LD FU-17SLD-F1
Optical output power [mW]	0.08	0.4	1.8	3.0	2.5
Operating current [mA]	< 150	< 20	< 20	< 35	< 28
Threshold current [mA]		< 6	< 6	< 15	<15
Differential efficiency [mW/mA]		0.25	0.25		0.07
Central wavelength [nm]	1290	850	850	1310	1300
Fiber	MM	MM	MM	MM	SM
Rise and fall time [ns]	< 4	< 0.3	< 0.3		< 0.5

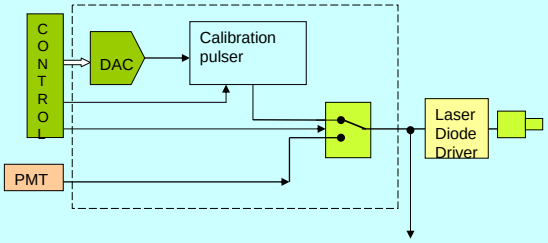
-The dual slope Optical Transmitter Module for LDs and VCSELs:

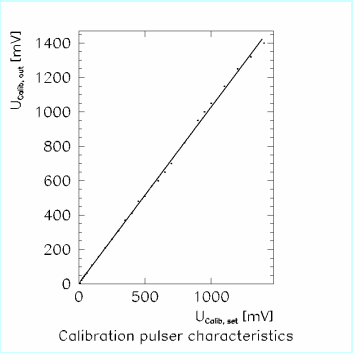




The calibration circuit:

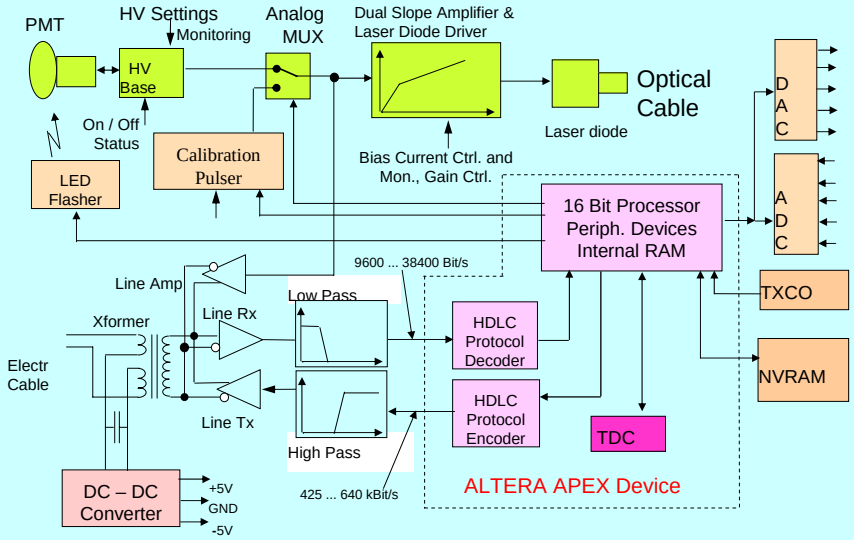
To correct for non-linearities of the active, analog optical/electrical pulse transmission we need a calibration circuit producing **'PMT-like' fast pulses**:





Calibration circuit produces negative 'triangular' pulses with 10 ns FWHM between 1 mV and 1500 mV!

The dAOM++ design overview:



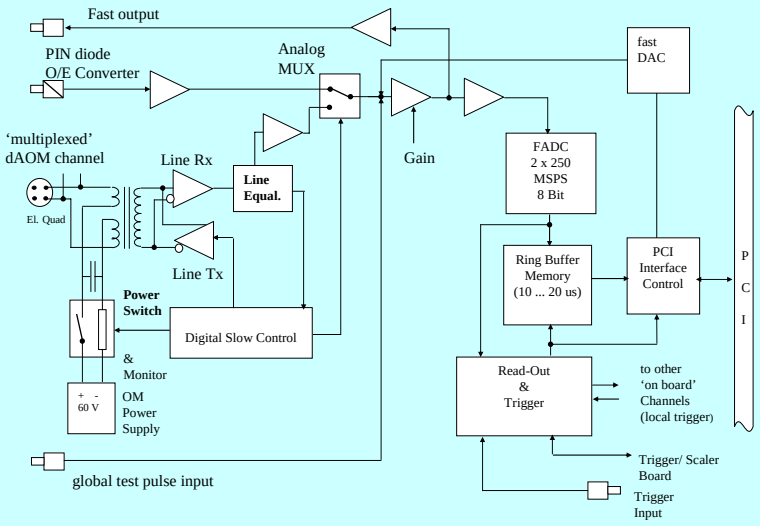
Power supply, HV, FPGA, CPU and digital communication:

- Input power supply via the same TP cable used for data transmission
- Galvanic separation with telecom technology transformer
- VAC transformer can handle upto 160 mA DC current → upto 4 W for two dAOMs
- Input voltage 60 VDC
- Using telecom technology DC/DC converter
- Ericsson DC/DC converter has high efficiency (83%), and high MTBF (4.9 Mh)
- HV: ISEG base

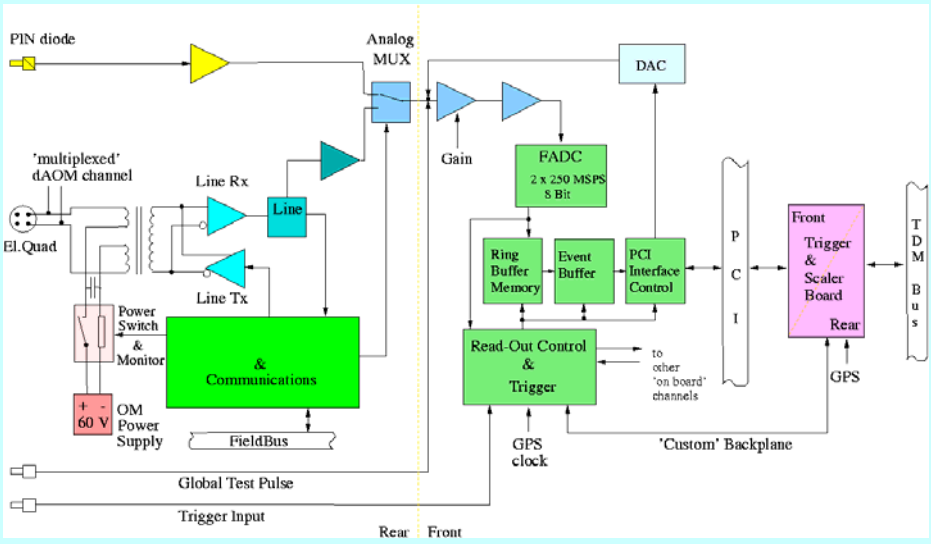
- Digital communication is duplex transmitted using different carrier frequencies
- Digital communication has been successfully tested via 2.7 Km TP cable at a rate of 625 Kbit/s
- Communication protocol: High level Data Link Control (HDLC)
- HDLC controller + coder/decoder implemented in FPGA using core from Innocor Ltd.

- FPGA: ALTERA APEX
- CPU: 16-bit integer RISC processor embedded in FPGA as softcore (NIOS)

dAOM DAQ System with PCI Interface

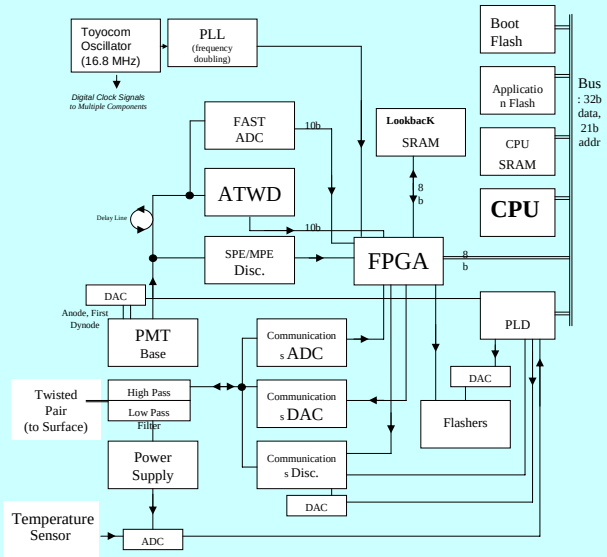


dAOM DAQ System with PCI Interface



Digital Optical Module

(First Prototype, Deployed 2000)



DOM-HUB: A Preliminary Proposal

K.-H. Sulanke, H. Leich, C. Spiering

3 ways of Implementation

- **Standard Compact PCI Solution**

plus:
- *off the shelf standard CPU's, good possibilty to tune the needed computing power*
- *optional less communication latency by using CPU's with Gigabit ethernet*
- *ethernet boot capability*
- *hot swap capability allows to mount DOM-HUB's under power*
- *high data rate (120 MBytes/sec) between DOM-HUB and CPU memory*
- *fast trigger decision in between up to 4 strings*
- *based on existing custom boards the development of a LINUX driver could start immediatly*

minus:
- *for the DOM-HUB a LINUX driver is needed*

- **Embedded PC**

- CPU AMD ELAN SC520 133 MHZ
- DRAM 16, 32 or 64 MByte onboard (128 MByte announced)
- Ethernet 10/100BaseT
- CompactFlash socket, easy upgradeable IDE flash disk
- 5V power only, max. 6W power consumption
- PCI and ISA businterface
- IDE, USB, COMn, LPT

plus:
- *off the shelf standard CPU's, good possibilty to tune the needed computing power*
- *ethernet boot capability*
- *high data rate (120 MBytes/sec) between DOM-HUB and CPU memory*

minus:
- *only up to 128 MByte DRAM available*
- *additional cost per DOM-HUB of about 350 US$, (sample: CPU 667.-DM, 64 MB DRAM 84.-DM)*

•**FPGA-only solution**

plus:

- *low latency, no operating system-overhead*
- *no special device driver needed*
- *ethernet boot capability*
- *only some knowledge of C is sufficient to change the DOM-HUB firmware*
- *low power consumption due to the missing of superfluous components*

minus:

- *less experience with the NIOS softcore*
- TCP/IP protocol has to be programmed

DOM - Hub, Blockdiagram, V.1

- 6 U CPCI board, 8 channels, 4 DOM's per channel